

HX4259-63-ST 10 MHz–3.0 GHz RF Switch

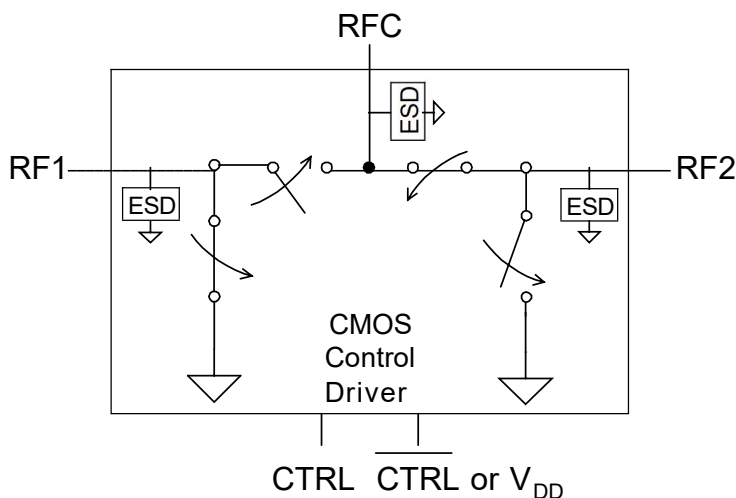
Product Description

The HX4259-63-ST UltraCMOS® RF switch is engineered to cater to a wide array of applications spanning from 10 MHz to 3000 MHz. This reflective switch integrates CMOS control logic onboard, complete with a CMOS-compatible control interface that operates at low voltage. It can be easily managed through either single-pin or complementary control inputs. With a nominal +3-volt power supply voltage, it achieves a typical input 1dB compression point of +33.5 dBm.

Manufactured using ZHHXDZ's patented UltraCMOS process, which is a unique variation of silicon-on-insulator (SOI) technology based on a sapphire substrate, the HX4259-63-ST combines the high performance of GaAs with the cost-effectiveness and integration capabilities of conventional CMOS.

Features

- ★ Single-pin or complementary CMOS logic control inputs
- ★ Low insertion loss:
 - (1) 0.5 dB @ 2000 MHz
 - (2) 0.35 dB @ 1000 MHz
- ★ Isolation of 30 dB @ 1000 MHz
- ★ High ESD tolerance of 2 kV HBM
- ★ Typical input 1 dB compression point of +33.5 dBm
- ★ 1.8V minimum power supply voltage
- ★ Ultra-small SOT-363 package

**SOT-363****Figure 1. Functional Diagram**

DOC-02109

Table 1. Electrical Specifications @ +25 °C, $V_{DD} = 3V$ ($Z_S = Z_L = 50\Omega$)

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operation frequency ¹		10		3000	MHz
Insertion loss ³	1000 MHz 2000 MHz		0.35 0.50	0.45 0.60	dB dB
Isolation	1000 MHz 2000 MHz	29 19	30 20		dB dB
Return loss ³	1000 MHz 2000 MHz	21 24	22 27		dB dB
'ON' switching time	50% CTRL to 0.1 dB of final value, 1 GHz		1.50		us
'OFF' switching time	50% CTRL to 25 dB isolation, 1 GHz		1.50		us
Video feedthrough ²			15		mVpp
Input 1dB compression point	1000 MHz @ 2.3–3.3V 1000 MHz @ 1.8–2.3V 2500 MHz @ 2.3–3.3V 2500 MHz @ 1.8–2.3V	31.5 29.5 28.5 28	33.5 30.5 30.5 29		dBm dBm dBm dBm
Input IP3	1000 MHz, 20 dBm input power		55		dBm

Notes: 1. Device linearity will begin to degrade below 10 MHz.
 2. The DC transient at the output of any port of the switch when the control voltage is switched from Low to High or High to Low in a 50 Ω test set-up, measured with 1ns risetime pulses and 500 MHz bandwidth.
 3. A tuning capacitor must be added to the application board to optimize the insertion loss and return loss performance. See *Figure 6* for details.

Figure 3. Pin Configuration (Top View)

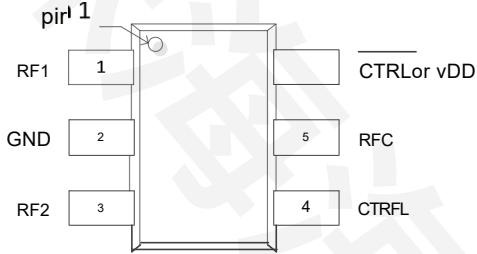


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RF1*	RF port 1.
2	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
3	RF2 ¹	RF port 2.
4	CTRL	Switch control input, CMOS logic level.
5	RFC ¹	RF common.
6	CTRL or V _{DD}	<p>This pin supports two interface options:</p> <p><i>Single-pin control mode.</i> A nominal 3-volt supply connection is required.</p> <p><i>Complementary-pin control mode.</i> A complementary CMOS control signal to CTRL is supplied to this pin. Bypassing on this pin is not required in this mode.</p>

Note: * All RF pins must be DC blocked with an external series capacitor or held at 0 VDC.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Unit
V _{DD} Power supply voltage	1.8	3.0	3.3	V
I _{DD} Power supply current (V _{DD} = 3V, V _{CNTL} = 3V)		9	20	μA
Control voltage high	0.7x V _{DD}			V
Control voltage low			0.3x V _{DD}	V

Switching Frequency

The HX4259-63-ST has a maximum 25 kHz switching rate.

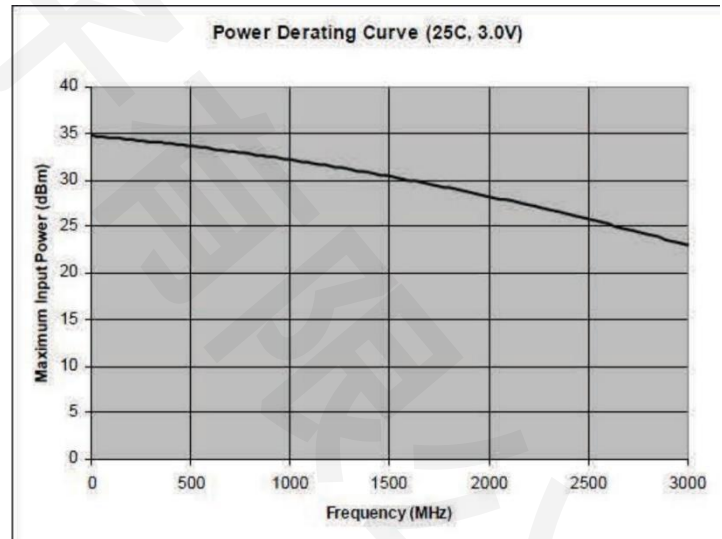
Table 4. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V _{DD}	Power supply voltage	-0.3	4.0	V
V _I	Voltage on any DC input	-0.3	V _{DD} +0.3	V
T _{ST}	Storage temperature range	-65	150	°C
T _{OP}	Operating temperature range	-40	85	°C
P _{IN}	Input power (50Ω)		+34*	dBm
V _{ESD}	ESD Voltage (HBM, ML STD 883 Method 3015.7)		2000	V
	ESD Voltage (MM, JEDEC, JESD22-A114-B)		100	V

Note: * To maintain optimum device performance, do not exceed Max P_{IN} at desired operating frequency (see Figure 4).

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Figure 4. Maximum Input Power



Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Table 5. Single-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 (V _{DD}) = V _{DD} Pin 4 (CTRL) = High	RFC to RF1
Pin 6 (V _{DD}) = V _{DD} Pin 4 (CTRL) = Low	RFC to RF2

Table 6. Complementary-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 (CTRL or V _{DD}) = Low Pin 4 (CTRL) = High	RFC to RF1
Pin 6 (CTRL or V _{DD}) = High Pin 4 (CTRL) = Low	RFC to RF2

Thermal Data

Psi-JT (Ψ_{JT}), junction top-of-package, is a thermal metric to estimate junction temperature of a device on the customer application PCB (JEDEC JESD51-2).

$$\Psi_{JT} = (T_J - T_T)/P$$

Where

Ψ_{JT} = junction-to-top of package characterization parameter, °C/W

T_J = die junction temperature, °C

T_T = package temperature (top surface, in the center), °C

P = power dissipated by device, Watts

Table 7. Thermal Data

Parameter	Typ	Unit
Maximum junction temperature, T _{JMAX} (RF input power, CW = 31.5 dBm, +85 °C ambient)	99	°C
Ψ_{JT}	37	°C/W
θ_{JA} , junction-to-ambient thermal resistance	104	°C/W

Control Logic Input

The HX4259-63-ST is a versatile RF CMOS switch that supports two operating control modes; single-pin control mode and complementary-pin control mode.

Single-pin control mode enables the switch to operate with a single control pin (pin 4) supporting a +3-volt CMOS logic input, and requires a dedicated +3-volt power supply connection on pin 6 (V_{DD}). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS μ Processor I/O port.

Complementary-pin control mode allows the switch to operate using complementary control pins CTRL and CTRL (pins 4 and 6), that can be directly driven by +3-volt CMOS logic or a suitable μ Processor I/O port. This enables the HX4259-63-ST to be used as a potential alternate source for SPDT RF switch products used in positive control voltage mode and operating within the HX4259-63-ST operating limits.

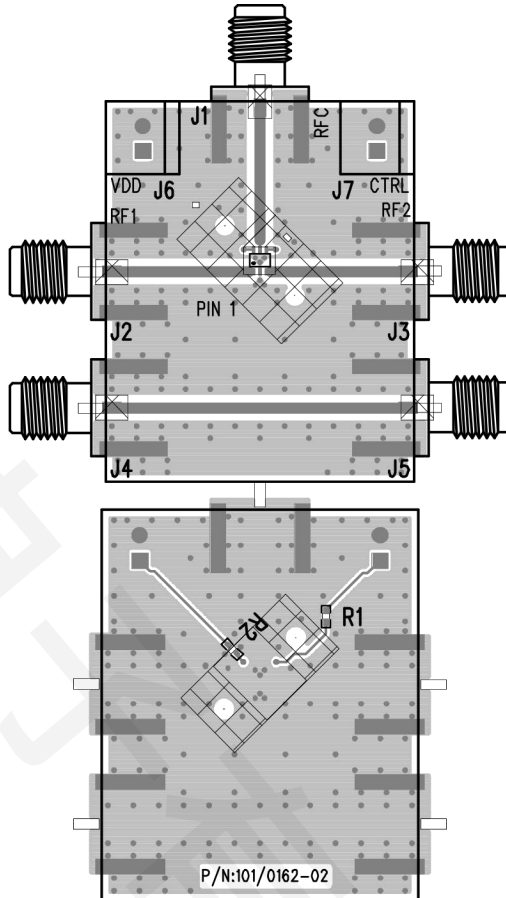
Evaluation Kit

The SPDT switch EK Board was designed to ease customer evaluation of ZHHXDZ's HX4259-63-ST. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J1. RF1 and RF2 are connected through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A through 50Ω transmission is available via SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ϵ_r of 4.4.

J6 and J7 provide a means for controlling DC and digital inputs to the device. J6-1 is connected to the device V_{DD} or CTRL input. J7-1 is connected to the device CTRL input.

Figure 5. Evaluation Board Layout



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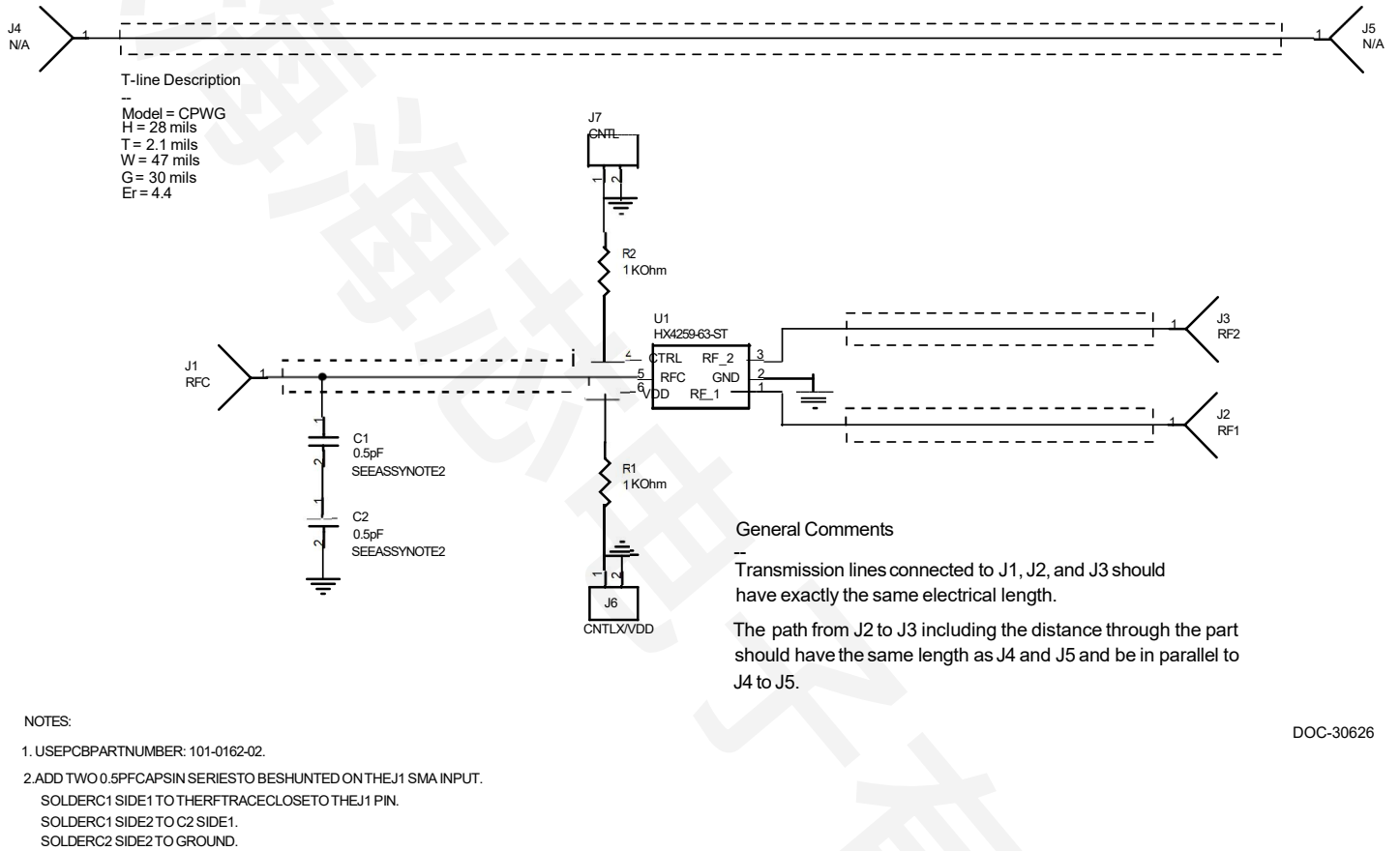


Figure 6. Evaluation Board Schematic

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Typical Performance Data @ -40 °C to 85 °C (Unless Otherwise Noted)

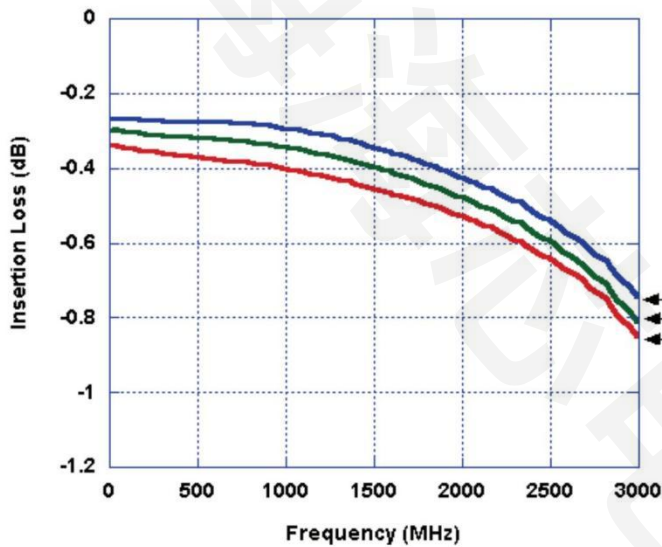


Figure 7. Insertion Loss

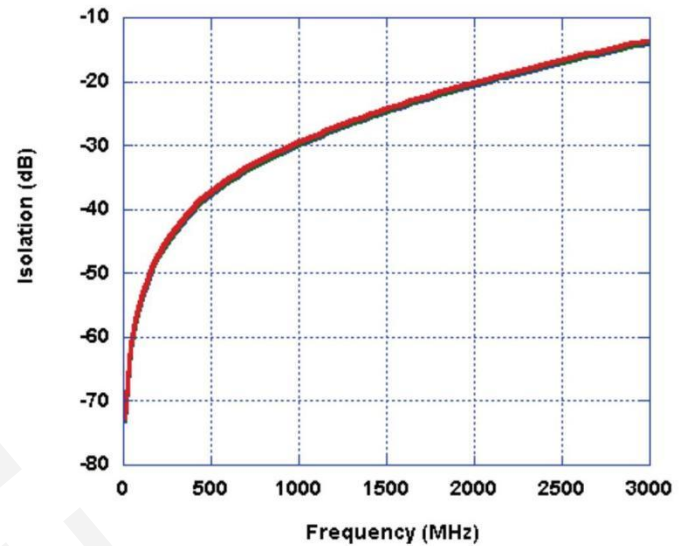


Figure 8. Isolation – Input to Output

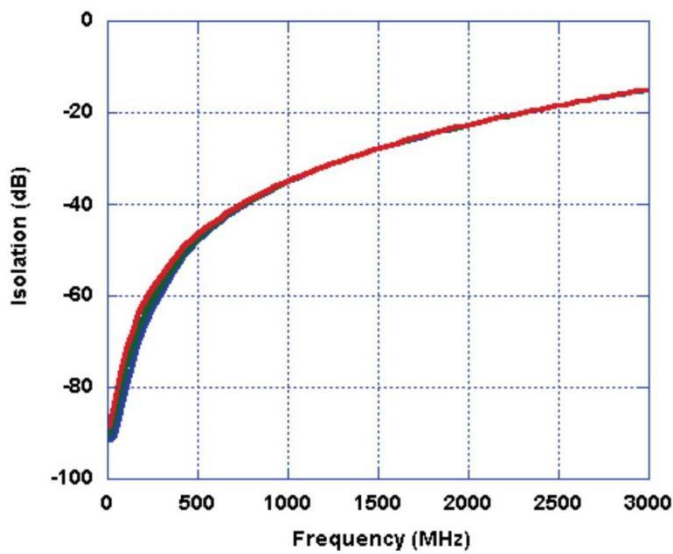


Figure 9. Isolation – Output to Output

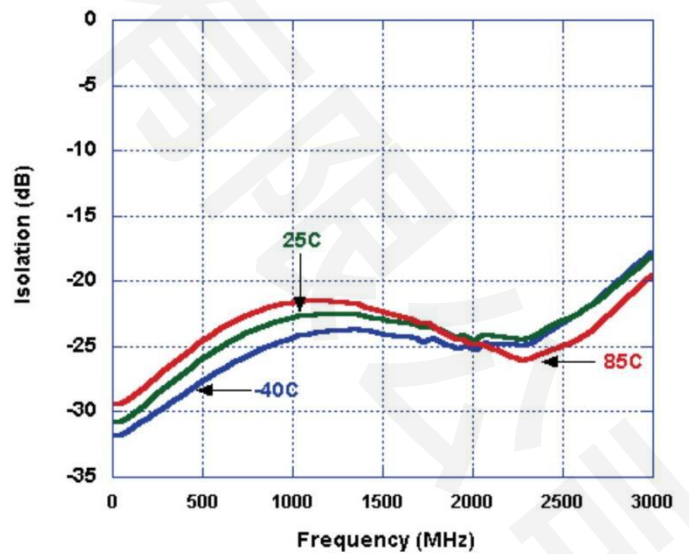


Figure 10. Return Loss (Input)

Typical Performance Data @ $V_{DD} = 2.3V$, $T = 25\text{ }^{\circ}C$

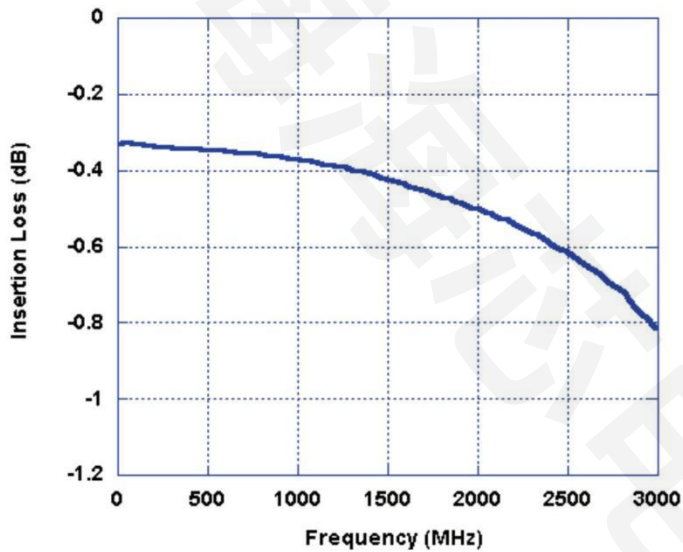


Figure 11. Insertion Loss

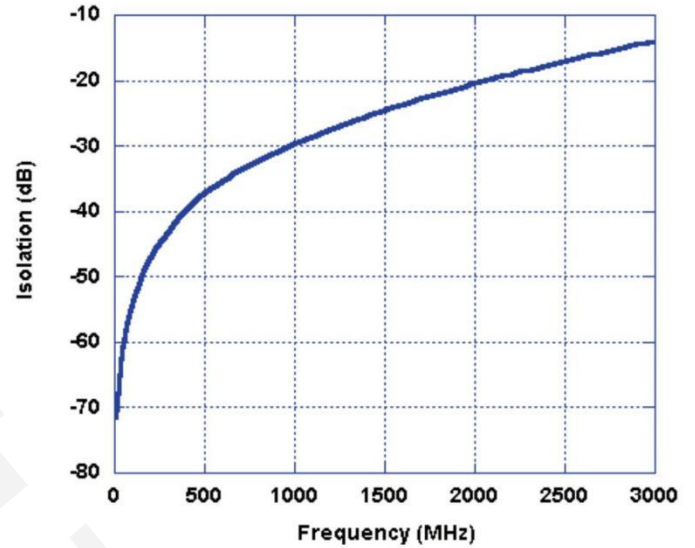


Figure 12. Isolation – Input to Output

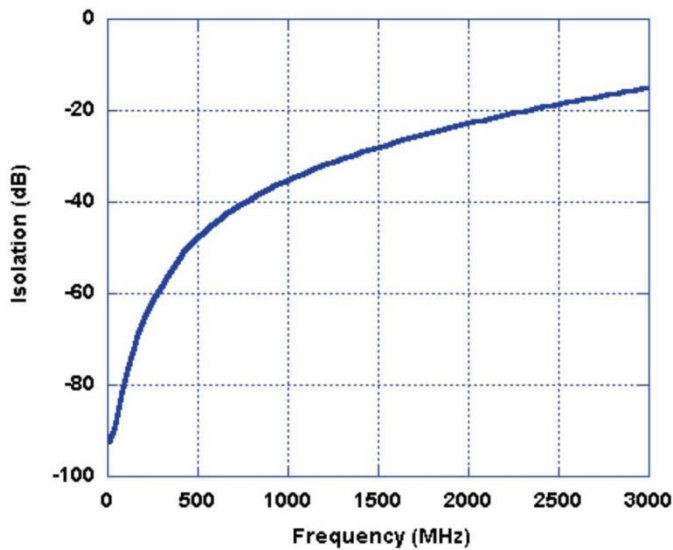


Figure 13. Isolation – Output to Output

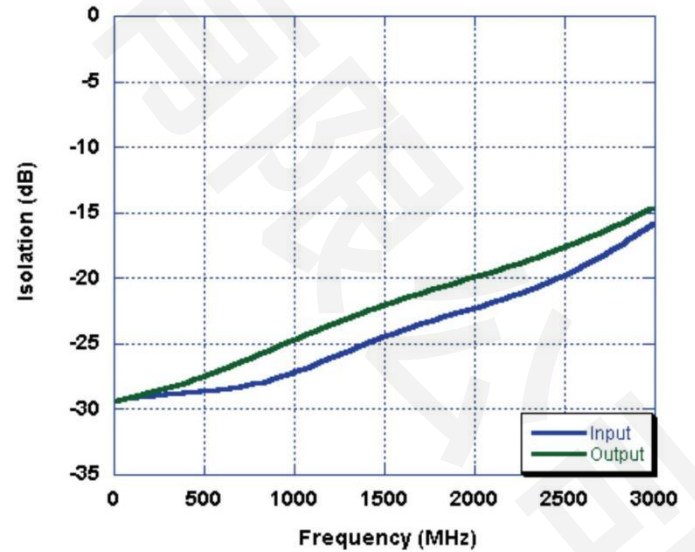


Figure 14. Return Loss (Input and Output)

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Figure 15. Package Drawing

SOT-363

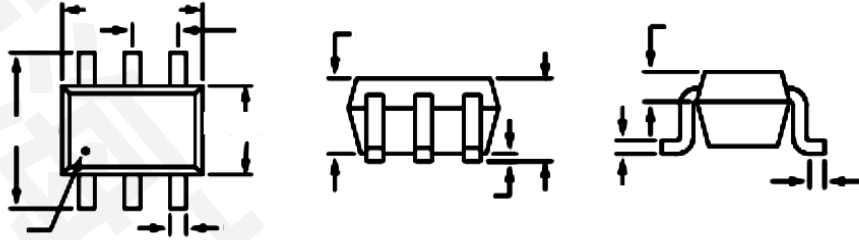


Table 7. Ordering Information

Part Number	Package Type	Package	quantity
HX4259-63-ST	SOT-363	Taping	3000