



GSV6155

Type-C/DisplayPort 1.4 Retimer with
Embedded MCU and PD Controller

Oct, 2023

Preliminary Product Specification

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Glossary

DDC	Display Data Channel
EDID	Extended Display Identification Data
ESD	Electrostatic Discharge
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I ² C	Inter-Integrated Circuit
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
OTP	One Time Programmable
PCM	Pulse Code Modulation
S/PDIF	Sony/Philips Digital Interface Format
SPI	Serial Peripheral Interface
TMD5	Transition Minimized Differential Signaling
SCDC	Status and Control Data Channel
CEC	Consumer Electronics Control
AUX	AUX_CH, DisplayPort Auxiliary Channel
DPCD	DisplayPort Configuration Data
Main-Link	Unidirectional channel stream from DPTX to DPRX
SDP	Secondary-data Packet
DDC/CI	VESA Display Data Channel/Command Interface
MCCS	Monitor Control Command Set (VESA)
DP	DisplayPort (VESA)
DPRX	DisplayPort Receiver
DPTX	DisplayPort Transmitter
DSC	Display Stream Compression
FEC	Forward Error Correction
HBR	DisplayPort High Bit Rate, HDMI High Bit-Rate Audio
MST	DisplayPort Multi-Stream Transport
SSC	Spread-Spectrum Clock

1. General Description

1.1 General Information

Gscoolink GSV6155 is a high-performance, low-power Type-C/DisplayPort 1.4 retimer. By integrating enhanced microcontroller, GSV6155 has created a cost-effective solution that provides time-to-market advantages. The DisplayPort Receiver and Transmitter support up to 32.4Gbps (HBR3, 4-lane). With embedded Channel Configuration (CC), Power Delivery (PD) controller and Billboard USB 2.0 controller, GSV6155 can support dual Type-C Alternate DisplayPort both as UFP and DFP in Type-C Alternate DisplayPort retimer application. The superior architecture of GSV6155 provides economical smaller footprint solutions using QFN64, targeting for low power embedded applications.

With extra pins for DFP USB 3.0 SS RX1/TX1, GSV6155 can support “C”/”D”/”E” pin assignments for both UFP/DFP which can be compatible with 4-lane Alt-DP mode and USB 3.0 + 2-lane Alt-DP mode.

Within 4KV HBM tolerance, GSV6155's operation temperature range is -45 °C to 85 °C using automotive qualified process.

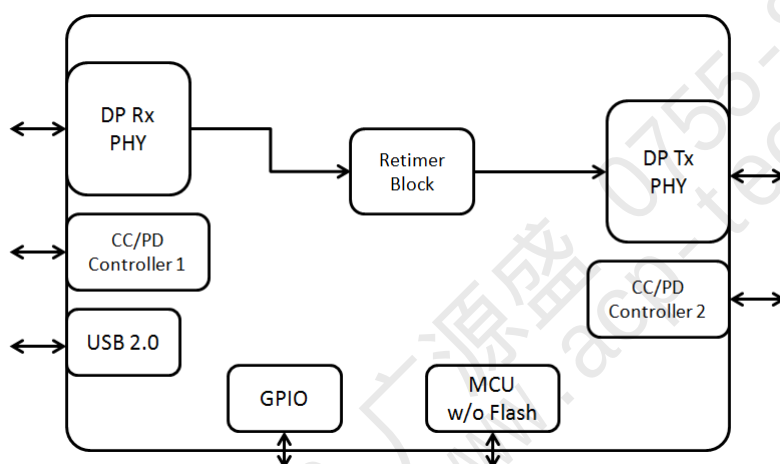


Figure 1. Top Diagram

1.2 Features

1.2.1 DisplayPort Receiver

- Compliant with VESA DisplayPort 1.4a

- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Compliant with both DisplayPort and USB Type-C Alternative Mode
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible MUX and Pins Swap
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support Full-Link Training and No-Link Training
- Embedded arbitrary EDID and MCCS
- Support Spread Spectrum Clock (SSC)

1.2.2 DisplayPort Transmitter

- Compliant with VESA DisplayPort 1.4a
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Compliant with both DisplayPort and USB Type-C Alternative Mode
- Support HBR3, HBR2, HBR and RBR (8.1/5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support Spread Spectrum Clock (SSC)

1.2.3 USB Type-C DisplayPort Alternative Mode Transceiver and

Receiver

- Compliant with USB Type-C 1.1/1.0 Specification
- Compliant with USB Power Delivery 3.0 Specification
- Programmable USB Type-C Channel Configuration function
- Support Billboard in USB 2.0

1.2.5 System Features

- Embedded MCU using External Flash
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO control from embedded MCU
- Mailbox feature for external MCU access on chip function status
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 Type-C Alt-Mode In to Out Application

RxPort is configured as Type-C Alt-Mode (DisplayPort) Rx Input. Together with on-chip CC, USB 2.0 IP support, Type-C USB input can be configured to DisplayPort 1.4a input stream for processing. TxPort is configured as DisplayPort Tx Output. Together with another on-chip CC IP support, Type-C USB output can be configured for DisplayPort 1.4a output stream.

2. Pin Description

2.1 Pin Diagram

QFN64 Pin definition is defined as below.

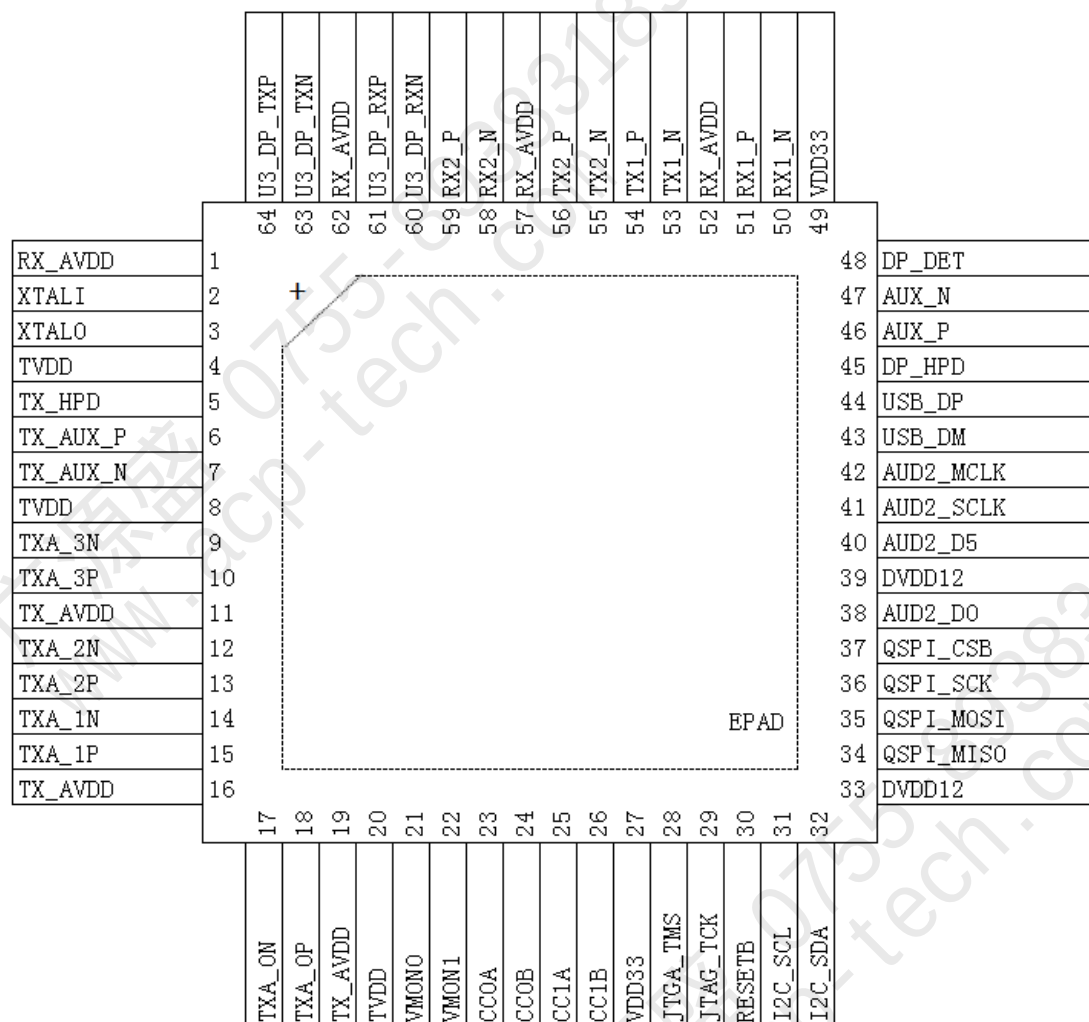


Figure 2. GSV6155 QFN64 Pin Diagram

2.2 QFN64 Pin Description

Table 1. QFN64 Pin Description

Pin Name	Direction	Pin No.	Description
Type-C UFP/DisplayPort RX Pins			
DP_DET	I	48	DP: RX DP Detection PAD
DP_HPD	I/O	45	DP: RX HPD PAD
AUX_P	I/O	46	DP: RX AUX_P PAD
AUX_N	I/O	47	DP: RX AUX_N PAD

RX1_N	I/O	50	DP: RX Negative Main-Link differential data input [0]
RX1_P	I/O	51	DP: RX Positive Main-Link differential data input [0]
TX1_N	I/O	53	DP: RX Negative Main-Link differential data input [1]
TX1_P	I/O	54	DP: RX Positive Main-Link differential data input [1]
TX2_N	I/O	55	DP: RX Negative Main-Link differential data input [2]
TX2_P	I/O	56	DP: RX Positive Main-Link differential data input [2]
RX2_N	I/O	58	DP: RX Negative Main-Link differential data input [3]
RX2_P	I/O	59	DP: RX Positive Main-Link differential data input [3]
Type-C DFP USB 3.0 Pins			
U3_DP_RXN	I/O	60	Type-C USB 3.0 DFP RX1N in "D" Pin-assignment
U3_DP_RXP	I/O	61	Type-C USB 3.0 DFP RX1P in "D" Pin-assignment
U3_DP_TXN	I/O	63	Type-C USB 3.0 DFP TX1N in "D" Pin-assignment
U3_DP_TXP	I/O	64	Type-C USB 3.0 DFP TX1P in "D" Pin-assignment
Type-C DFP/DisplayPort TX Pins			
TX_AUX_P	I/O	6	DP: TXA AUX_P PAD
TX_AUX_N	O	7	DP: TXA AUX_N PAD
TX_HPD	I	5	DP: TXA HPD PAD
TX_0N	I/O	17	DP: TXA Negative Main-Link differential data output [0]
TX_0P	I/O	18	DP: TXA Positive Main-Link differential data output [0]
TX_1N	I/O	14	DP: TXA Negative Main-Link differential data output [1]
TX_1P	I/O	15	DP: TXA Positive Main-Link differential data output [1]
TX_2N	I/O	12	DP: TXA Negative Main-Link differential data output [2]
TX_2P	I/O	13	DP: TXA Positive Main-Link differential data output [2]
TX_3N	I/O	9	DP: TXA Negative Main-Link differential data output [3]
TX_3P	I/O	10	DP: TXA Positive Main-Link differential data output [3]
Power/Ground Pins			
DVDD12	Power	33,39,	Digital 1.2V voltage power supply
VDD33	Power	27,49,	Analog/Digital 3.3V voltage power supply
TVDD	Power	4,8,20,	Analog 3.3V voltage power supply for TX Port
RX_AVDD	Power	1,52, 57,62,	Analog 1.2V voltage power supply for RX Port
TX_AVDD	Power	11,16, 19,	Analog 1.2V voltage power supply for TX Port
Digital pins			
I2C_SDA	I/O	32	Default: Digital IO for I2C Data Alternate: GPIO8 for internal MCU

I2C_SCL	I/O	31	Default: Digital IO for I2C Clock Alternate: GPIO9 for internal MCU
AUD_SCLK	I/O	41	Digital IO PAD Alternate 1: GPIO5 for internal MCU control Alternate 2: EP_SCK for internal MCU SPI control Alternate 3: ADV_TIM2 for internal MCU control
AUD_MCLK	I/O	42	Digital IO PAD Alternate 1: GPIO4 for internal MCU control Alternate 2: EP_CSB for internal MCU SPI control Alternate 3: ADV_TIM1 for internal MCU control
AUD_D0	I/O	38	Digital IO PAD Alternate 1: GPIO7 for internal MCU control Alternate 2: EP_MISO for internal MCU SPI control Alternate 3: UART_TX for internal MCU control
AUD_D5	I/O	40	Digital IO PAD Alternate 1: GPIO6 for internal MCU control Alternate 2: EP_MOSI for internal MCU SPI control Alternate 3: UART_RX for internal MCU control Alternate 4: CEC
RESETB	I	30	Reset Pin. Low for reset state, High for functional state.
XTALI	I/O	2	25M Crystal Input
XTALO	I/O	3	25M Crystal output
JTAG_TMS	I/O	28	Default: TMS, Internal MCU programming pin Alternate: General Interrupt Output Pin
JTAG_TCK	I	29	Default: TCK, Internal MCU programming pin Alternate: AVMUTE Interrupt Output Pin
QSPI_SCK	I/O	36	QSPI_SCK for QSPI Flash connection
QSPI_CSB	I/O	37	QSPI_CSB for QSPI Flash connection
QSPI_MISO	I/O	34	QSPI_MISO for QSPI Flash connection
QSPI_MOSI	I/O	35	QSPI_MOSI for QSPI Flash connection
VMON0	I/O	21	VBus0 Monitor Pin
VMON1	I/O	22	VBus1 Monitor Pin
CC0A	I/O	23	Type-C CC0 Pin1
CC0B	I/O	24	Type-C CC0 Pin2
CC1A	I/O	25	Type-C CC1 Pin1
CC1B	I/O	26	Type-C CC1 Pin2
USB_DP	I/O	44	USB 2.0 D+ Pin

USB_DM	I/O	43	USB 2.0 D- Pin
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3. Electrical Specifications

3.1 Timing Information

3.1.1 Power Up and Reset Timing Diagrams

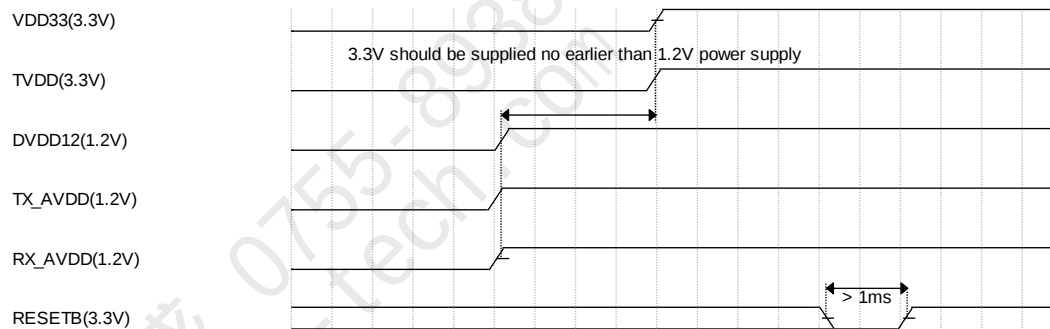


Figure 3. Power Up Sequence

3.1.2 I2C Timing Diagrams

The I2C bus uses 8-bit page address and 16-bit register address. ACK should be provided per 8-bit transaction. For every register, 8-bit data will be accessed. The device address is 0xB0 in 8-bit.

The I2C write timing is shown below.

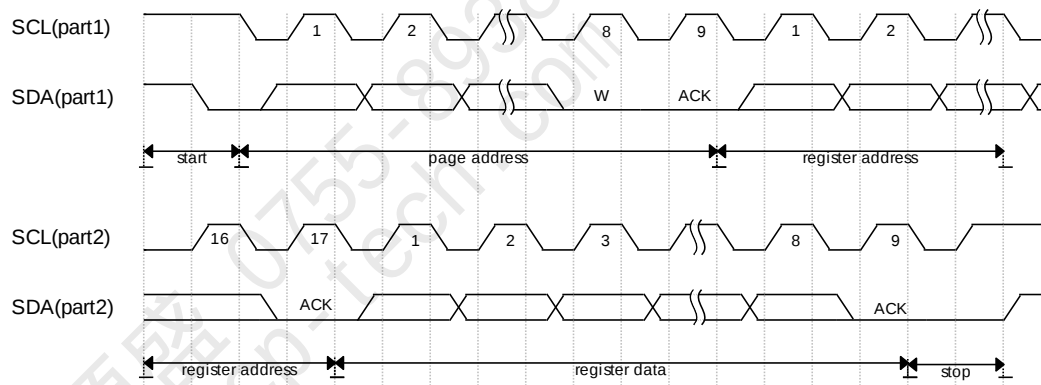


Figure 4. I2C Timing Diagram(Write)

The I2C read timing is shown below.

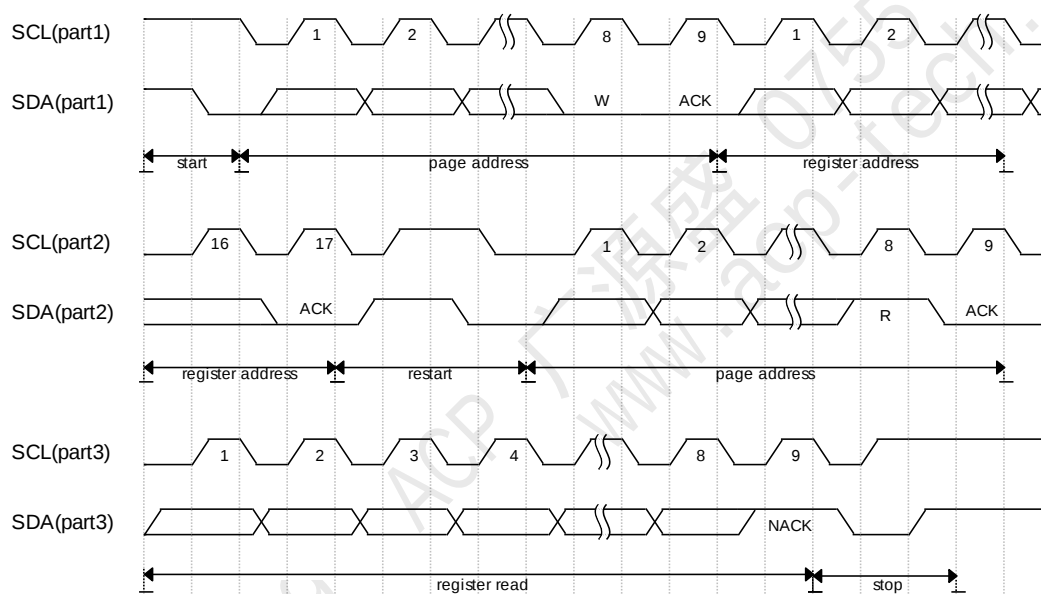


Figure 5. I2C Timing Diagram(Read)

3.2 Operating Conditions

3.2.1 Temperature Conditions

GSV6155's operation temperature range is -45 °C to 85 °C. The maximum junction temperature is at 125 °C.

3.2.2 I2C Conditions

GSV6155's I2C maximum SCL frequency is 400KHz.

4. Package Information

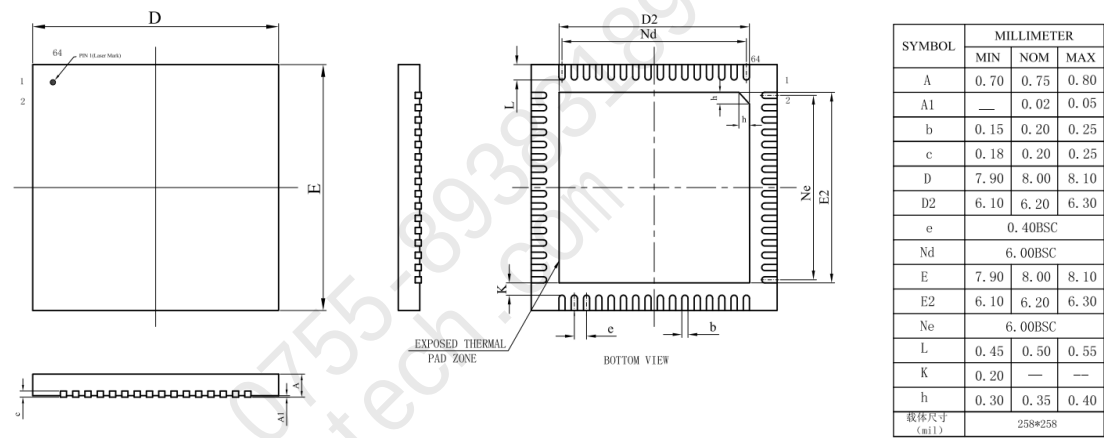


Figure 6. Package Dimensions (QFN64)

5. Ordering Guide

Table 2. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV6155	-45°C to +85°C	QFN64	Tray

6. Revision History

Table 3. Revision history

Revision No.	Description	Date
V0.1	Draft Initial Version for internal review.	Feb 20, 2024

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