



## Descriptions

TS5MP646NYFPR is a high performance four-data lane MIPI, DPHYswitch. This single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources. The TS5MP646NYFPR has wide bandwidth and maintains good signal integrity, which makes it ideal for design for the MIPI specification and allows connection to a CSI or DSI module. 36-Ball Wafer Level Chip Scale Package (WLCSP) 2.4mm x 2.4mm with Pb-free and Halogen-free, makes it ideal for mobile device.

## Order Information

Package	Part Number	Top-Side Marking
CSP-36(DSBGA-36)	Tape and Reel	TS5MP646NYFPR

## Features

- Pin-to-Pin FSA646, CSP-36(DSBGA-36)
- Wide VCC Supply Range: 1.65v~5.5v
- Low Quiescent Current: 35uA Typical
- Insertion loss: -1dB@1GHz, -2dB@1.5GHz, -3dB@5.1GHz
- Channel-to-Channel Cross-talk: -30dB Typical
- Power-off Truly Isolated and Off-Isolation: -25dB Typical

## Applications

- Laptop, Multi-Camera and Displays, 4G/5G Smart Phone, Mobile and AI Device



## Functional Diagram

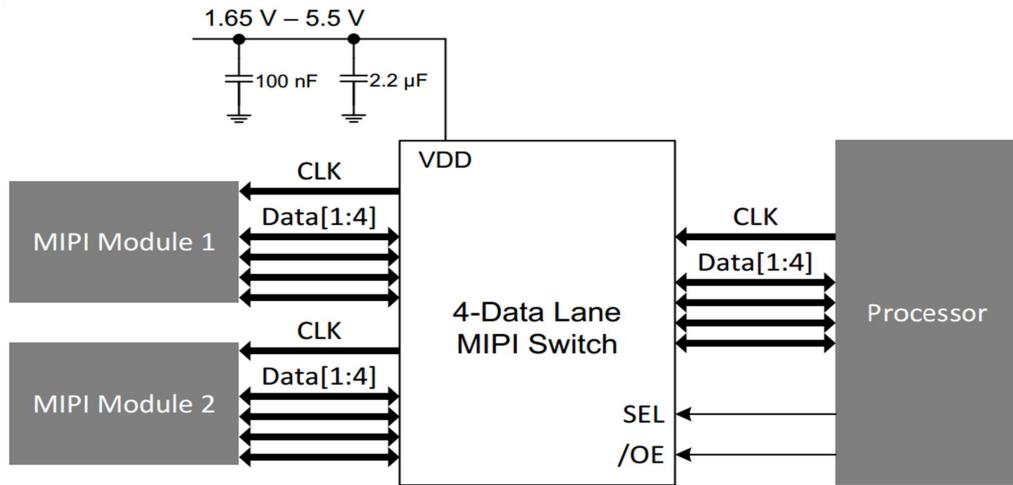


Fig.1 Functional Diagram

## Pin Configuration

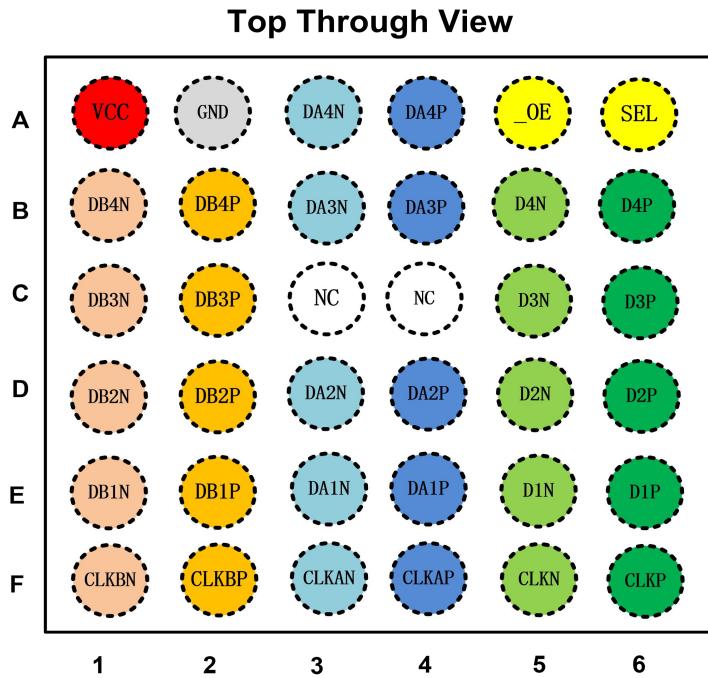


Fig.2 Top-Through View and Top-Side View



### Pin Descriptions

Pin #	Name	Type	Description
A1	VCC	PWR	1.5~5V Positive Supply
A2	GND	GND	Primary Ground Connection. Must be Connected to System Ground
A3	DA4N	I/O	A Side Data Path 4 Negative
A4	DA4P	I/O	A Side Data Path 4 Positive
A5	_OE	I	Chip Enable, Low Active
A6	SEL	I	Channel Selection. When Low, A side selected; When High, B side selected
B1	DB4N	I/O	B Side Data Path 4 Negative
B2	DB4P	I/O	B Side Data Path 4 Positive
B3	DA3N	I/O	A Side Data Path 3 Negative
B4	DA3P	I/O	A Side Data Path 3 Positive
B5	D4N	I/O	Common Side Data Path 4 Negative
B6	D4P	I/O	Common Side Data Path 4 Positive
C1	DB3N	I/O	B Side Data Path 3 Negative
C2	DB3P	I/O	B Side Data Path 3 Positive
C3	NC	O	Not Connected
C4	NC	O	Not Connected
C5	D3N	I/O	Common Side Data Path 3 Negative
C6	D3P	I/O	Common Side Data Path 3 Positive
D1	DB2N	I/O	B Side Data Path 2 Negative
D2	DB2P	I/O	B Side Data Path 2 Positive
D3	DA2N	I/O	A Side Data Path 2 Negative
D4	DA2P	I/O	A Side Data Path 2 Positive
D5	D2N	I/O	Common Side Data Path 2 Negative
D6	D2P	I/O	Common Side Data Path 2 Positive
E1	DB1N	I/O	B Side Data Path 1 Negative
E2	DB1P	I/O	B Side Data Path 1 Positive
E3	DA1N	I/O	A Side Data Path 1 Negative
E4	DA1P	I/O	A Side Data Path 1 Positive
E5	D1N	I/O	Common Side Data Path 1 Negative
E6	D1P	I/O	Common Side Data Path 1 Positive
F1	CLKBN	I/O	B Side Clock Path Negative
F2	CLKBP	I/O	B Side Clock Path Positive
F3	CLKAN	I/O	A Side Clock Path Negative
F4	CLKAP	I/O	A Side Clock Path Positive
F5	CLKN	I/O	Common Side Clock Path Negative
F6	CLKP	I/O	Common Side Clock Path Positive

Table-1 Pin Descriptions



**Absolute Maximum Ratings** over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		<b>Range</b>	<b>Unit</b>
Power Supply Voltage	VCC	-0.5 ~ 6.0	V
Control Pins	_OE, SEL	-0.5 ~ VCC	V
DC Switch I/O Voltage	V <sub>SW</sub>	-0.3 ~ VCC	V
DC I/O Current	I <sub>IK</sub>	-50 ~ 50	mA
Storage Temperature Range	T <sub>STG</sub>	-55 ~ 150	°C
ESD HBM, ANSI/ESDA/JEDEC JS-001-2012	VCC	±2	kV
	_OE, SEL	±2	kV
	Other I/O Pins	±2	kV
ESD MM, JESD22-A115	VCC	±200	V
	_OE, SEL	±2	kV
	Other I/O Pins	±2	kV

**Table-2 Absolute Maximum Ratings**

(1) Stresses beyond those listed in Table-2 *Absolute Maximum Ratings* may cause permanent damage to the device. They are stress ratings only, which do not imply functional operation of the device at these or any other conditions. Beyond those indicated under *Recommended Operating Conditions*, exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### Recommend Operating Conditions

		<b>Range</b>	<b>Unit</b>
Power Supply Voltage	VCC	1.65 ~ 5.5	V
Control Pins	_OE, SEL	0 ~ VCC	V
Signal Pins	HS Mode	0 ~ 0.3	V
	LP Mode	0 ~ 1.3	V
Operating Temperature	T <sub>A</sub>	-40 ~ 85	°C

**Table-3 Recommend Operating Conditions**

(1) If \_OE is left undriven, it will be pulled up to VCC by internal resistor; If SEL is left undriven, it will be pulled down to Ground by internal resistor.



**Electrical Characteristics (Ta=25°C, VCC=1.8V, unless otherwise specified)**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>Power Supply</b>						
VCC Quiescent Current	I <sub>Q</sub>	SEL=0 or VCC, _OE=0		30		uA
Power-down Current	I <sub>PD</sub>	SEL=0 or VCC, _OE=VCC			1	uA
<b>DC Characteristics</b>						
Input logic high	V <sub>IH</sub>	VCC=1.8~4.5V	1.6			V
Input logic low	V <sub>IL</sub>	VCC=1.8~4.5V			0.4	V
_OE Internal pull-up resistor	R <sub>UP</sub>			2		MΩ
SEL Internal pull-down resistor	R <sub>DN</sub>			2		MΩ
On-Resistance for LP MIPI	R <sub>ON_LP</sub>	V <sub>IS</sub> = 1.2V I <sub>ON</sub> =8mA		4.8	10	Ω
On-Resistance for HS MIPI	R <sub>ON_HS</sub>	V <sub>IS</sub> = 0.2V I <sub>ON</sub> =8mA		4.3	9	Ω
R <sub>ON</sub> Flatness for LP MIPI	R <sub>FLAT_LP</sub>	V <sub>IS</sub> = 0 to 1.2V I <sub>ON</sub> =8mA		0.9		Ω
R <sub>ON</sub> Flatness for HS MIPI	R <sub>FLAT_HS</sub>	V <sub>IS</sub> = 0 to 0.2V I <sub>ON</sub> =8mA		0.2		Ω
R <sub>ON</sub> Matching Between Channels	R <sub>MATCH</sub>	V <sub>IS</sub> = 0 to 1.2V I <sub>ON</sub> =8mA		0.1		Ω
Switch Off Leakage Current	I <sub>OFF</sub>	_OE=VCC Dn, Dp =VCC DAn, DBn, DAp, DBp=0 CLKn, CLKp=0 CLKAn, CLKBn, CLKAp, CLKBp=VCC	-0.5		0.5	uA
<b>AC Characteristics</b>						
Enable Time _OE to Output	t <sub>EN</sub>	R <sub>L</sub> =50Ω C <sub>L</sub> =0pF V <sub>IS</sub> = 0.6V		80	150	uS
Disable Time _OE to Output	t <sub>DIS</sub>	R <sub>L</sub> =50Ω C <sub>L</sub> =0pF V <sub>IS</sub> = 0.6V		40	250	nS
Turn-On Time SEL to Output	t <sub>ON</sub>	R <sub>L</sub> =50Ω C <sub>L</sub> =0pF V <sub>IS</sub> = 0.6V		400	1200	nS
Turn-Off Time SEL to Output	t <sub>OFF</sub>	R <sub>L</sub> =50Ω C <sub>L</sub> =0pF V <sub>IS</sub> = 0.6V		130	800	nS
Break-Before-Make Time	t <sub>BBM</sub>	R <sub>L</sub> =50Ω C <sub>L</sub> =0pF V <sub>IS</sub> = 0.6V		250	500	nS
Propagation Delay	t <sub>PD</sub>	R <sub>L</sub> =50Ω C <sub>L</sub> =0pF V <sub>IS</sub> = 0.6V		0.25		nS
HS Mode Skew of Opposite Transitions of the Same Output	t <sub>SK(P)</sub>	R <sub>L</sub> =50Ω C <sub>L</sub> =0pF V <sub>IS</sub> = 0.3V		6		pS
HS Mode Skew of Channel-to-Channel Single-Ended Skew	t <sub>SK(O)</sub>	R <sub>L</sub> =50Ω C <sub>L</sub> =0pF V <sub>IS</sub> = 0.3V		6		pS
Off Isolation	Off	R <sub>L</sub> = 50Ω f = 1.2GHz V <sub>IS</sub> = 0.2V <sub>PP</sub>		-25		dB
Crosstalk (Channel-to-Channel)	X <sub>TALK</sub>	R <sub>L</sub> = 50Ω f = 1.2GHz V <sub>IS</sub> = 0.2V <sub>PP</sub>		-30		dB
-3dB Bandwidth (Insertion Loss)	BW <sub>-3dB</sub>	R <sub>L</sub> =50Ω C <sub>L</sub> =0pF Signal 0dBm		5.1		GHz



<b>Capacitance</b>						
Switch On Capacitance	$C_{ON}$	$V_{Bias} = 0.2V, f = 1250MHz$			1.5	pF
Switch Off Capacitance	$C_{OFF}$	$V_{Bias} = 0.2V, f = 1250MHz$			1.0	pF

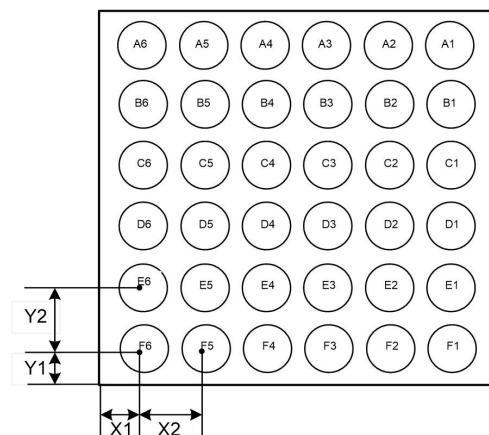
**Table-4 Electrical Characteristics**

**Note:**

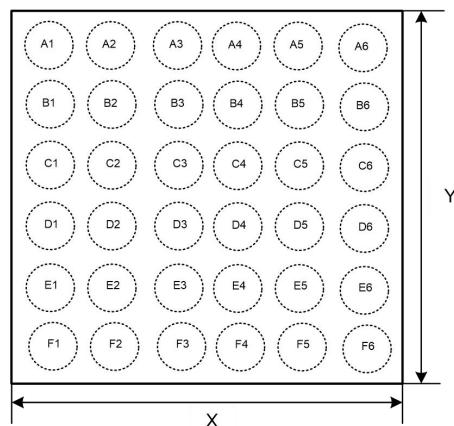
- (1) Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.
- (2) Crosstalk is inversely proportional to source impedance

**Package Outline Dimensions**

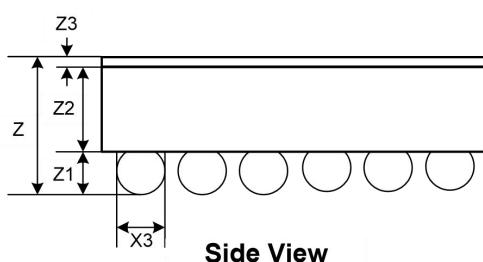
**CSP-36(DSBGA-36)**



**Bottom-Up View**



**Top-Through View**



**Side View**

**Fig.3 Package Outline Dimensions**

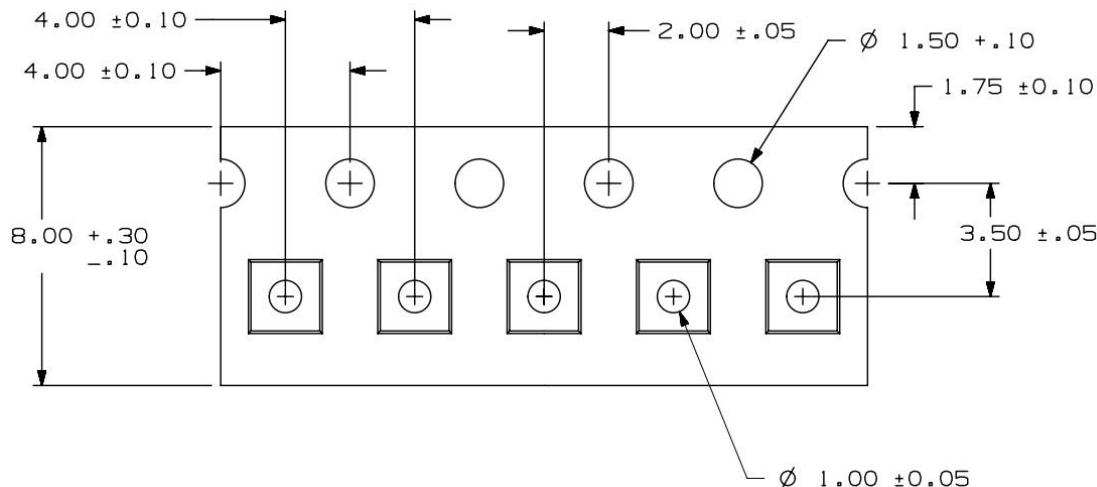


Symbol	Dimensions In Millimeter		
	Min.	Typ.	Max.
X	2.37	2.40	2.43
Y	2.37	2.40	2.43
X1		0.16	
X2		0.40	
X3	0.175	0.205	0.235
Y1		0.16	
Y2		0.40	
Z	0.550	0.600	0.650
Z1	0.145	0.170	0.195
Z2	0.340	0.365	0.390
Z3	0.395	0.040	0.045

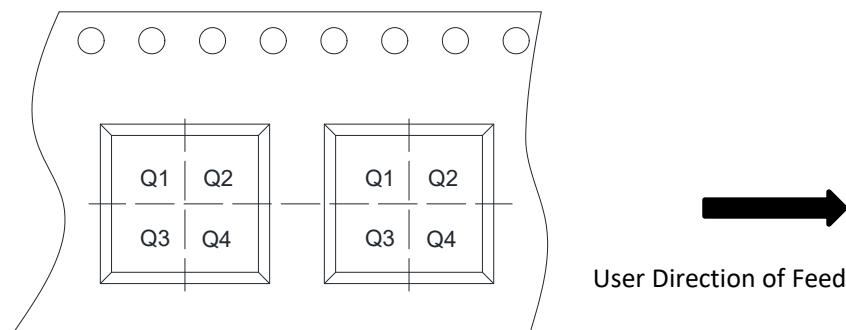
Table-5 Package Outline Dimensions



### Tape and Reel Information



### Quadrant Assignments for PIN 1 Orientation In Tape



Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2	<input type="checkbox"/> Q3	<input type="checkbox"/> Q4
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Fig.4 Tape and Reel Information



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