1. DESCRIPTION

The 74HC4514 is a 4-to-16 line decoder/demultiplexer having four binary weighted address inputs (A0 to A3), with latches, a latch enable input (LE), an enable input (E) and 16 outputs (Q0 to Q15). When LE is HIGH, the selected output is determined by the data on An. When LE goes LOW, the last data present at An are stored in the latches and the outputs remain stable. When E is LOW, the selected output, determined by the contents of the latch, is HIGH. At E HIGH, all outputs are LOW. The enable input E does not affect the state of the latch. When the device is used as a demultiplexer, E is the data input and A0 to A3 are the address inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. FEATURES

- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Input levels: CMOS level
- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into 16 mutually-exclusive outputs
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
  -JESD8C (2.7 V to 3.6 V)
  -JESD7A (2.0 V to 6.0 V)

3. APPLICATIONS

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding

4. FUNCTIONAL DIAGRAM

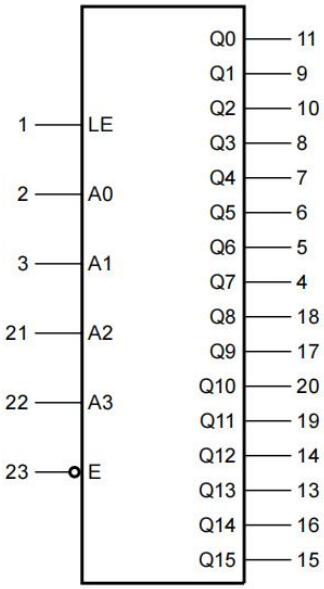


Fig. 1. Logic symbol

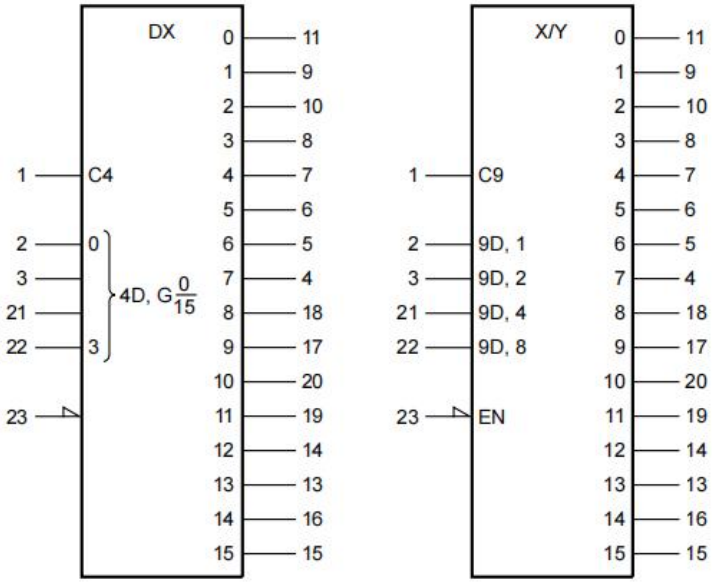


Fig. 2. IEC logic symbol

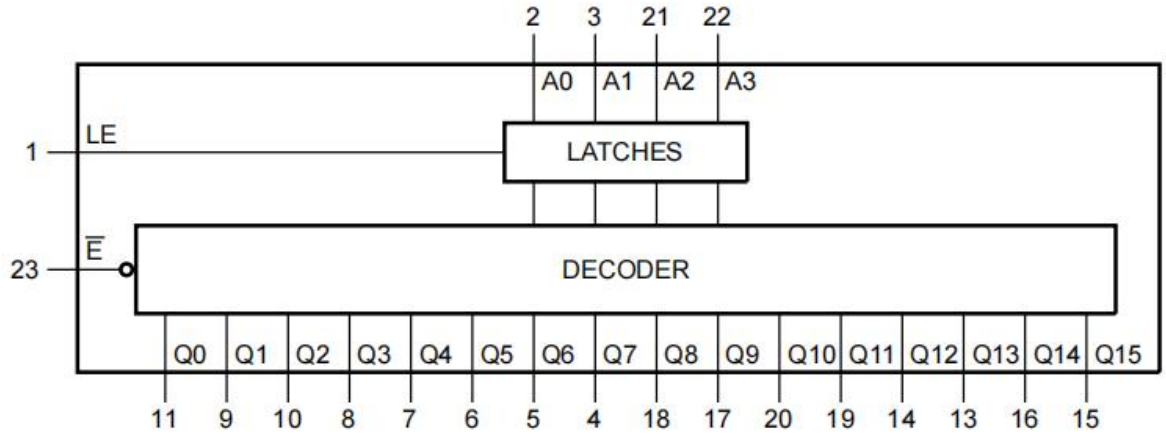


Fig. 3. Functional diagram

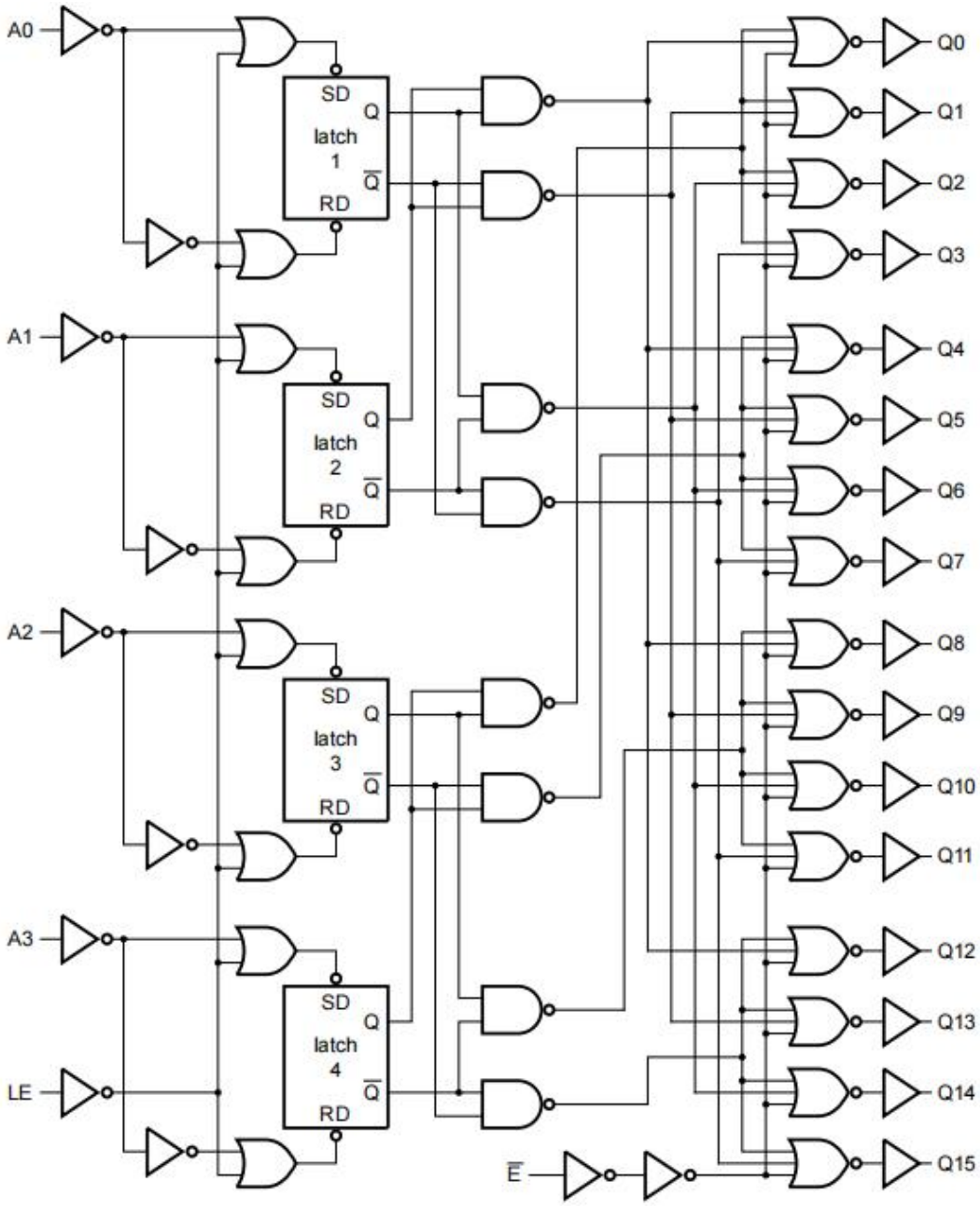
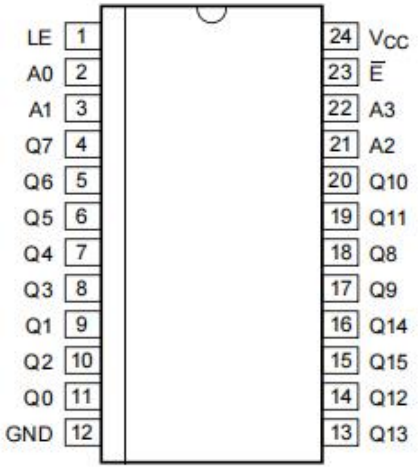


Fig. 4. Logic diagram

5. PINNING INFORMATION

SOP24



TSSOP24

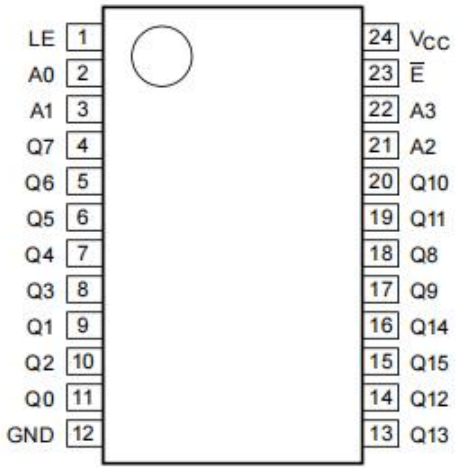


Table 1. Pin description

Symbol	Pin	Description
LE	1	latch enable input (active HIGH)
$\overline{E}$	23	enable input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15	11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	multiplexer outputs (active HIGH)
A0, A1, A2, A3	2, 3, 21, 22	address inputs
GND	12	ground (0 V)
VCC	24	supply voltage

6. FUNCTIONAL DESCRIPTION

Table 2. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.
Input LE = HIGH.

Inputs					Outputs															
E	A0	A1	A2	A3	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12	Q13	Q14	Q15
H	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

7. LIMITING VALUES

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	—	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	—	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	—	±25	mA
I_{CC}	supply current		—	50	mA
I_{GND}	ground current		-50	—	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	Note1	—	500	mW

Note：1.For SO24 package: Ptot derates linearly with 16.2 mW/K above 119 °C.
For TSSOP24 package: Ptot derates linearly with 12.4 mW/K above 110 °C.

8. RECOMMENDED OPERATING CONDITIONS

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	—	V_{CC}	V
V_O	output voltage		0	—	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	—	—	625	ns/V
		V_{CC} = 4.5 V	—	1.67	139	ns/V
		V_{CC} = 6.0 V	—	—	83	ns/V
T_{amb}	ambient temperature		-40	—	+85	°C

9. STATIC CHARACTERISTICS

Table 5. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	+25°C			-40°C to 85°C		Unit
			Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	—	1.5	—	V
		Vcc=4.5V	3.15	2.4	—	3.15	—	V
		Vcc=6.0 V	4.2	3.2	—	4.2	—	V
V_{IL}	LOW-level input voltage	Vcc=2.0 V	—	0.8	0.5	—	0.5	V
		Vcc=4.5V	—	2.1	1.35	—	1.35	V
		Vcc = 6.0 V	—	2.8	1.8	—	1.8	V
V_{OH}	HIGH level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	2.0	—	1.9	—	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	4.5	—	4.4	—	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.9	6.0	—	5.9	—	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	—	3.84	—	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	—	5.34	—	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20 μA; V_{CC} = 2.0 V	—	0	0.1	—	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	—	0	0.1	—	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	—	0	0.1	—	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	—	0.15	0.26	—	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	—	0.16	0.26	—	0.33	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	—	—	±0.1	—	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	—	—	8.0	—	80	μA
C_I	input capacitance		—	3.5	—	—	—	pF

10. DYNAMIC CHARACTERISTICS

Table 6. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 7.

Symbol	Parameter	Conditions	+25°C			-40°C to 85°C		Unit
			Min	Typ	Max	Min	Max	
t_{pd}	propagation delay	An to Qn; see Fig. 5-NOTE1						
		V_{CC} = 2.0 V	—	74	230	—	290	ns
		V_{CC} = 4.5 V	—	27	46	—	58	ns
		V_{CC} = 5 V; C_L = 15 pF	—	23	—	—	—	ns
		V_{CC} = 6.0 V	—	22	39	—	49	ns
		LE to Qn; see Fig. 5						
		V_{CC} = 2.0 V	—	74	230	—	290	ns
		V_{CC} = 4.5 V	—	27	46	—	58	ns
		V_{CC} = 6.0 V	—	22	39	—	49	ns
		E to Qn; see Fig. 5						
		V_{CC} = 2.0 V	—	41	175	—	220	ns
		V_{CC} = 4.5 V	—	15	35	—	44	ns
		V_{CC} = 6.0 V	—	12	30	—	37	ns
t_t	transition time	Qn; see Fig. 5-NOTE2						
		V_{CC} = 2.0 V	—	19	75	—	95	ns
		V_{CC} = 4.5 V	—	7	15	—	19	ns
		V_{CC} = 6.0 V	—	6	13	—	16	ns
t_W	pulse witdh	LE HIGH; see Fig. 6						
		V_{CC} = 2.0 V	80	14	—	100	—	ns
		V_{CC} = 4.5 V	16	5	—	20	—	ns
		V_{CC} = 6.0 V	14	4	—	17	—	ns
t_{su}	set-up time	An to LE; see Fig. 6						
		V_{CC} = 2.0 V	90	25	—	115	—	ns
		V_{CC} = 4.5 V	18	9	—	23	—	ns
		V_{CC} = 6.0 V	15	7	—	20	—	ns
t_n	hold time	An to LE; see Fig. 6						
		V_{CC} = 2.0 V	1	-11	—	1	—	ns
		V_{CC} = 4.5 V	1	-4	—	1	—	ns
		V_{CC} = 6.0 V	1	-3	—	1	—	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC}-NOTE3	—	44	—	—	—	pF

NOTE: 1.t_{pd} is the same as t_{PLH} and t_{PHL}

2.tt is the same as tTLH and tTHL

3.C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}\ 2 \times f_i \times N + \Sigma(C_L \times V_{CC}{}^2 \times fo)$ where:

f_i = input frequency in MHz;

f_O = output frequency in MHz;

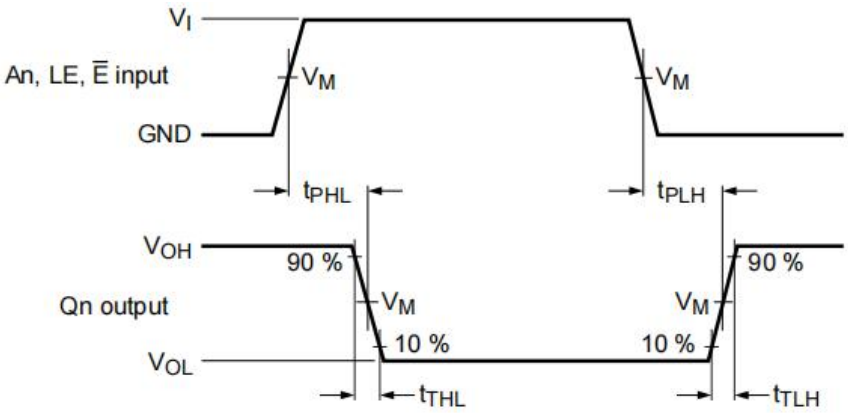
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of load switching outputs;

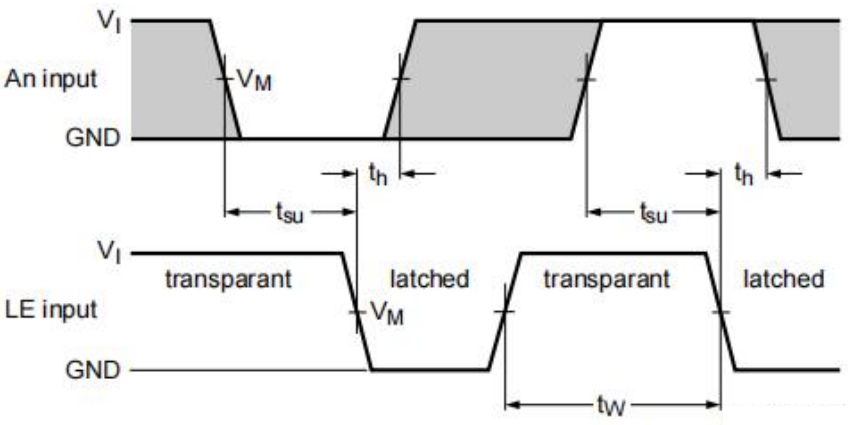
$\Sigma(C_L \times V_{CC}{}^2 \times f_O)$ = sum of the outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 7.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The inputs (An, LE, E) to output (Qn) propagation delays and the output transition times

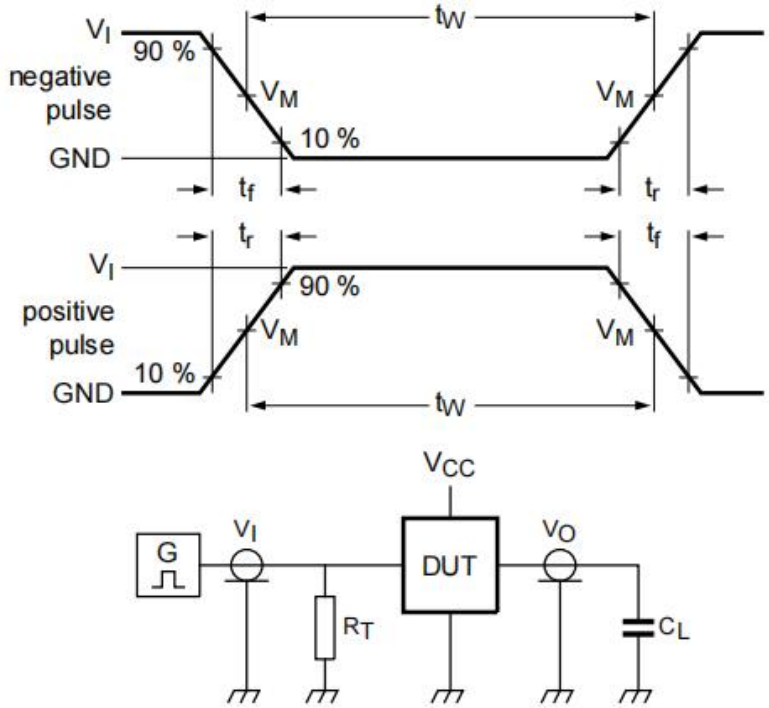


Measurement points are given in Table 7.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6. Data set-up and hold times for An input to LE input and LE input pulse width

Table 7. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC4514	GND to V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 8.
Definitions for test circuit:
RT = Termination resistance; should be equal to output impedance Zo of the pulse generator;
CL = Load capacitance including jig and probe capacitance

Fig. 7. Test circuit for measuring switching times

Table 8. Test data

Type	Input		Load
	V_I	tr,tf	CL
74HC4514	GND to V_{CC}	6ns	15pF,50pF

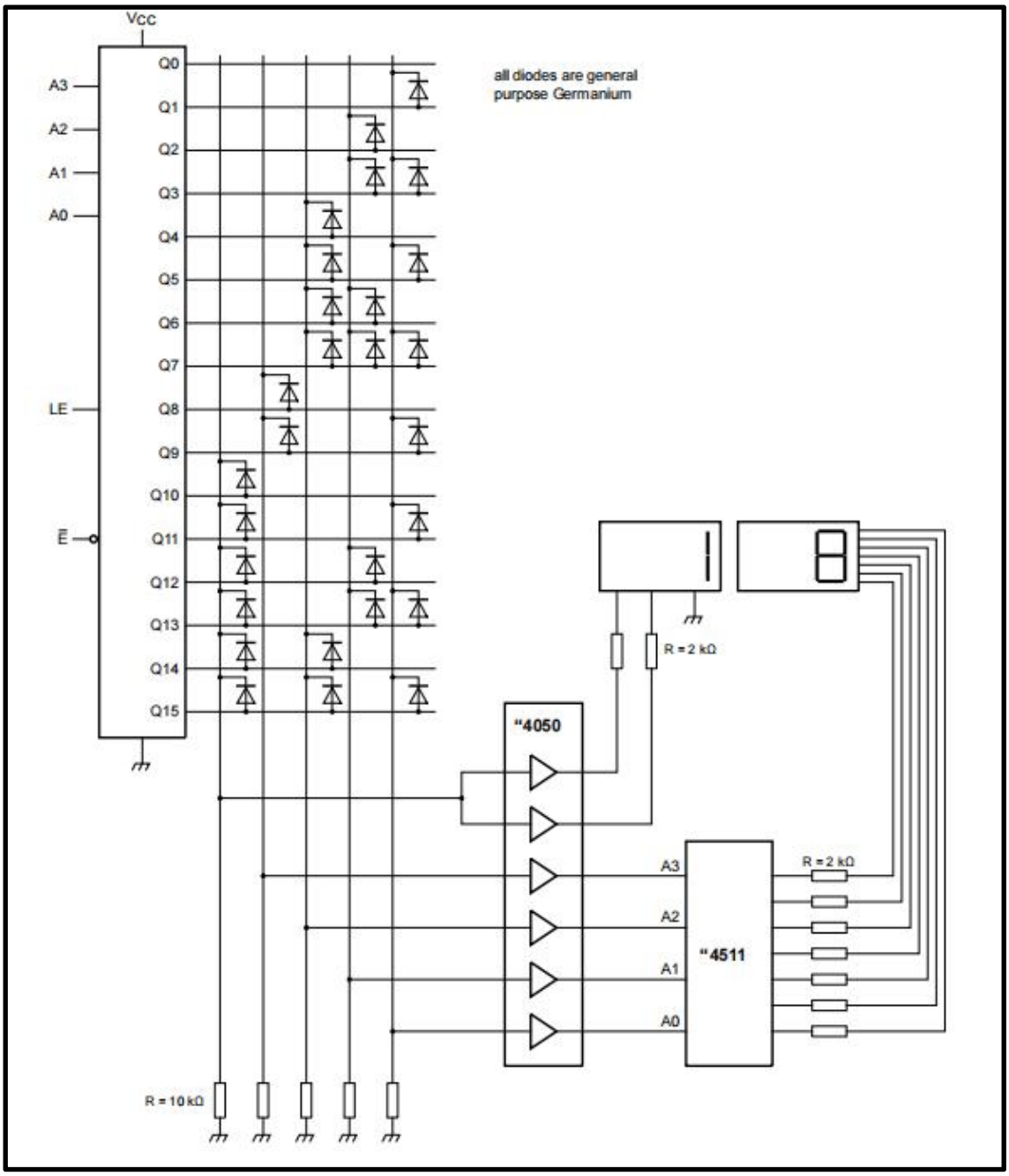


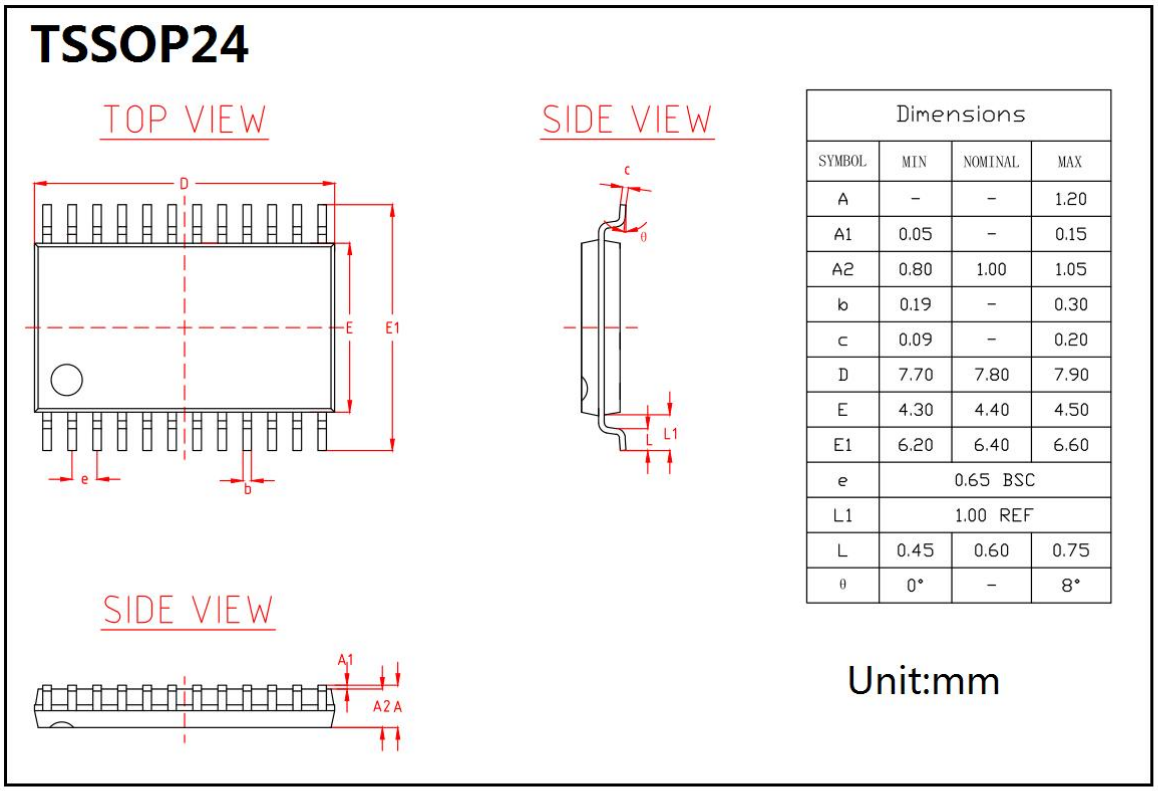
Fig. 8. Code-to-code conversion; hexadecimal to BCD

11. ORDERING INFORMATION

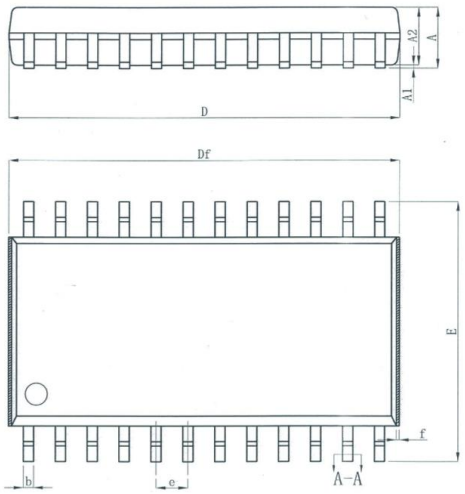
Ordering Information

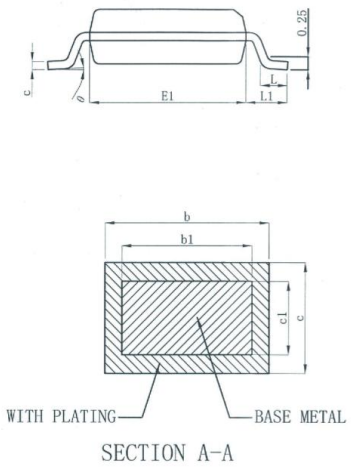
Part Number	Device Making	Package type	Body size (mm)	Temperate (℃)	MSL	Transpo Rt	Package Quantit
XL74HC4514D	XL4514D	SOP24	15.29 *7.50	-40 to +85	MSL3	T&R	2000
XL74HC4514PW	XL4514	TSSOP24	7.80*4.40	-40 to +85	MSL3	T&R	2500

12. DIMENSIONAL DRAWINGS



SOP24





symbol	millimeter		
	Min	Nom	Max
A	2.47	2.52	2.57
A1	0.10	0.15	0.20
A2	2.24	2.34	2.44
b	0.39	---	0.47
b1	0.38	0.41	0.43
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	15.19	15.29	15.39
Df	15.29	---	15.79
E	10.25	10.30	10.35
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.76	0.86	0.96
L1	1.30	1.40	1.50
θ	0°	---	8°
f	0.05	---	0.20