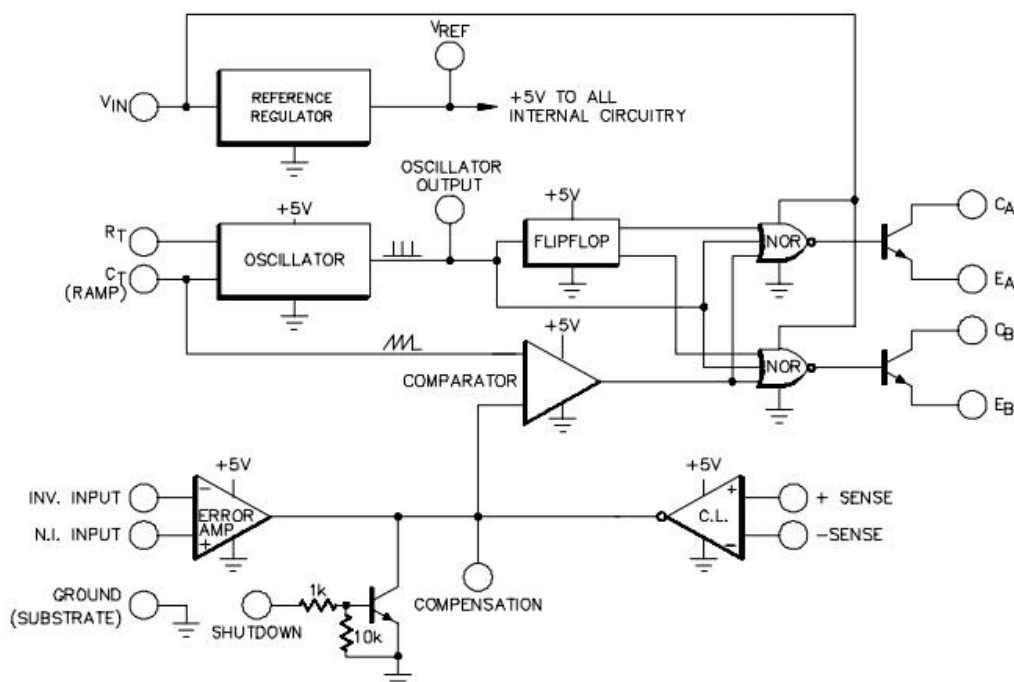


1. DESCRIPTION

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches, and current-limiting and shutdown circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformer-less voltage doublers, and polarity converters, as well as other power applications.

2. FEATURES

- 8V to 40V operation
- 5V reference
- Reference line and load regulation of 0.4%
- 100 Hz to 300 kHz oscillator range
- Excellent external sync capability
- Dual 50 mA output transistors
- Current limit circuitry
- Complete PwM power control circuitry
- Single-ended or push-pull outputs
- Total supply current less than 10 mA



3. ABSOLUTE MAXIMUM RATINGS

 Table 1-1. Absolute Maximum Ratings¹

Parameter	Value	Units
Input voltage (+V _{IN})	42	V
Collector voltage	40	V
Logic inputs	−0.3 to 5.5	V
Current limit sense inputs	−0.3 to 0.3	V
Output current (each transistor)	100	mA
Reference load current	50	mA
Oscillator charging current	5	mA
Operating Junction Temperature		
Hermetic (J, L packages)	150	°C
Plastic (N, D packages)	150	°C
Storage temperature range	−65 to 150	°C
Lead temperature (soldering, 10 seconds) ²	300	°C

Notes:

1. Values beyond which damage may occur
2. Pb-free/RoHS peak package solder reflow temp. (40 sec. max. exposure) 260 °C (+0, −5)

4. THERMAL DATA

 Table 2-1. Thermal Data ⁽¹⁻²⁾

Parameter	Value	Units
J Package		
Thermal resistance-junction to case, θ_{JC}	30	°C/W
Thermal resistance-junction to ambient, θ_{JA}	80	°C/W
N Package		
Thermal resistance-junction to case, θ_{JC}	40	°C/W
Thermal resistance-junction to ambient, θ_{JA}	65	°C/W
DW Package		
Thermal resistance-junction to case, θ_{JC}	50	°C/W
Thermal resistance-junction to ambient, θ_{JA}	120	°C/W
L Package		
Thermal resistance-junction to case, θ_{JC}	35	°C/W
Thermal resistance-junction to ambient, θ_{JA}	120	°C/W

Notes:

1. Junction temperature calculation: $T_J = T_A + (P_D \times \theta_{JA})$
2. The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

5. RECOMMENDED OPERATING CONDITIONS

Table 3-1. Recommended Operating Conditions¹

Parameter	Value	Units
Input voltage (+Vin)	8 to 40	V
Collector voltage	0 to 40	V
Error amp common mode range	1.8 to 3.4	V
Current limit sense common mode range	-0.3 to 0.3	V
Output current (each transistor)	0 to 50	mA
Reference load current	0 to 20	mA
Oscillator charging current	30 μ A to 2 mA	μ A, mA
Oscillator frequency range	100 Hz to 300 kHz	Hz, kHz
Oscillator timing resistor (Rt)	1.8 to 100	k Ω
Oscillator timing capacitor (Ct)	1 nF to 1.0 μ F	nf, μ F
Operating Ambient Temperature Range		
XLSG3524	-25 to 85	$^{\circ}$ C

Note:

1. Range over which the device is functional and parameter limits are guaranteed.

6. Electrical Characteristics

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for XLSG3524 with $0\text{ }^{\circ}\text{C} \leq T_A \leq 70\text{ }^{\circ}\text{C}$, and $+V_{IN} = 20\text{V}$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Table 4-1. Electrical Characteristics

Parameter	Test Conditions	Min	Typ	Max	Units
Reference Section¹					
Output voltage	$T_J = 25^{\circ}\text{C}$	4.60	5.00	5.40	V
Line regulation	$V_{IN} = 8\text{V to } 40\text{V}$	—	—	30	mv
Load regulation	$I_L = 0 \text{ to } 20 \text{ mA}$	—	—	50	mv
Temperature stability ²	Over operating temperature range	—	—	50	mv
Output voltage range ²	Over line, load and temperature	4.60	—	5.40	V
Short circuit current	$V_{REF} = 0\text{V}$	25	50	150	mA
Oscillator Section³					
Initial accuracy	$T_J = 25^{\circ}\text{C}$	36	44	44	kHz
	$\text{Min} \leq T_J \leq \text{Max}$	34	—	46	kHz
Voltage stability	$V_{IN} = 8\text{V to } 40\text{V}$	—	0.1	1	%
Maximum frequency	$R_T = 2 \text{ k}\Omega$, $C_T = 1 \text{ nF}$	200	400	—	kHz
Sawtooth peak voltage	$V_{IN} = 40\text{V}$	3	—	3.8	V
Sawtooth valley voltage	$V_{IN} = 8\text{V}$	0.6	1	1.2	V
Clock amplitude	—	3.2	—	—	V
Clock pulse width	—	0.3	—	1.5	μs
Error Amplifier Section⁴					
Input offset voltage	$R_S \leq 2 \text{ k}\Omega$	—	2	10	mv
Input bias current	—	—	1	10	μA
Input offset current	—	—	—	2	μA
DC open loop gain	$R_L \geq 10 \text{ M}\Omega$, $T_J = 25^{\circ}\text{C}$	60	—	—	dB
Output low level	$V_{PIN1} - V_{PIN2} \geq 150 \text{ mV}$	—	0.2	0.5	V
Output high level	$V_{PIN2} - V_{PIN1} \geq 150 \text{ mV}$	3.8	4.2	—	V
Common mode rejection	$V_{CM} = 1.8\text{V to } 3.4\text{V}$	—	—	—	dB
Supply voltage rejection	$V_{IN} = 8\text{V to } 40\text{V}$	—	—	—	dB
Gain-bandwidth product ²	$T_J = 25^{\circ}\text{C}$	1	2	—	MHz
P.W.M. Comparator³					
Minimum duty cycle	$V_{COMP} = 0.5\text{V}$	—	—	0	%
Maximum duty cycle	$V_{COMP} = 3.6\text{V}$	45	49	—	%
Current Limit Amplifier Section⁵					
Sense voltage	$T_J = 25^{\circ}\text{C}$	180	200	220	mV
Input bias current	—	—	—	200	μA
Shutdown Section					
Threshold voltage	$T_J = 25^{\circ}\text{C}$	0.5	0.8	1.2	V
	$\text{Min} \leq T_J \leq \text{Max}$	0.2	—	1.8	V

Parameter	Test Conditions	Min	Typ	Max	Units
Output Section (Each Transistor)					
Collector leakage current	$V_{CE} = 40V$	—	—	50	μA
Collector saturation voltage	$I_C = 50\text{ mA}$	—	—	2	V
Emitter output voltage	$I_E = 50\text{ mA}$	17	—	—	V
Collector voltage rise time	$R_C = 2\text{ k}\Omega$	—	—	0.4	μs
Collector voltage fall time	$R_C = 2\text{ k}\Omega$	—	—	0.2	μs
Power Consumption					
Standby current	$V_{IN} = 40V$	—	7	10	mA

Notes:

1. $I_L = 0\text{ mA}$
2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
3. $F_{osc} = 40\text{ kHz}$ ($R_T = 2.9\text{ k}\Omega$, $C_T = 0.01\text{ }\mu F$)
4. $V_{CM} = 2.5V$
5. $V_{CM} = 0V$

7. APPLICATION NOTES

7.1. Oscillator

The oscillator in the XLSG3524 uses an external resistor R_T to establish a constant charging current into an external capacitor C_T . While this uses more current than a series-connected RC, it provides a linear ramp voltage at C_T which is used as a time-dependent reference for the PWM comparator. The charging current is equal to $3.6V/R_T$, and should be restricted to between 30 μA and 2 mA. The equivalent range for R_T is 100k to 1.8k.

The range of values for C_T also has limits, as the discharge time of C_T determines the pulse width of the oscillator output pulse. The pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead-time relationship is shown in [Figure 5-1](#). A pulse width below 0.35 microseconds may cause failure of the internal flip-flop to toggle. This restricts the minimum value of C_T to 1000 pF. (Note: Although the oscillator output is a convenient oscilloscope sync input, the probe capacitance will increase the pulse width and decrease the oscillator frequency slightly.) Obviously, the upper limit to the pulse width is determined by the modulation range required in the power supply at the chosen switching frequency. Practical values of C_T fall between 1000 pF and 0.1 μF , although successful 120 Hz oscillators have been implemented with values up to 5 μF and a series surge limit resistor of 100 ohms.

The oscillator frequency is approximately $1/RT \times CT$; where R is in ohms, C is in microfarads, and the frequency is in Megahertz. For greater accuracy, the chart in [Figure 5-2](#) may be used for a wide range of operating frequencies. Note that for buck regulator topologies, the two outputs can be wire-ORed for an effective 0-90% duty cycle range. With this connection, the output frequency is the same as the oscillator frequency. For push-pull applications, the outputs are used separately; the flip-flop limits the duty cycle range at each output to 0-45%, and the effective switching frequency at the transformer is 1/2 the oscillator frequency.

If it is desired to synchronize the XLSG3524 to an external clock, a positive pulse may be applied to the clock pin. The oscillator should be programmed with R_T and C_T values that cause it to free-run at 90% of the external sync frequency. A sync pulse with a maximum logic 0 of +0.3 volts and a minimum logic 1 of +2.4 volts applied to Pin 3 will lock the oscillator to the external source. The minimum sync pulse-width should be 200 nanoseconds, and the maximum is determined by the required dead-time. The clock pin should never be driven more negative than -0.3 volts, nor more positive than +5.0 volts. The nominal resistance to ground is 3.2k at the clock pin, $\pm 25\%$ over temperature.

If two or more XLSG3524 must be synchronized together, program one controller unit with R_T and C_T for the desired frequency. Leave the R_T pins on the target open, connect the C_T pins to the C_T of the controller, and connect the clock pins to the clock pin of the controller. Since C_T is a high-impedance node, this sync technique works best when all devices are close together.

Since the gain of this circuit is relatively low (42 dB), there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage required to get 25% duty cycle (+2 volts at the error amplifier output) with the error amplifier signaling maximum duty cycle.

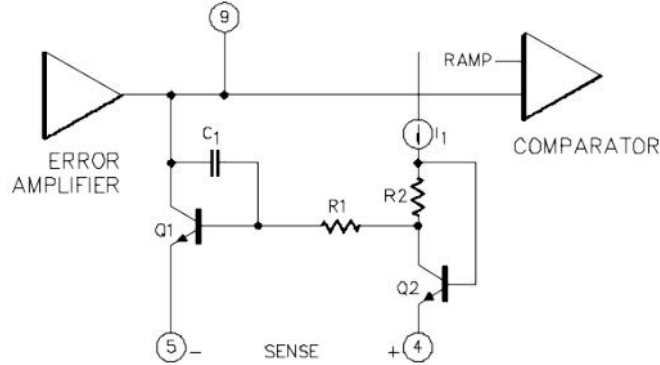
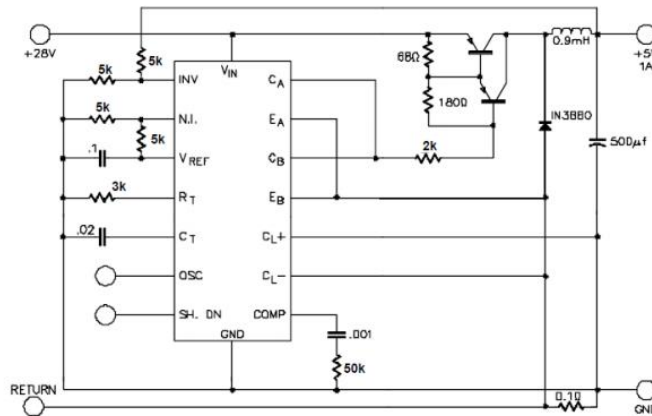
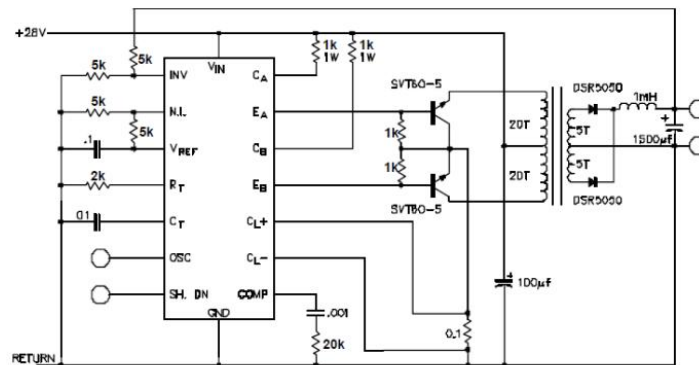


Figure 5-3. Current Limiting Circuitry of the XLSG3524



In this conventional single-ended regulator circuit, the two outputs of the XLSG3524 are connected in parallel for effective 0-90% duty-cycle modulation. The use of an output inductor requires an R-C phase compensation network for loop stability.



Push-pull outputs are used in this transformer-coupled DC-DC regulating converter. Note that the oscillator must be set at twice the desired output frequency as the XLSG3524 internal flip-flop divides the frequency by 2 as it switches the PWM signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

8. ORDERING INFORMATION

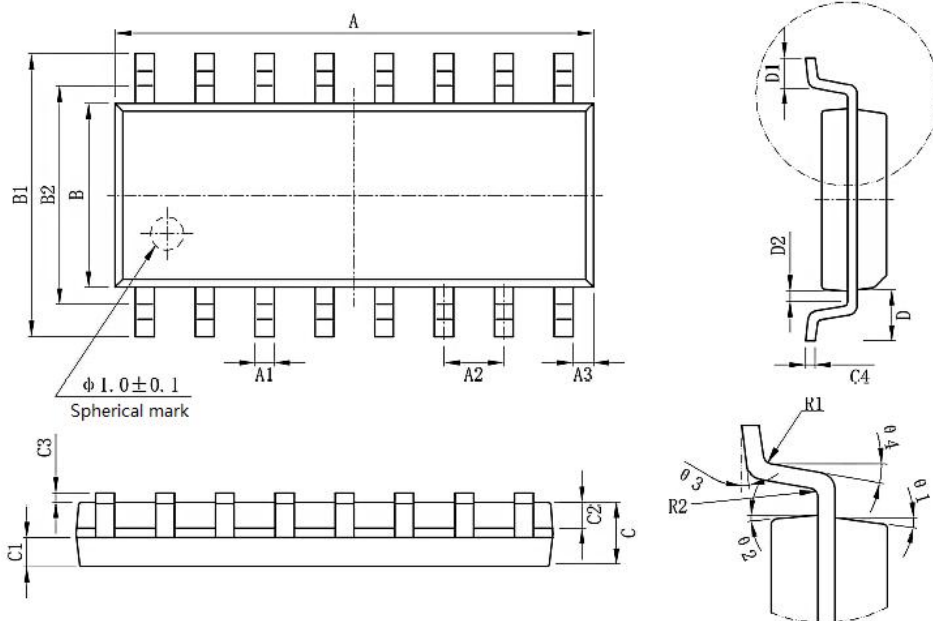
Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperature (°C)	MSL	Transpo Rt	Package Quantit
XLSG3524N	XL3524N	DIP16	19.05*6.35	-25 to +85	MSL3	Tube 25	1000
XLSG3524DR	XL3524D	SOP16	10.00*3.95	-25 to +85	MSL3	T&R	2500

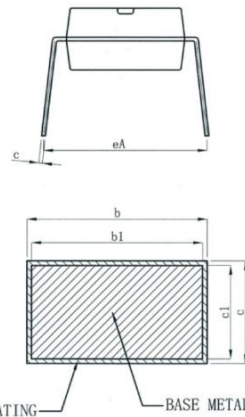
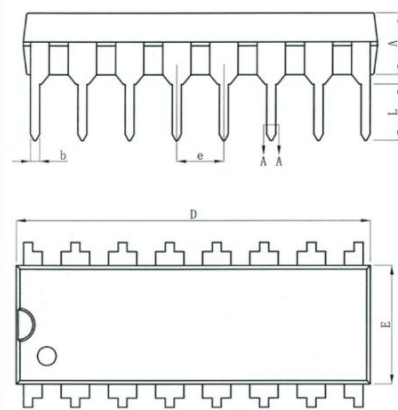
9. DIMENSIONAL DRAWINGS

SOP16

MARK	SYM	MIN (mm)	MAX (mm)	MARK	SYM	MIN (mm)	MAX (mm)
A		9.80	10.00	C4		0.203	0.233
A1		0.356	0.456	D		1.05TYP	
A2		1.27TYP		D1		0.40	0.70
A3		0.302TYP		D2		0.15	0.25
B		3.85	3.95	R1		0.20TYP	
B1		5.84	6.24	R2		0.20TYP	
B2		5.00TYP		θ 1		8° ~ 12° TYP4	
C		1.40	1.60	θ 2		8° ~ 12° TYP4	
C1		0.61	0.71	θ 3		0° ~ 8°	
C2		0.54	0.64	θ 4		4° ~ 12°	
C3		0.05	0.25				



DIP16



symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---