

# IRLI540NPBF-VB Datasheet

## N-Channel 100-V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
100	0.034 at $V_{GS} = 10$ V	50 <sup>a</sup>

### FEATURES

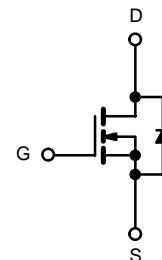
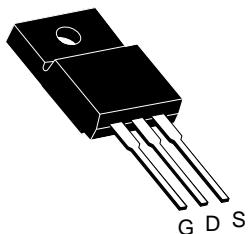
- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- Low Thermal Resistance Package
- 100 %  $R_g$  Tested



### APPLICATIONS

- Isolated DC/DC Converters

TO-220 FULLPAK



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175$ °C)	$I_D$	50 <sup>a</sup>	A
		28 <sup>a</sup>	
Pulsed Drain Current	$I_{DM}$	120	A
Avalanche Current	$I_{AS}$	31	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	61	mJ
Maximum Power Dissipation <sup>b</sup>	$P_D$	360 <sup>c</sup>	W
		3.70	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175	°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	$R_{thJA}$	40	°C/W
Junction-to-Case (Drain)	$R_{thJC}$	0.4	

Notes:

a. Package limited.

b. Duty cycle  $\leq 1$  %.

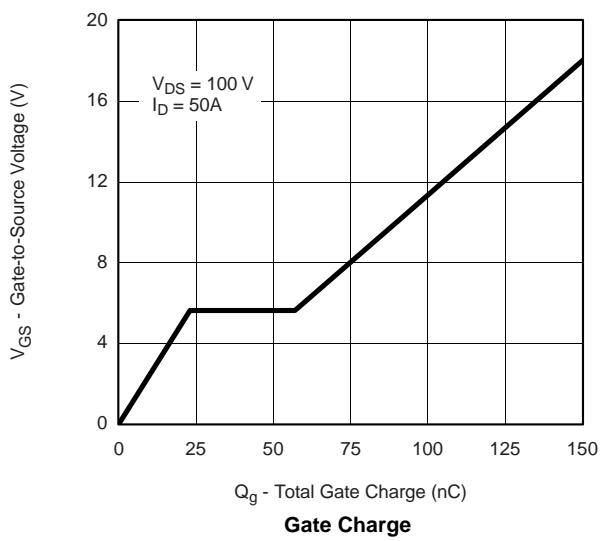
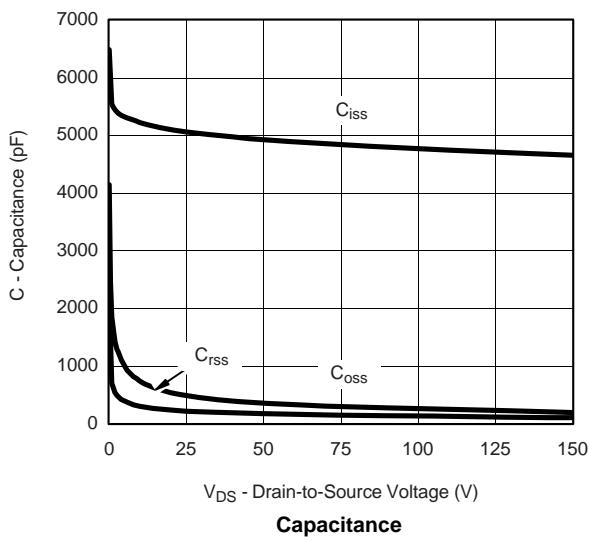
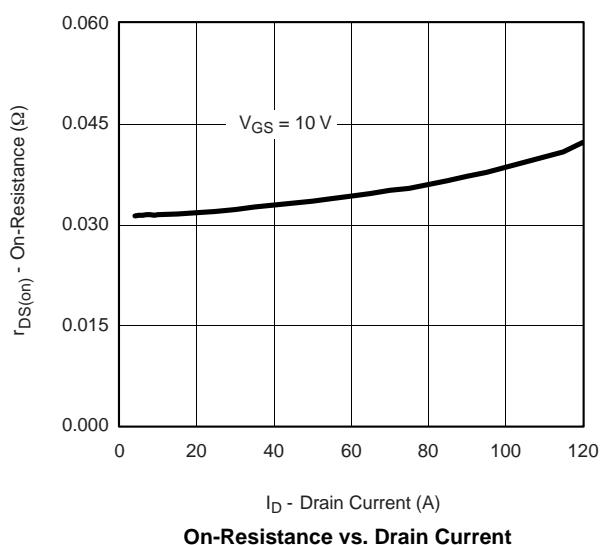
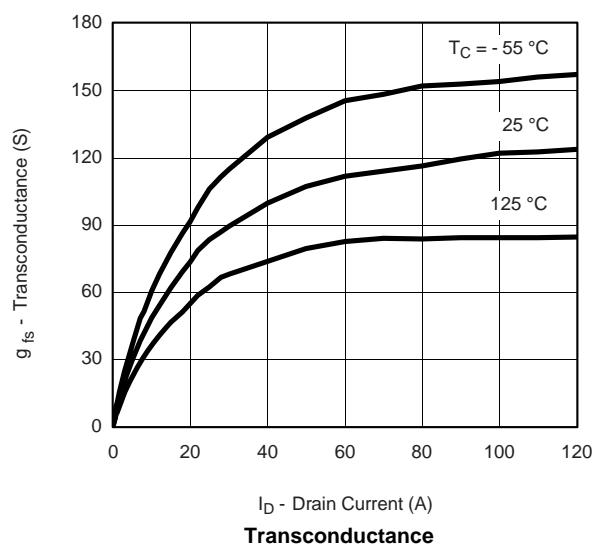
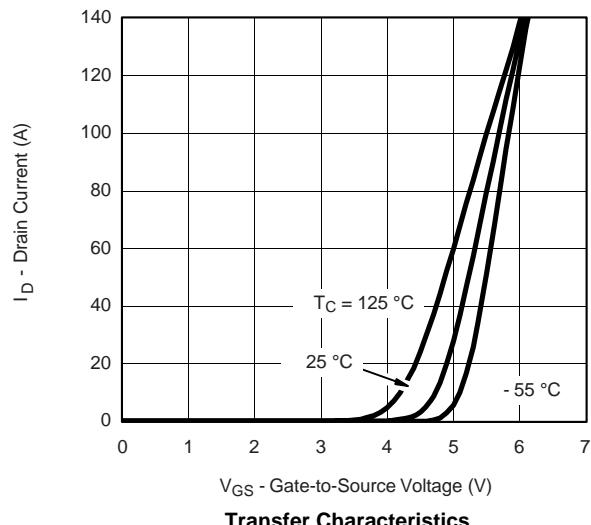
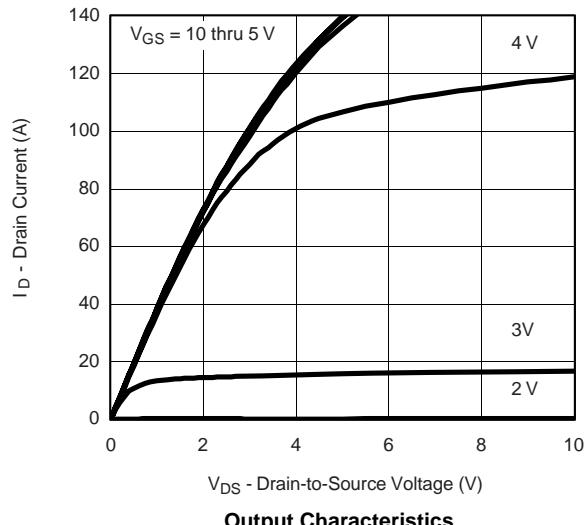
c. See SOA curve for voltage derating.

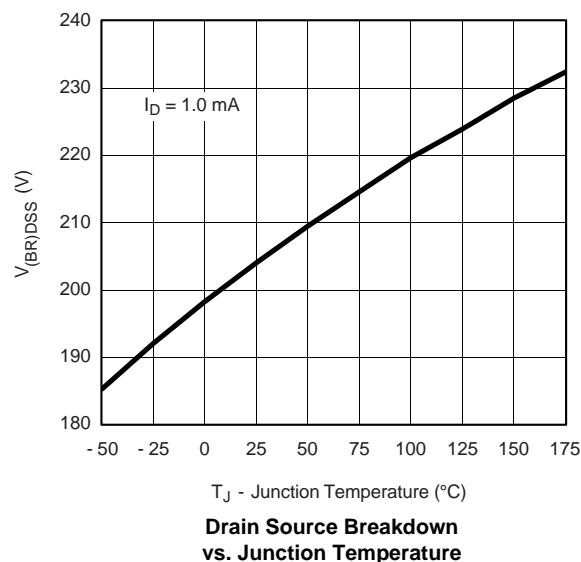
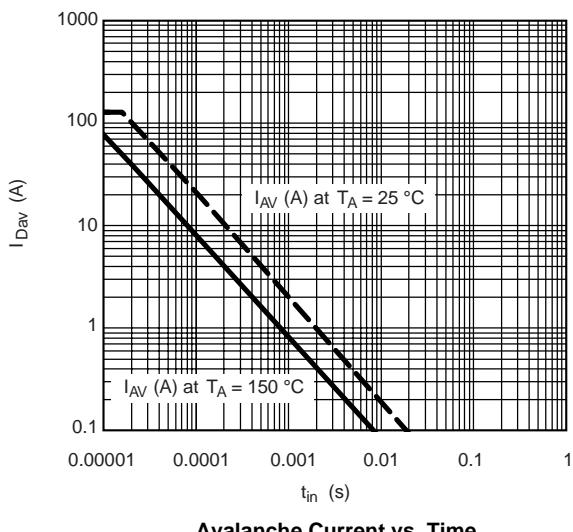
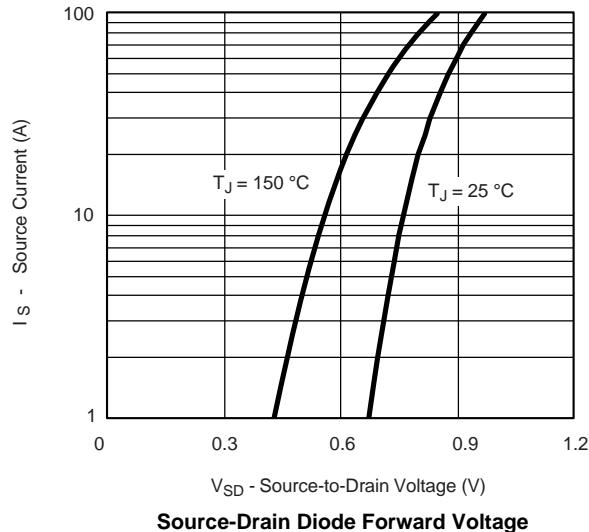
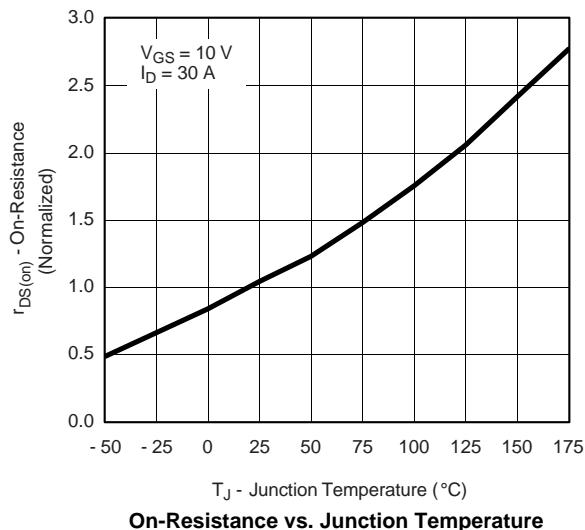
d. When Mounted on 1" square PCB (FR-4 material).

<b>SPECIFICATIONS</b> $T_J = 25^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{DS}} = 0 \text{ V}, I_{\text{D}} = 250 \mu\text{A}$	100			V
Gate-Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = 250 \mu\text{A}$	1.5		2.5	
Gate-Body Leakage	$I_{\text{GSS}}$	$V_{\text{DS}} = 0 \text{ V}, V_{\text{GS}} = \pm 20 \text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}} = 100 \text{ V}, V_{\text{GS}} = 0 \text{ V}$			1	$\mu\text{A}$
		$V_{\text{DS}} = 100 \text{ V}, V_{\text{GS}} = 0 \text{ V}, T_J = 125^\circ\text{C}$			50	
		$V_{\text{DS}} = 100 \text{ V}, V_{\text{GS}} = 0 \text{ V}, T_J = 175^\circ\text{C}$			250	
On-State Drain Current <sup>a</sup>	$I_{\text{D}(\text{on})}$	$V_{\text{DS}} \geq 5 \text{ V}, V_{\text{GS}} = 10 \text{ V}$	120			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}, I_{\text{D}} = 30 \text{ A}$		0.034		$\Omega$
		$V_{\text{GS}} = 10 \text{ V}, I_{\text{D}} = 30 \text{ A}, T_J = 125^\circ\text{C}$		0.063		
		$V_{\text{GS}} = 10 \text{ V}, I_{\text{D}} = 30 \text{ A}, T_J = 175^\circ\text{C}$		0.084		
Forward Transconductance <sup>a</sup>	$g_{\text{fs}}$	$V_{\text{DS}} = 15 \text{ V}, I_{\text{D}} = 30 \text{ A}$	25			S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 25 \text{ V}, f = 1 \text{ MHz}$		5100		pF
Output Capacitance	$C_{\text{oss}}$			480		
Reverse Transfer Capacitance	$C_{\text{rss}}$			210		
Total Gate Charge <sup>c</sup>	$Q_{\text{g}}$	$V_{\text{DS}} = 100 \text{ V}, V_{\text{GS}} = 10 \text{ V}, I_{\text{D}} = 65 \text{ A}$		90	130	nC
Gate-Source Charge <sup>c</sup>	$Q_{\text{gs}}$			23		
Gate-Drain Charge <sup>c</sup>	$Q_{\text{gd}}$			34		
Gate Resistance	$R_{\text{g}}$		0.5	1.7	3.3	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 100 \text{ V}, R_{\text{L}} = 1.5 \Omega$ $I_{\text{D}} \geq 65 \text{ A}, V_{\text{GEN}} = 10 \text{ V}, R_{\text{g}} = 2.5 \Omega$		24	35	ns
Rise Time <sup>c</sup>	$t_{\text{r}}$			220	330	
Turn-Off Delay Time <sup>c</sup>	$t_{\text{d}(\text{off})}$			45	70	
Fall Time <sup>c</sup>	$t_{\text{f}}$			200	300	
<b>Source-Drain Diode Ratings and Characteristics</b> $T_C = 25^\circ\text{C}^b$						
Continuous Current	$I_{\text{S}}$			50		A
Pulsed Current	$I_{\text{SM}}$			120		
Forward Voltage <sup>a</sup>	$V_{\text{SD}}$	$I_{\text{F}} = 65 \text{ A}, V_{\text{GS}} = 0 \text{ V}$		1.0	1.5	V
Reverse Recovery Time	$t_{\text{rr}}$	$I_{\text{F}} = 50 \text{ A}, \text{di/dt} = 100 \text{ A}/\mu\text{s}$		130	200	ns
Peak Reverse Recovery Current	$I_{\text{RM}(\text{REC})}$			8	12	A
Reverse Recovery Charge	$Q_{\text{rr}}$			0.52	1.2	$\mu\text{C}$

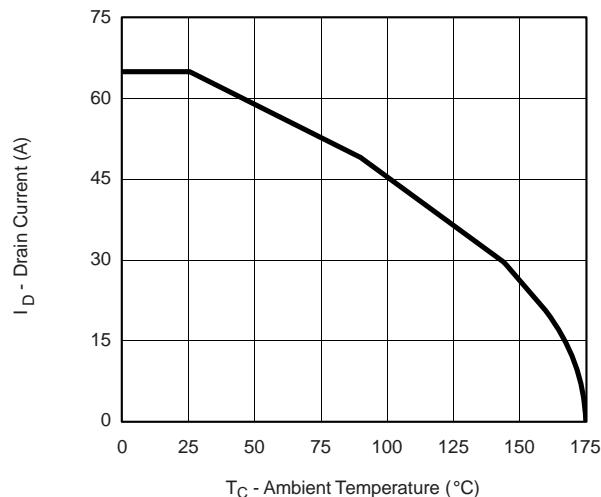
Notes:

- a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

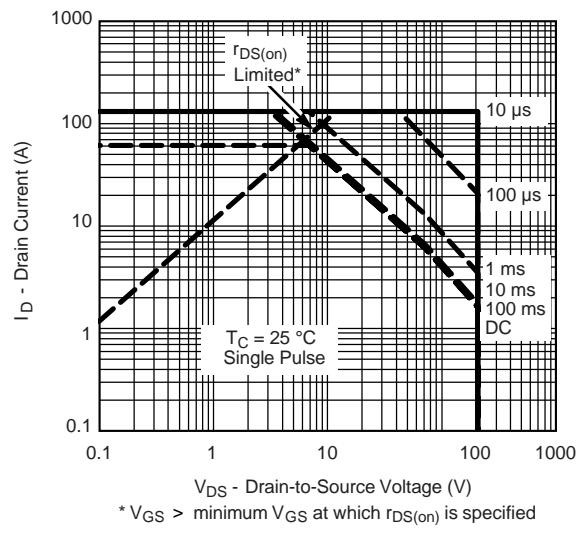
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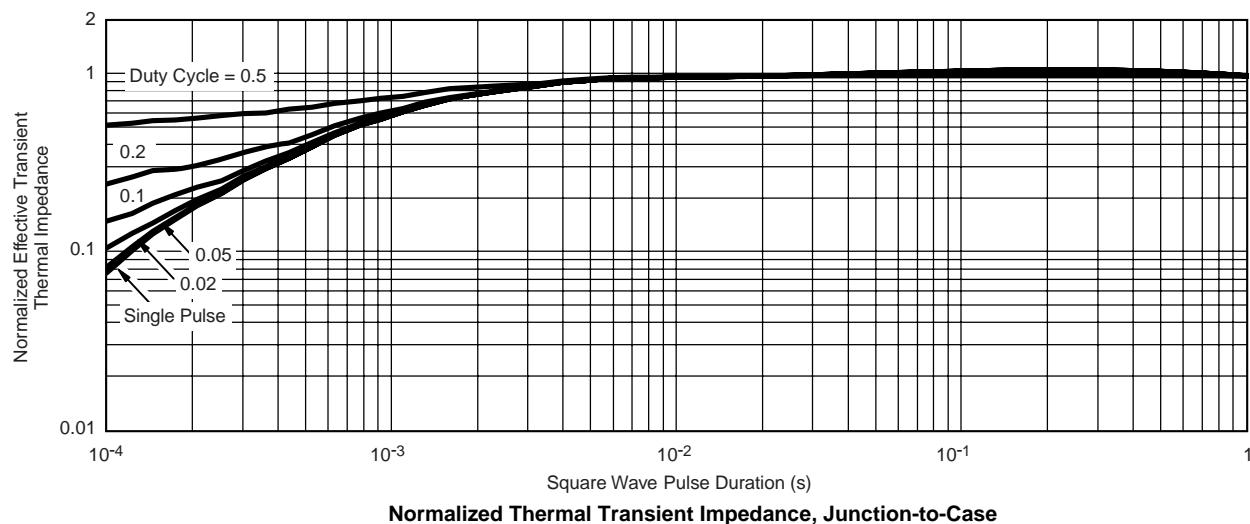
## THERMAL RATINGS



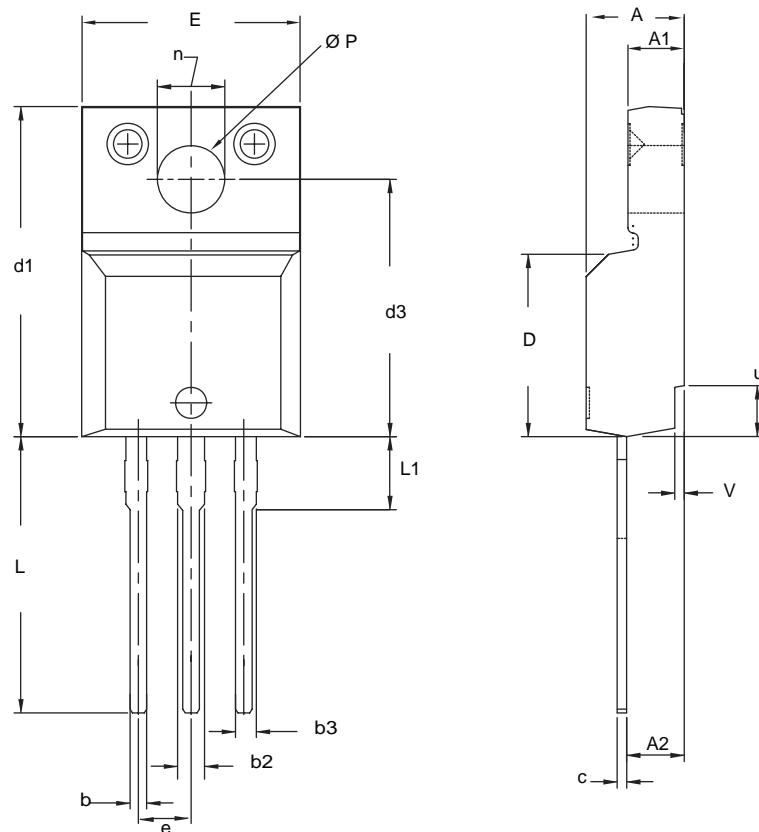
**Maximum Avalanche and Drain Current  
vs. Case Temperature**



**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Case**

**TO-220 FULLPAK (HIGH VOLTAGE)**


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
ØP	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

 ECN: X09-0126-Rev. B, 26-Oct-09  
 DWG: 5972

**Notes**

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet  $C_{pk} > 1.33$ .
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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