GSV6703

3 In to 1 Out HDMI 2.1 Repeater with Embedded MCU

April, 2022

Preliminary Product Specification

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Glossary

DDC	Display Data Channel
EDID	Extended Display Identification Data
ESD	Electrostatic Discharge
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I²C	Inter-Integrated Circuit
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
OTP	One Time Programmable
PCM	Pulse Code Modulation
S/PDIF	Sony/Philips Digital Interface Format
SPI	Serial Peripheral Interface
TMDS	Transition Minimized Differential Signaling
SCDC	Status and Control Data Channel
CEC	Consumer Electronics Control
AUX	AUX_CH, DisplayPort Auxiliary Channel
DPCD	DisplayPort Configuration Data
Main-Link	Unidirectional channel stream from DPTX to DPRX
SDP	Secondary-data Packet
DDC/CI	VESA Display Data Channel/Command Interface
MCCS	Monitor Control Command Set (VESA)
DP	DisplayPort (VESA)
DPRX	DisplayPort Receiver
DPTX	DisplayPort Transmitter
DSC	Display Stream Compression
FEC	Forward Error Correction
HBR	DisplayPort High Bit Rate, HDMI High Bit-Rate Audio
MST	DisplayPort Multi-Stream Transport
SSC	Spread-Spectrum Clock

1. General Description

1.1 General Information

Gscoolink GSV6703 is a high-performance, low-power 3 In to 1 Out HDMI 2.1 repeater. By integrating enhanced microcontroller based on RISC-V, GSV6703 has created a cost-effective solution that provides time-to-market advantages. HDMI Receiver and HDMI Transmitter support up to 40Gbps (FRL, 10G/4Lane). The superior architecture of GSV6703 provides economical smaller footprint solutions using QFN88, targeting applications of Consumer Switch and KVM.

HDCP 1.4 and HDCP 2.2/2.3 are implemented in GSV6703 for its all HDMI ports in HDMI 2.0 and FRL mode. Color Space Conversion is supported at HDMI Tx in HDMI 2.0 mode.

An internal Video Generator can be used to generate any uncompressed video timing defined in HDMI 2.1, such as 8K@60Hz, 8K@30Hz, 4K@120Hz, 480i@60Hz.

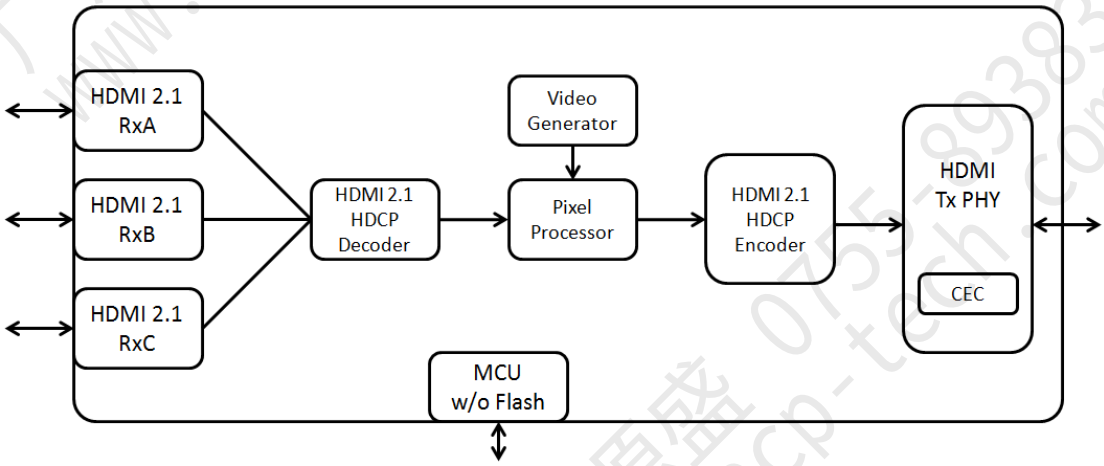


Figure 1. Top Diagram

The supported audio formats are listed in Table 1

Table 1. Supported Audio Format

Packet ID	Packet Type	Sampling Frequency (KHz)		
		32/44.1/48/88.2/ 96/176.4/192	256/352.8/384/ 512/705.6/768	64/128
0x02	Audio Sample Packet (LPCM and Compressed Audio)	Y		Y
0x07	One Bit Audio Sample Packet	Y		
0x08	DST Audio Packet	Y		
0x09	High Bit-rate Audio Stream Packet	Y	Y	

1.2 Features

1.2.1 HDMI Receiver

- Compliant with HDMI 2.1, HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4 in repeater/receiver mode
- Data rate up to 40Gbps (FRL 10Gbps/4 Lane)
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync
- Support ALLM
- Support Forward Error Correction (FEC)
- Support DSC pass-through for compressed input timing
- Embedded arbitrary EDID (up to 512 bytes)
- 5V tolerance on DDC/HPD pins
- 3D format support of frame packing, side-by-side, top-and-bottom

1.2.2 HDMI Transmitter

- Compliant with HDMI 2.1a, HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Data rate up to 40Gbps (FRL 10Gbps/4 Lane)
- Programmable Voltage Swing, Slew-Rate and Pre-emphasis
- Support AC-coupling on TMDS input/output
- Support Color Space Converter in TMDS mode
- Support HDR (HDR10/HDR10+/Dolby Vision/HLG)
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync

- Support ALLM
- Support DSC encoded stream pass-through from HDMI input
- Hardware CEC Engine for Low Level protocol decoding
- 5V tolerance on DDC/HPD/CEC pins
- 3D format support of frame packing, side-by-side, top-and-bottom

1.2.3 System Features

- Optional External MCU (via I2C)/ Internal MCU mode
- Embedded MCU and External Flash
- External pins of Flash QSPI interface
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO control from embedded MCU
- Mailbox feature for external MCU access on chip function status
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 HDMI switch application

RxA/RxB/RxC are configured as HDMI Rx Inputs. This mode is applicable for monitor application.

Within bandwidth limitation, GSV6703 can keep input stream consistent and intact, while dynamically switch output between FRL and HDMI 2.0 mode for the best compatibility. For example, when FRL10G/4Lane 4K@60Hz timing is input, GSV6703 can convert to HDMI 2.0 or FRL 6G/3Lane, FRL 6G/4Lane, FRL 8G/4Lane, FRL 10G/4Lane as output. During HDMI output mode switch, HDMI input stream will not be disturbed.

GSV6703 can also support fixed output FRL rate, regardless of HDMI input mode. For example, when HDMI 2.0 4K@30Hz is input, GSV6703 can convert it to FRL 10G/4Lane output. And when FRL 8G/4Lane 4K@120Hz is input, GSV6703 can still maintain FRL 10G/4Lane output with timing conversion.

Meanwhile, Audio extraction can be applicable if required.

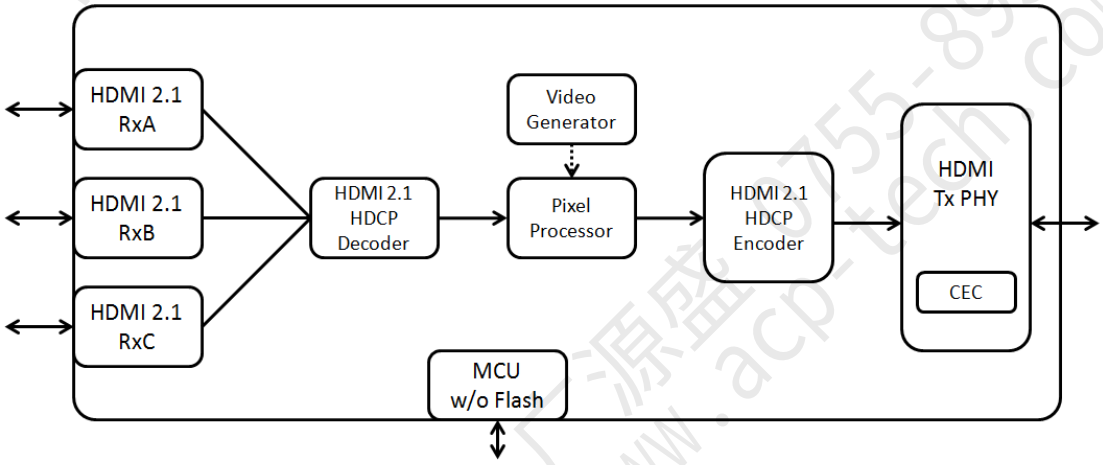


Figure 2. Input Switch Between Different Inputs

2. Pin Description

2.1 QFN88 Pin Diagram

QFN88 Pin definition is defined as below.

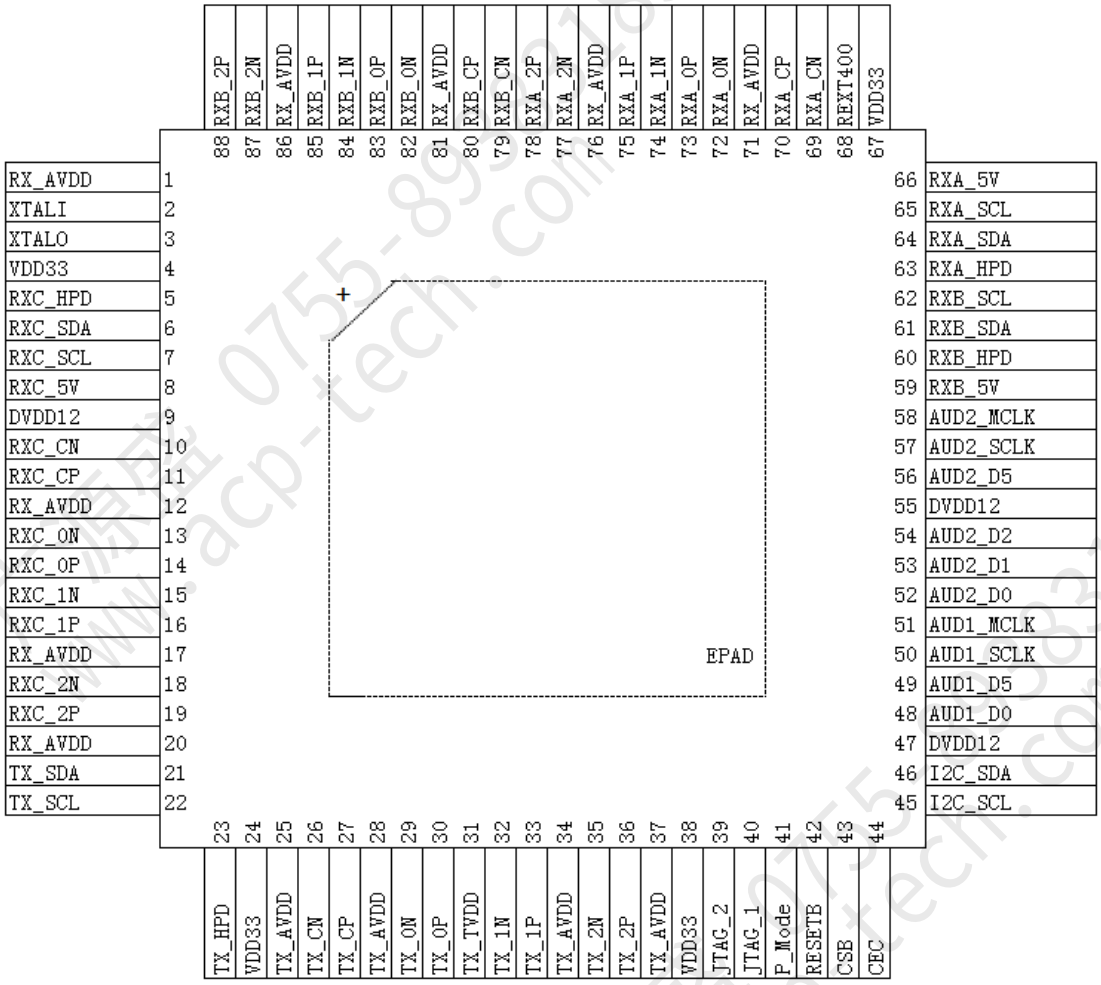


Figure 3. GSV6703 QFN88 Pin Diagram

2.2 QFN88 Pin Description

Table 2. QFN88 Pin Description

Pin Name	Direction	Pin No.	Description
HDMI RxA Pins			
RXA_5V	I	66	RXA 5V Detection PAD
RXA_HPD	I/O	63	RXA HPD PAD
RXA_SDA	I/O	64	RXA DDC SDA PAD
RXA_SCL	I/O	65	RXA DDC SCL PAD

RXA_CN	I	69	RXA Negative TMDS differential data input [3]/ TMDS clock differential input
RXA_CP	I	70	RXA Positive TMDS differential data input [3]/ TMDS clock differential input
RXA_0N	I	72	RXA Negative TMDS differential data input [0]
RXA_0P	I	73	RXA Positive TMDS differential data input [0]
RXA_1N	I	74	RXA Negative TMDS differential data input [1]
RXA_1P	I	75	RXA Positive TMDS differential data input [1]
RXA_2N	I	77	RXA Negative TMDS differential data input [2]
RXA_2P	I	78	RXA Positive TMDS differential data input [2]
HDMI RxB Pins			
RXB_5V	I	59	RXB 5V Detection PAD
RXB_HPD	I/O	60	RXB HPD PAD
RXB_SDA	I/O	61	RXB DDC SDA PAD
RXB_SCL	I/O	62	RXB DDC SCL PAD
RXB_CN	I	79	RXB Negative TMDS differential data input [3]/ TMDS clock differential input
RXB_CP	I	80	RXB Positive TMDS differential data input [3]/ TMDS clock differential input
RXB_0N	I	82	RXB Negative TMDS differential data input [0]
RXB_0P	I	83	RXB Positive TMDS differential data input [0]
RXB_1N	I	84	RXB Negative TMDS differential data input [1]
RXB_1P	I	85	RXB Positive TMDS differential data input [1]
RXB_2N	I	87	RXB Negative TMDS differential data input [2]
RXB_2P	I	88	RXB Positive TMDS differential data input [2]
HDMI RxC Pins			
RXC_5V	I	8	RXC 5V Detection PAD
RXC_HPD	I/O	5	RXC HPD PAD
RXC_SDA	I/O	6	RXC DDC SDA PAD
RXC_SCL	I/O	7	RXC DDC SCL PAD
RXC_CN	I	10	RXC Negative TMDS differential data input [3]/ TMDS clock differential input
RXC_CP	I	11	RXC Positive TMDS differential data input [3]/ TMDS clock differential input
RXC_0N	I	13	RXC Negative TMDS differential data input [0]
RXC_0P	I	14	RXC Positive TMDS differential data input [0]

RXC_1N	I	15	RXC Negative TMDS differential data input [1]
RXC_1P	I	16	RXC Positive TMDS differential data input [1]
RXC_2N	I	18	RXC Negative TMDS differential data input [2]
RXC_2P	I	19	RXC Positive TMDS differential data input [2]
Power/Ground Pins			
DVDD12	Power	9,47,55	Digital 1.2V voltage power supply
TX_TVDD	Power	31,	Analog 3.3V voltage power supply for TX Port
VDD33	Power	4,24,38, 67	Digital 3.3V voltage power supply
RX_AVDD	Power	1,12,17, 20,71,76, 81,86	Analog 1.2V voltage power supply for RX Port
TX_AVDD	Power	25,28, 34,37	Analog 1.2V voltage power supply for TX Port
REXT400	Power	68	External 400 ohm resistors to 3.3V Power supply
HDMI Tx Pins			
TX_SDA	I/O	21	TXA DDC SDA Pin
TX_SCL	O	22	TXA DDC SCL Pin
TX_HPD	I	23	TXA HPD PAD
CEC	I/O	44	TXA CEC Pin
TX_CN	O	26	TXA Negative TMDS clock output/ differential data output [3]
TX_CP	O	27	TXA Positive TMDS clock output/ differential data output [3]
TX_0N	O	29	TXA Negative TMDS differential data output [0]
TX_0P	O	30	TXA Positive TMDS differential data output [0]
TX_1N	O	32	TXA Negative TMDS differential data output [1]
TX_1P	O	33	TXA Positive TMDS differential data output [1]
TX_2N	O	35	TXA Negative TMDS differential data output [2]
TX_2P	O	36	TXA Positive TMDS differential data output [2]
Digital pins			
I2C_SDA	I/O	46	Default: Digital IO for I2C Data Alternate: GPIO8 for internal MCU
I2C_SCL	I/O	45	Default: Digital IO for I2C Clock Alternate: GPIO9 for internal MCU

AUD2_D0	I/O	52	Digital IO PAD Default: Data0 of Audio Bus 2 Alternate 1: QSPI_D1 for QSPI Flash connection Alternate 2: GPIO7 for internal MCU control Alternate 3: EP_MISO for internal MCU SPI control Alternate 4: UART_TX for internal MCU control
AUD2_D1	I/O	53	Digital IO PAD Default: Data1of Audio Bus 2 Alternate 1: QSPI_D1 for QSPI Flash connection Alternate 2: GPIO10 for internal MCU control Alternate 3: EP_MISO for internal MCU SPI control Alternate 4: UART_TX for internal MCU control
AUD2_D2	I/O	54	Digital IO PAD Default: Data2 of Audio Bus 2 Alternate 1: QSPI_D0 for QSPI Flash connection Alternate 2: GPIO11 for internal MCU control Alternate 3: EP_MOSI for internal MCU SPI control Alternate 4: UART_RX for internal MCU control
AUD2_D5	I/O	56	Digital IO PAD Default: Data5 of Audio Bus 2 Alternate 1: QSPI_D0 for QSPI Flash connection Alternate 2: GPIO6 for internal MCU control Alternate 3: EP_MOSI for internal MCU SPI control Alternate 4: UART_RX for internal MCU control Alternate 5: CEC
AUD2_SCLK	I/O	57	Digital IO PAD Default: SCLK of Audio Bus 2 Alternate 1: QSPI_SCK for QSPI Flash connection Alternate 2: GPIO5 for internal MCU control Alternate 3: EP_SCK for internal MCU SPI control Alternate 4: ADV_TIM2 for internal MCU control
AUD2_MCLK	I/O	58	Digital IO PAD Default: MCLK of Audio Bus 2 Alternate 1: QSPI_CSB for QSPI Flash connection Alternate 2: GPIO4 for internal MCU control Alternate 3: EP_CSB for internal MCU SPI control Alternate 4: ADV_TIM1 for internal MCU control

RESETB	I	42	Reset Pin. Low for reset state, High for functional state.
XTALI	I/O	2	25M Crystal Input
XTALO	I/O	3	25M Crystal output
JTAG_2	I/O	39	Default: TMS, Internal MCU programming pin Alternate: General Interrupt Output Pin
JTAG_1	I	40	Default: TCK, Internal MCU programming pin Alternate: AVMUTE Interrupt Output Pin
P_MODE	I	41	Internal MCU Boot Option High = QSPI Flash boot Low = External MCU boot
SPI_CSB	I/O	51	QSPI_CSB for QSPI Flash connection
SPI_SCK	I/O	50	QSPI_SCK for QSPI Flash connection
SPI_MOSI	I/O	49	QSPI_MOSI for QSPI Flash connection
SPI_MISO	I/O	48	QSPI_MISO for QSPI Flash connection
CSB	I/O	43	Chip Selection Option High = Not Selected Low = Selected (Default)
NC	I/O		No Connection

3. Electrical Specifications

3.1 Timing Information

3.1.1 Power Up and Reset Timing Diagrams

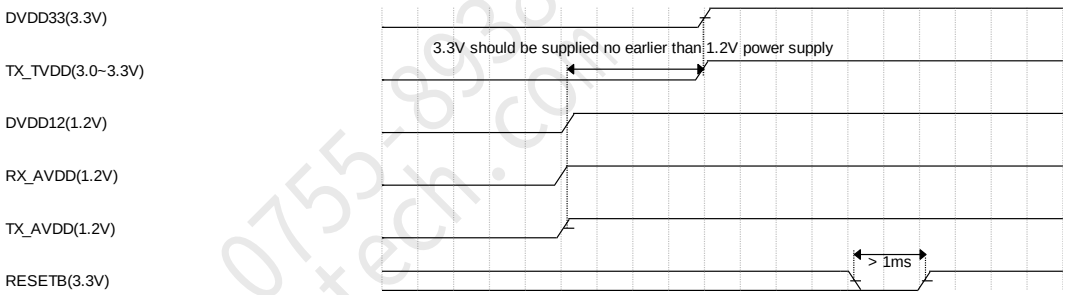


Figure 4. Power Up Sequence

3.1.2 I2C Timing Diagrams

The I2C bus uses 8-bit page address and 16-bit register address. ACK should be provided per 8-bit transaction. For every register, 8-bit data will be accessed. The device address is 0xB0 in 8-bit.

The I2C write timing is shown below.

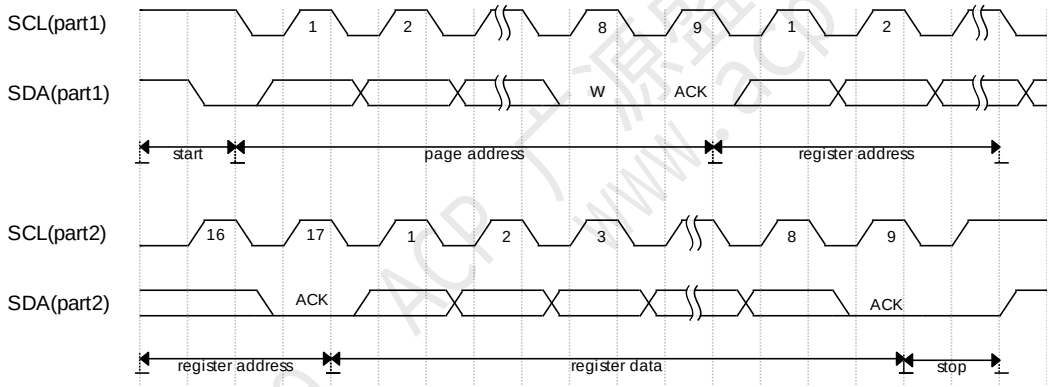


Figure 5. I2C Timing Diagram(Write)

The I2C read timing is shown below.

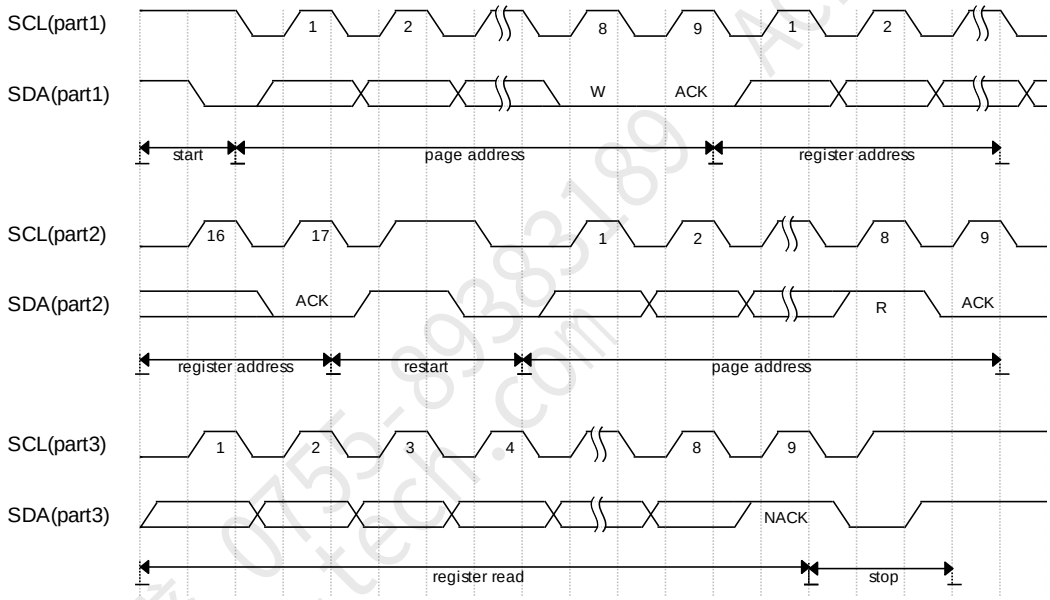


Figure 6. I2C Timing Diagram(Read)

3.1.3 I2S Timing Diagrams

I2S standard timing is shown as below, which is the default I2S timing of audio input/output.

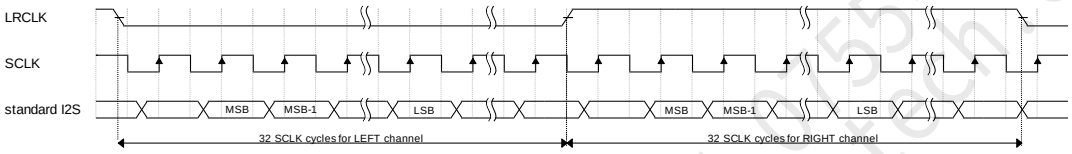


Figure 7. I2S Standard Timing Diagram

I2S left-justified timing is shown as below, which is can be tuned by register configuration.

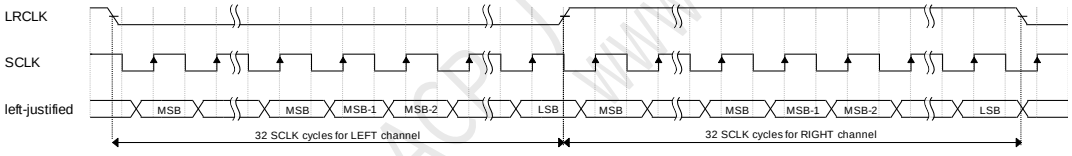


Figure 8. I2S Left-Justified Timing Diagram

I2S right-justified timing is shown as below, which is can be tuned by register configuration.

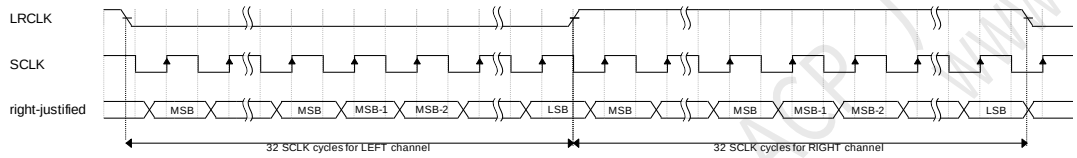


Figure 9. I2S Right-Justified Timing Diagram

3.2 Operating Conditions

3.2.1 Temperature Conditions

GSV6703's operation temperature range is -20 ºC to 85 ºC. The maximum junction temperature is at 125 ºC. GSV6703 embeds internal temperature sensor for junction temperature read back.

3.2.2 Electrical Conditions

Table 3. Absolute Maximum Ratings

Power Domain	Minimum	Typical	Maximum
DVDD33	-0.5V	3.3V	5.0V
TX_TVDD	-0.5V	3.3V	5.0V
DVDD12	-0.5V	1.2V	1.8V
RX_AVDD	-0.5V	1.2V	1.8V
TX_AVDD	-0.5V	1.2V	1.8V
HBM(ESD)			+/-2KV
CDM(ESD)			+/-1KV
MM(ESD)			+/-200V

If HDMI Rx is 48G as FRL maximum rate in dedicated application, 1.19V is the minimum operation voltage for DVDD12/RX_AVDD/TX_AVDD/TX_PVDD, typical and maximum operation conditions are listed below. When 40G and below FRL maximum rate is used in applications, follow the below table for operation conditions.

Table 4. Functional Operation Conditions

Power Domain	Minimum	Typical	Maximum
DVDD33	3.0V	3.3V	3.6V
TX_TVDD	3.0V	3.3V	3.6V
DVDD12	1.08V	1.2V	1.32V
RX_AVDD	1.08V	1.2V	1.32V
TX_AVDD	1.08V	1.2V	1.32V

3.2.3 Audio Pin Conditions

GSV6703's Audio TTL pins can tolerate 2.8V~3.6V as logic HIGH.

3.2.4 I2C Conditions

GSV6703's I2C maximum SCL frequency is 400KHz.

3.2.5 Crystal Oscillator Conditions

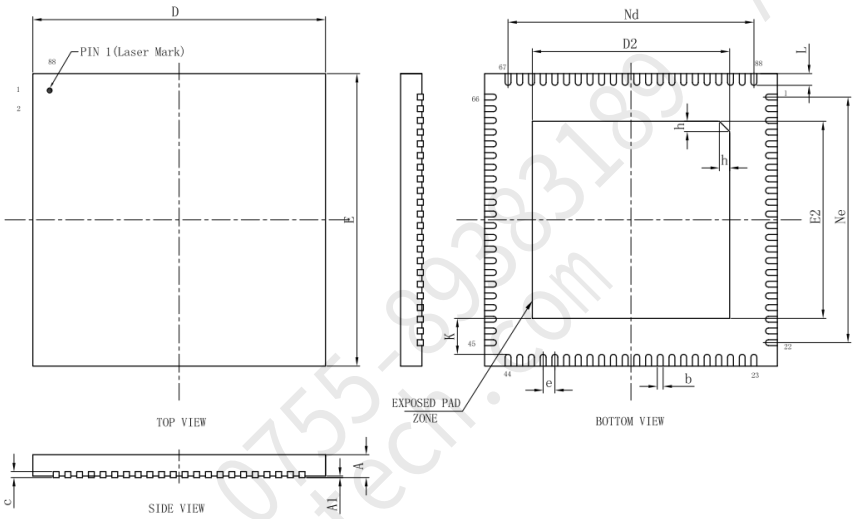
GSV6703's crystal oscillator input should be <300 ppm, EF<0.7, CL=18pF,ESR=50.

3.3 HDMI Transmitter

Table 5. TMDS DC and AC Characteristics

Item	Value
Single-Ended High Level Voltage Range: Data Channels 0,1,2	TVDD - 400mV ~ TVDD + 10mV
Single-Ended Low Level Voltage Range: Data Channels 0,1,2	TVDD - 1000mV ~ TVDD - 400mV
Single-Ended High Level Range: Clock Channel	TVDD - 400mV ~ TVDD + 10mV
Single-Ended Low Level Voltage Range: Clock Channel	TVDD - 1000mV ~ TVDD - 400mV
Single-Ended Swing Voltage: Data Channels 0,1,2	400mV~600mV
Single-Ended Swing Voltage: Clock Channel	200mV~600mV

4. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	9.90	10.00	10.10
D2	6.64	6.74	6.84
e	0.40BSC		
Nd	8.40REF		
E	9.90	10.00	10.10
E2	6.64	6.74	6.84
Ne	8.40REF		
L	0.30	0.40	0.50
K	0.20	-	-
h	0.30	0.35	0.40
L/F载体尺寸 (mil)	300x300		

Figure 10. Package Dimensions (QFN88)

5. Ordering Guide

Table 6. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV6703	−20°C to +85°C	QFN88	Tray

6. Revision History

Table 7. Revision history

Revision No.	Description	Date
V0.1	Draft Initial Version for internal review.	Apr 28, 2022
V0.2	Package information update to QFN124	Jun 28, 2022
V0.3	Correct TCK/TMS pin description	Jul 18, 2022
V0.4	Correct Power up Sequence	Jul 18, 2022
V0.5	Modify content to mass production version.	Aug 4, 2022
V0.6	Remove description about QFN96	Aug 10, 2022
V0.7	Modify audio support feature	Sep 15, 2022
V0.8	Correct typo of Audio Extraction	Oct 14, 2022
V0.9	Clarify External Flash definition	Jan 3, 2023
V1.0	Add Power Information	Mar 3, 2023
V1.1	Separate TX_TVDD pins in pin list, add I2S timing table and crystal requirement	Apr 12, 2023
V1.2	Update TX_TVDD, TVDD pin description	Apr 25, 2023
V1.3	Correct Pin mapping name of NC pins	May 4, 2023
V1.4	Add minimum power condition for 48G FRL	Sep 8, 2023
V1.5	Add 3D support, ESD information, fix typo	Nov 13, 2023
V1.6	Modify to QFN88 package	Feb 20, 2024

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