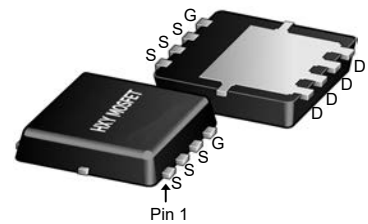


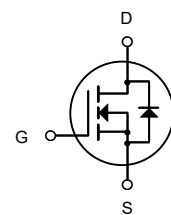
### Description

The HSiR804DP uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



DFN5X6-8L

## General Features

$$V_{DS} = 30V \quad I_D = 80A$$
$$R_{DS(ON)} < 6 \text{ m}\Omega \quad V_{GS}=10V$$


## N-Channel MOSFET

## Application

## Battery protection

Load switch

Uninterruptible power supply

## Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
HSiR804DP	DFN5X6-8L	HXY MOSFET	5000

**Absolute Maximum Ratings (T<sub>c</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	30	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	80	A
I <sub>D</sub> @T <sub>C</sub> =70°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	45	A
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	280	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>3</sup>	56	mJ
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	37	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C
R <sub>θJA</sub>	Thermal Resistance Junction-Ambient <sup>1</sup>	30	°C/W



**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	30	--	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	--	--	0.1	μA
	Zero Gate Voltage Drain Current(T <sub>J</sub> =125°C)	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	--	--	100	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	--	--	±100	nA
V <sub>GS(TH)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.7	2.5	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance③	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	--	4.7	6	mΩ
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance③	V <sub>GS</sub> =4.5V, I <sub>D</sub> =16A	--	5.4	8	mΩ
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	--	1930	--	pF
C <sub>oss</sub>	Output Capacitance		--	310	--	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	260	--	pF
R <sub>g</sub>	Gate Resistance	f=1MHz	--	0.85	--	
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =15V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	--	38	--	nC
Q <sub>gs</sub>	Gate-Source Charge		--	5.1	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	12	--	nC
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =15V, I <sub>D</sub> =20A, R <sub>G</sub> =3, V <sub>GS</sub> =10V	--	8.5	--	nS
t <sub>r</sub>	Turn-on Rise Time		--	9	--	nS
t <sub>d(off)</sub>	Turn-Off Delay Time		--	31	--	nS
t <sub>f</sub>	Turn-Off Fall Time		--	9	--	nS
V <sub>SD</sub>	Forward on voltage	I <sub>SD</sub> =20A, V <sub>GS</sub> =0V	--	0.8	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	T <sub>J</sub> =25°C, I <sub>sd</sub> =20A, V <sub>GS</sub> =0V	--	16	--	nS
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=500A/μs		42		nC

**NOTE:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.5mH, R<sub>G</sub> = 25 , I<sub>AS</sub> = 15A, V<sub>GS</sub> =10V. Part not recommended for use above this value
- ③ Pulse width ≤ 300μs; duty cycle≤ 2%.



## Typical Characteristics

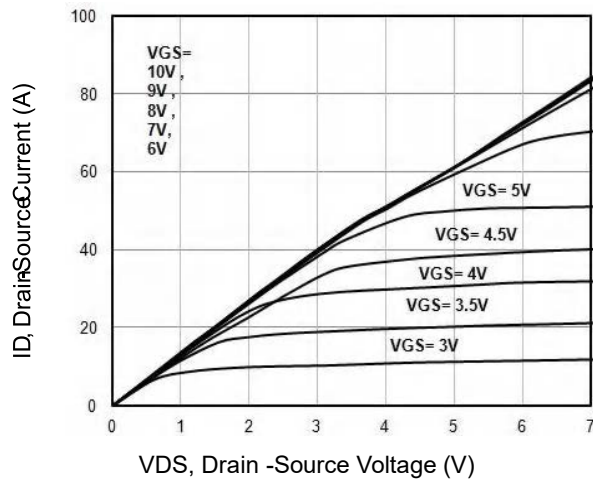


Fig1. Typical Output Characteristics

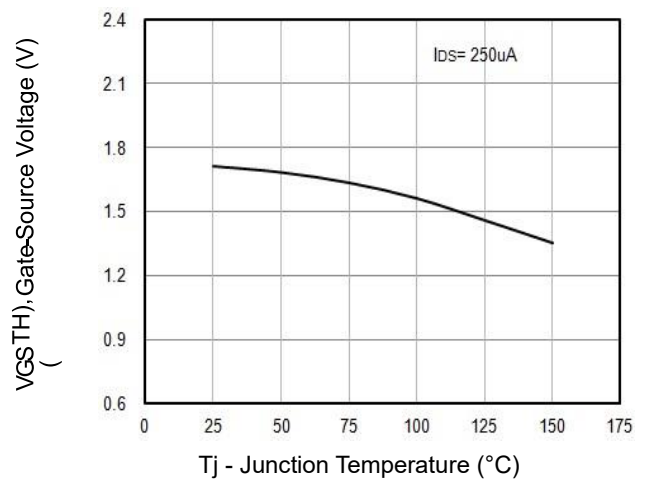


Fig2.  $V_{GS(TH)}$  Gate-Source Voltage Vs.  $T_J$

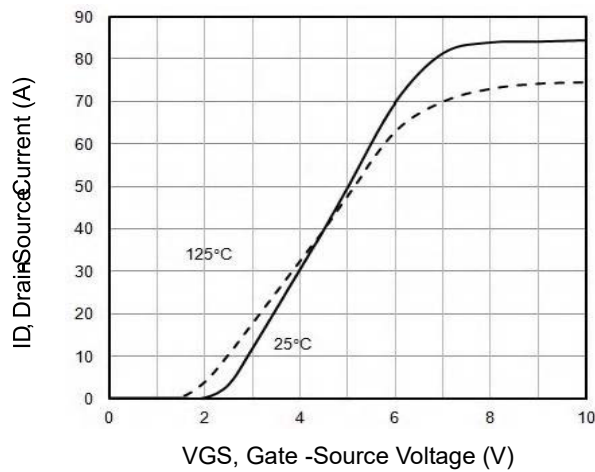


Fig3. Typical Transfer Characteristics

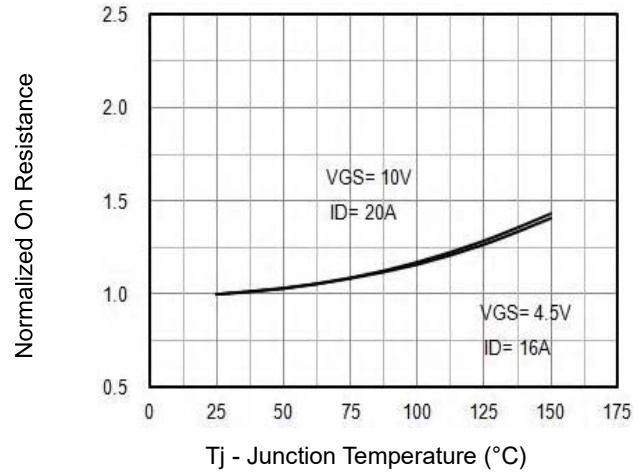


Fig4. Normalized On-Resistance Vs.  $T_J$

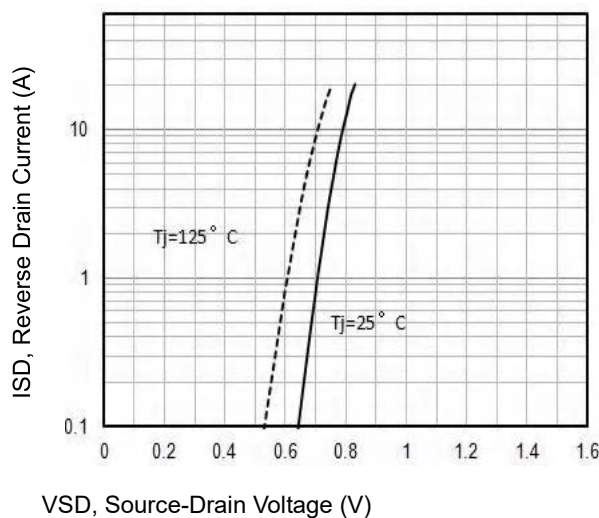


Fig6. Maximum Safe Operating Area  
Voltage

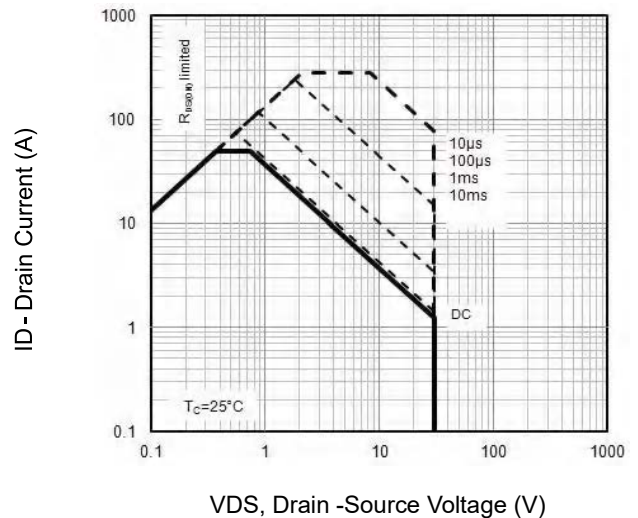


Fig5. Typical Source-Drain Diode Forward

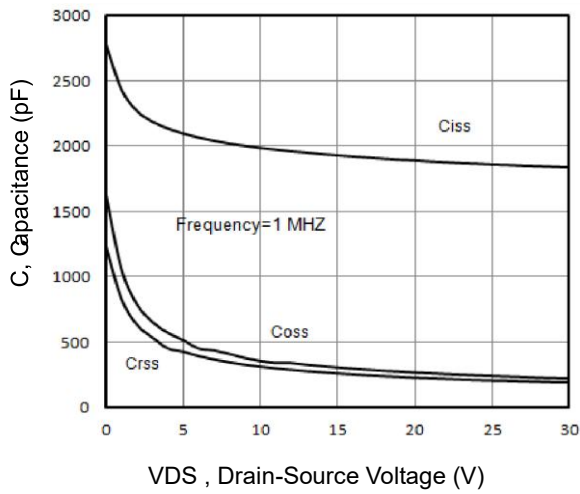


Fig7. Typical Capacitance Vs. Drain-Source Voltage

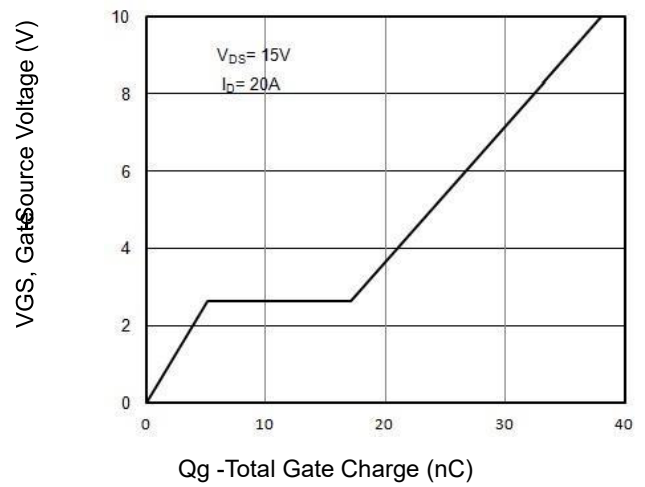


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

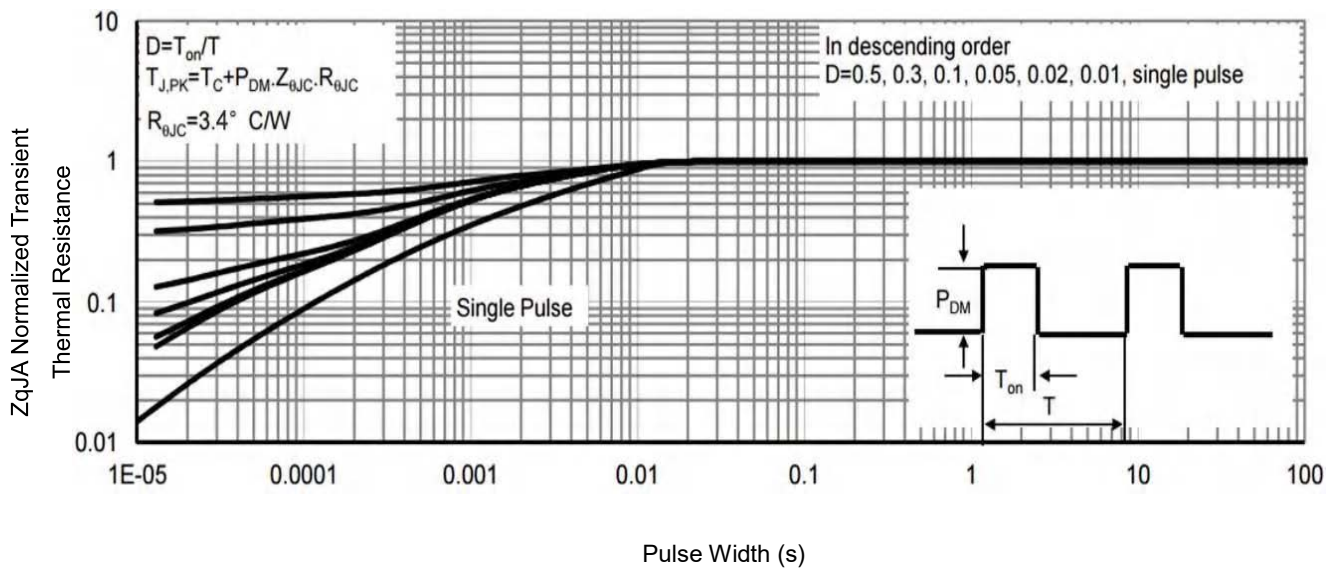


Fig9. Normalized Maximum Transient Thermal Impedance

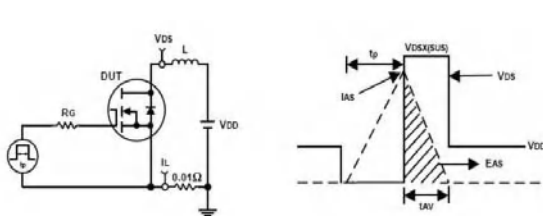


Fig10. Unclamped Inductive Test Circuit and waveforms

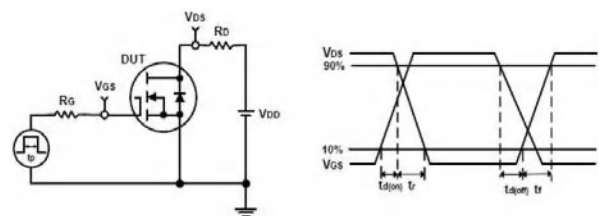
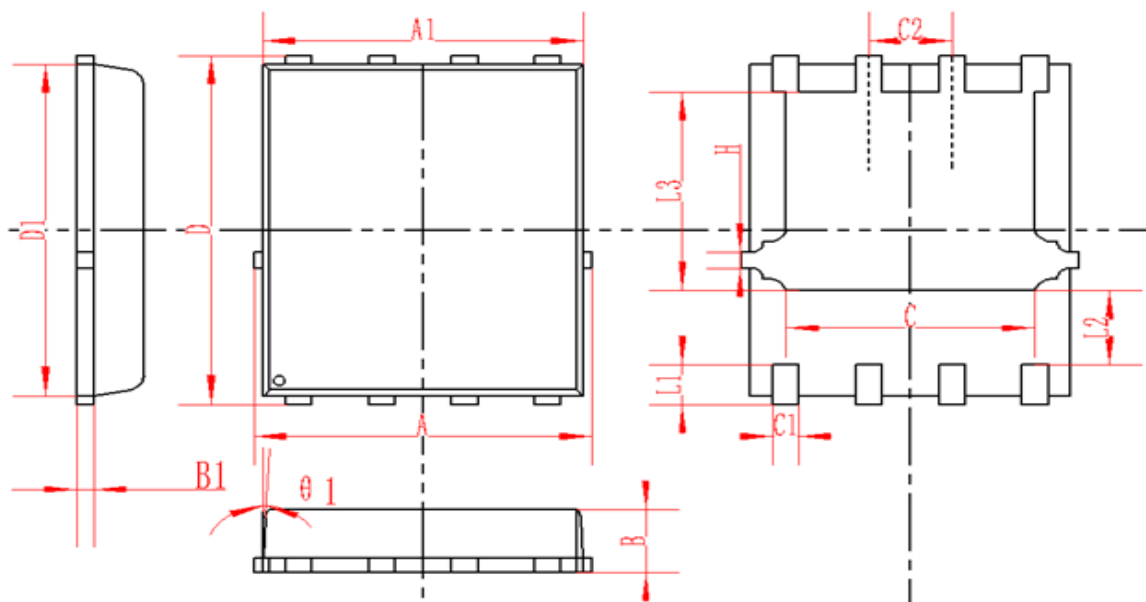


Fig11. Switching Time Test Circuit and waveforms



## DFN5X6-8L Package Information



SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
θ1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010



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