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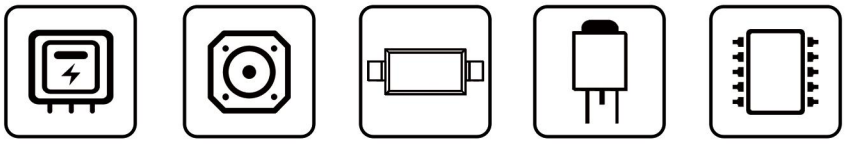
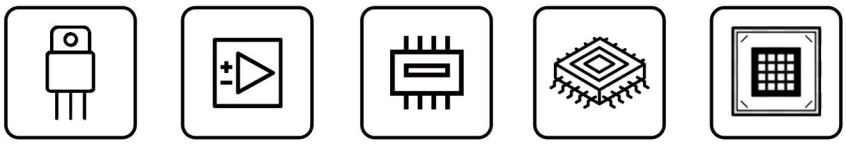




AO4409-TD

產品規格說明書

AO4409-TD
30V P-Channel Enhancement Mode MOSFET

General Description:

The AO4409-TD is the single P-Channel logic enhancement mode power field effect transistors to provide excellent RDS(on), low gate charge and low gate resistance. It's up to -30V operation voltage is well suited in switching mode power supply, SMPS, notebook computer power management and other battery powered circuits.

Features:

$R_{DS(ON)}$<7.5m @V_{GS}=10V (P-Ch)

$R_{DS(ON)}$<13 m @V_{GS}=4.5V (P-Ch)

Super high density cell design for extremely low

RDS(ON) Exceptional on-resistance and maximum DC current

Applications:

Switching power supply, SMPS

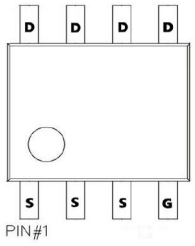
Battery Powered System

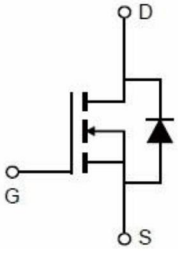
DC/DC Converter

DC/AC Converter

Load Switch

SOP-8 Pin Configuration





Package Marking and Ordering Information

Product ID	Package	Marking	QTY(PCS)	Packing methed
AO4409-TD	SOP-8	AO4409-TD	3000	Reel

Absolute Maximum Ratings (TC=25℃ unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ -10V[1,6]	-18	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ -10V[1,6]	-8.8	A
I_{DM}	Pulsed Drain Current[2]	-53	A
EAS	Single Pulse Avalanche Energy[3]	-80	mJ
I_{AS}	Avalanche Current	-40	A
P_D@T_C=25℃	Total Power Dissipation[4]	90	W
T_{STG}	Storage Temperature Range	-55 to 175	℃
T_J	Operating Junction Temperature Range	-55 to 175	℃
$R_{\theta JA}$	Thermal Resistance Junction-ambient [1](t≦10S)	20	℃/W
	Thermal Resistance Junction-ambient [1](Steady State)	50	℃/W

$R_{\theta JC}$	Thermal Resistance Junction-case [1]	1.6	°C/W

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-30	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-20A	---	5.6	7.5	mΩ
		V_{GS}=-4.5V , I_D=-15A	---	9.5	13	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.2	---	-2.5	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-24V , V_{GS}=0V , T_J=25°C	---	---	-1	uA
		V_{DS}=-24V , V_{GS}=0V , T_J=55°C	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
Rg	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.2	---	Ω
Q_g	Total Gate Charge (-10V)	V_{DS}=-15V , V_{GS}=-10V , I_D=-18A	---	60	---	nC
Q_{gs}	Gate-Source Charge		---	9	---	
Q_{gd}	Gate-Drain Charge		---	15	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V , V_{GS}=-10V , R_G=3.3 , I_D=-20A	---	17	---	ns
T_r	Rise Time		---	40	---	
$T_{d(off)}$	Turn-Off Delay Time		---	55	---	
T_f	Fall Time		---	13	---	
C_{iss}	Input Capacitance	V_{DS}=-25V , V_{GS}=0V , f=1MHz	---	3450	---	pF
C_{oss}	Output Capacitance		---	255	---	
C_{rss}	Reverse Transfer Capacitance		---	140	---	
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	-70	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25°C	---	---	-1.2	V
t_{rr}	Reverse Recovery Time	I_F=-20A , di/dt=100A/μs , T_J=25°C	---	22	---	nS
Q_{rr}	Reverse Recovery Charge		---	72	---	nC

Note :
1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=-50V,V_{GS}=-10V,L=0.1mH,I_{AS}=-40A
4.The power dissipation is limited by 150°C junction temperature
5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation
6.The maximum current rating is package limited.

Typical Characteristics

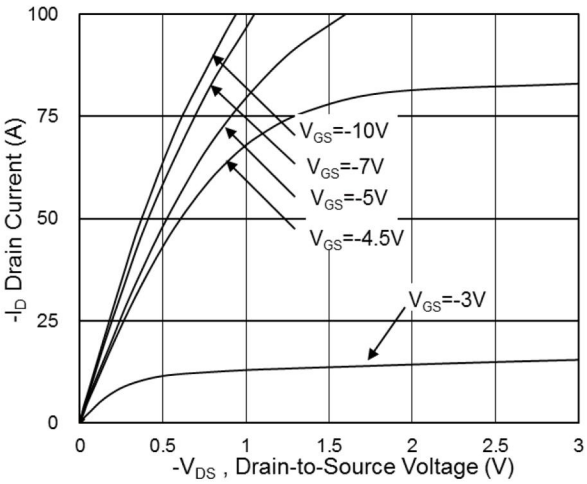


Fig.1 Typical Output Characteristics

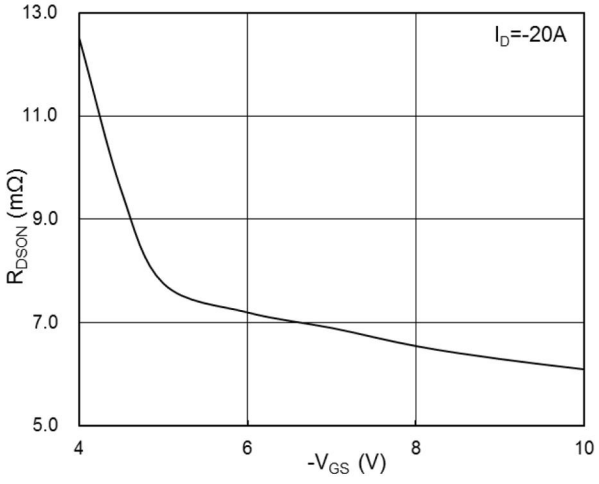


Fig.2 On-Resistance vs. Gate-Source Voltage

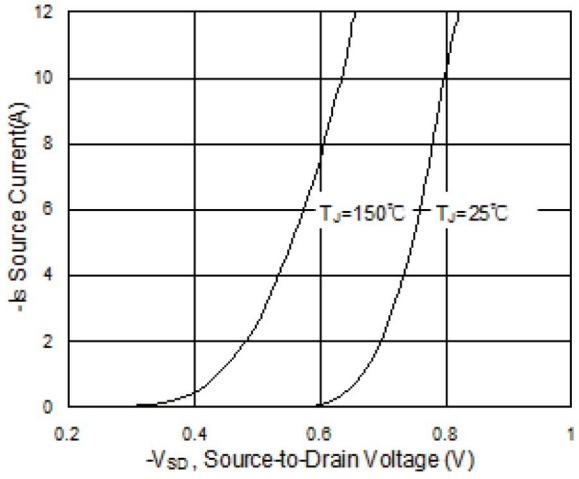


Fig.3 Forward Characteristics of Reverse

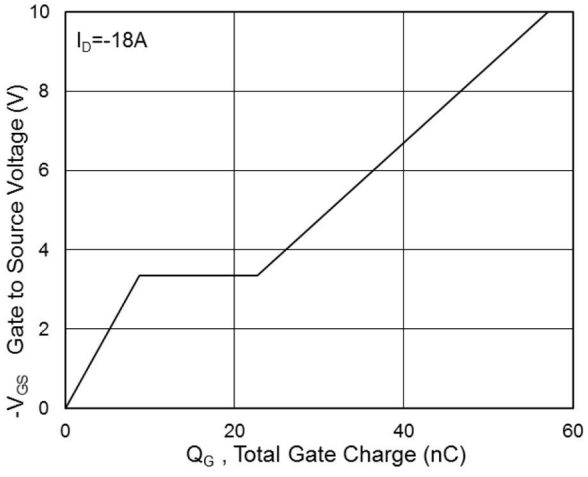


Fig.4 Gate-Charge Characteristics

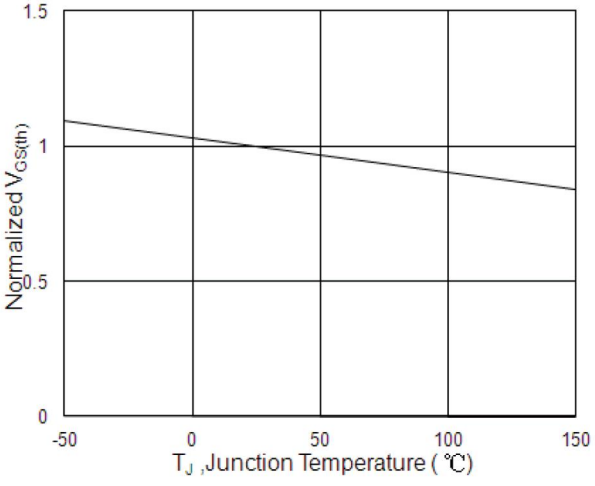


Fig.5 Normalized $-V_{GS(th)}$ vs. T_J

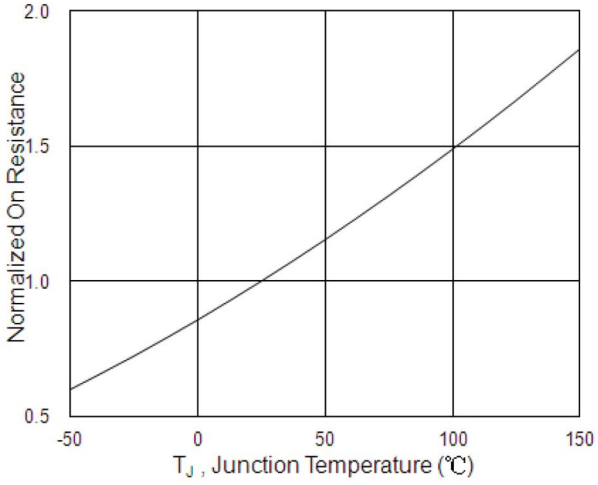


Fig.6 Normalized R_{DSON} vs. T_J

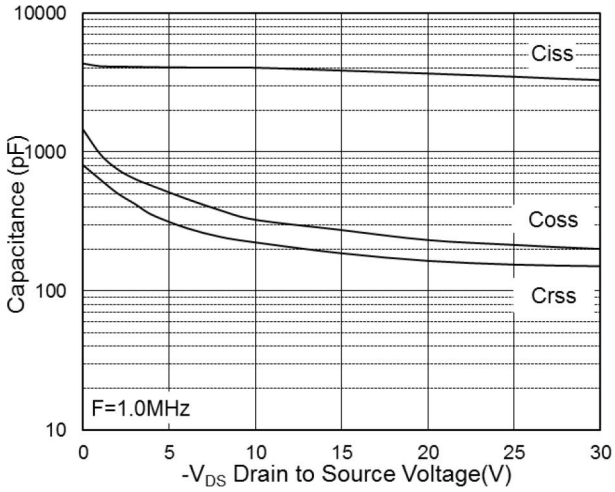


Fig.7 Capacitance

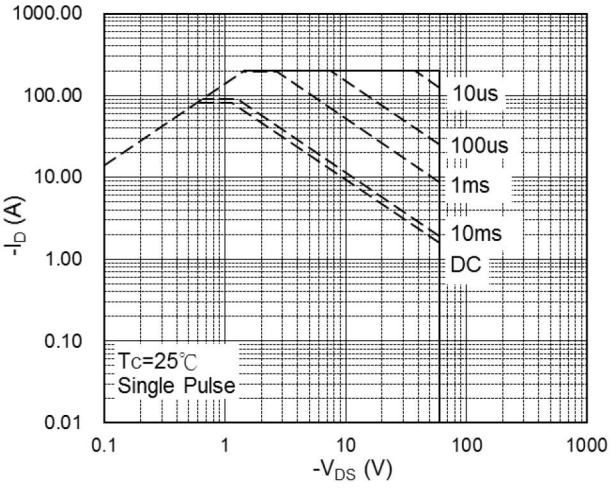


Fig.8 Safe Operating Area

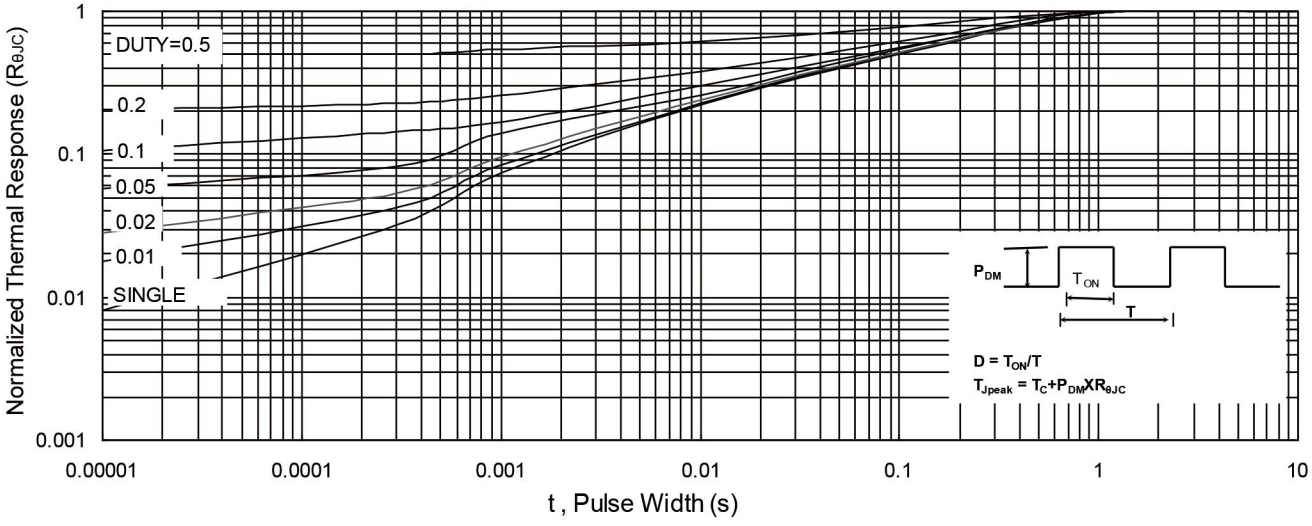


Fig.9 Normalized Maximum Transient Thermal Impedance

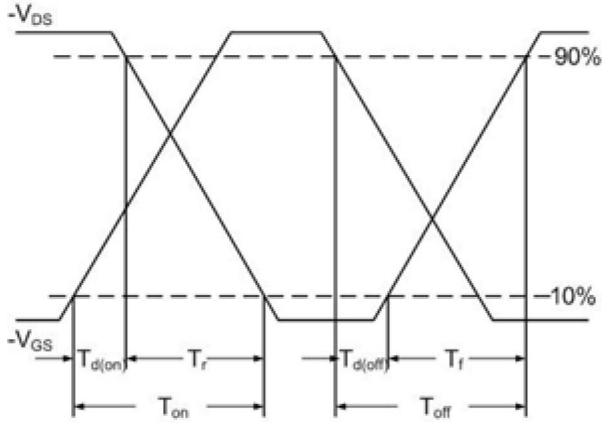


Fig.10 Switching Time Waveform

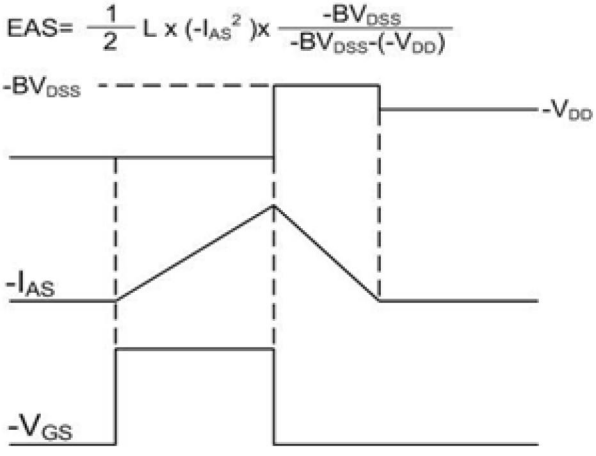
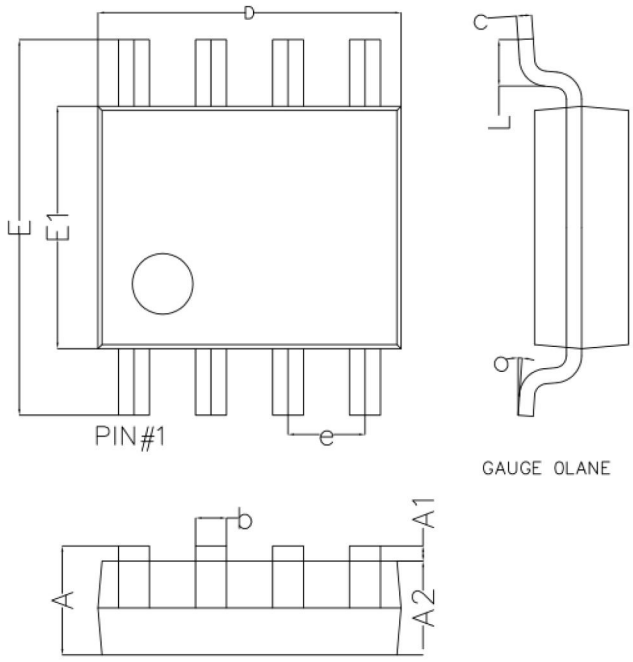


Fig.11 Unclamped Inductive Switching Waveform

SOP8 Package outline



Symbol	Dim in mm		
	Min	Nor	Max
A	1.350	1.550	1.750
A1	0.100	0.175	0.250
A2	1.350	1.450	1.550
b	0.330	0.420	0.510
c	0.170	0.210	0.250
D	4.800	4.900	5.000
e	1.270(BSC)		
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.400	0.835	1.2700
θ	0°	4°	8°