3A High Accuracy Ultra-Low Noise LDO Voltage Regulator

Features

- Ultra-Low Dropout Voltage: 85mV (TYP) at 3A Load
- 1.0% Accuracy Over Line, Load and Temperature
- Ultra-Low Output Noise: 6.5μV_{RMS} (TYP) Independent of Output Voltages
- Input Voltage Range:
  - With BIAS: 1.1V to 6.5V
  - Without BIAS: 1.4V to 6.5V
- Output Voltage Range:
  - Adjustable Operation: 0.8V to 5.15V
  - Pin-Programmable Operation: 0.8V to 3.95V
- High PSRR: 36dB at 1MHz
- Excellent Load Transient Responses
- Open-Drain Power-Good (PG) Output
- Thermal Shutdown and Over-Current Protection
- Stable with a 22μF or larger ceramic capacitor
- Operating Junction Temperature: -40°C to +125°C
- 3.5mm x 3.5mm 20-PIN VQFN Package

Applications

- Macro remote radio units (RRU)
- Outdoor backhaul units
- Active antenna system mMIMO (AAS)
- Ultrasound scanners
- Lab and field instrumentation
- Sensor, imaging, and radar

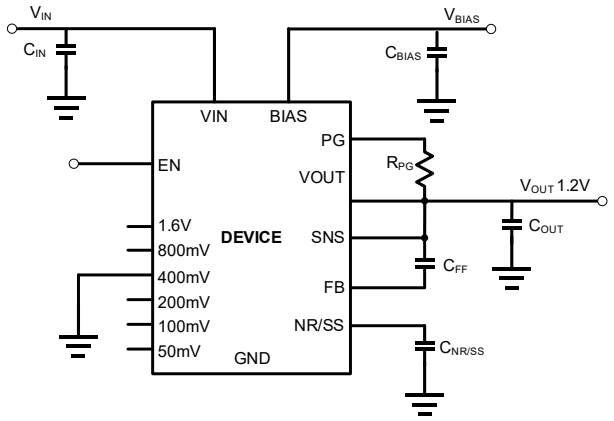
Description

The device is an ultra-low-noise (6.5μV_{RMS}), high PSRR, and high accuracy low-dropout (LDO) voltage regulator capable of sourcing 3A current. The output voltage can be set from 0.8V to 3.95V in pin-programmable operation and adjusted from 0.8V to 5.15V by using external resistor divider. The device has a wide input voltage range from 1.1V to 6.5V

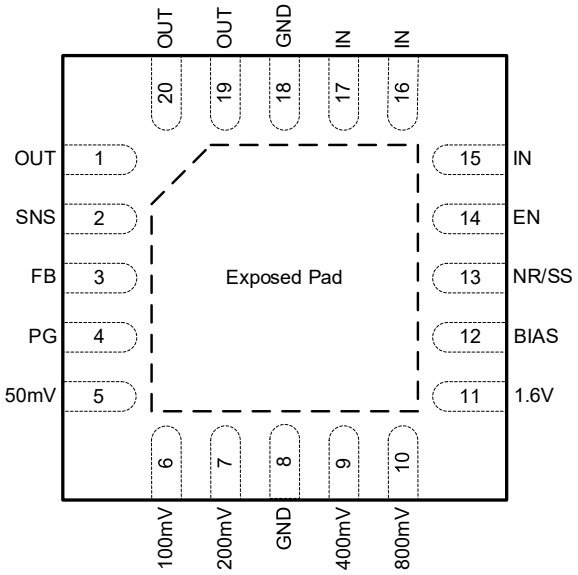
The combination of low-noise (6.5μV_{RMS}), high PSRR, and high output current capability makes this device ideal to power noise-sensitive components such as those found in high-speed communications, video, medical, or test and measurement applications. The high performance of this device limits power-supply-generated phase noise and clock jitter, making this device ideal for powering high performance serializer and deserializer (SerDes), analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and RF components. Specifically, RF amplifiers benefit from the high-performance and 5.0V output capability of the device.

For digital loads such as ASICs, FPGAs and DSPs requiring low-input voltage low-output voltage (LILO) operation, the exceptional accuracy, remote sensing, excellent transient performance, and soft-start capabilities of this device ensure the optimal system performance.

Typical Application Circuit



Pin Configuration and Functions



3.5mm x 3.5mm 20-Pin VQFN, Top View

Pin Descriptions

PIN Number	PIN Name	I/O	Function
1, 19, 20	OUT	O	Regulator output voltage pin. A 22µF or larger ceramic capacitor from OUT to ground is required to ensure regulator stability. The capacitor should be placed as close to the output as possible. Minimize the impedance from the OUT pin to the load.
2	SNS	I	Output voltage sense input pin. Connect this pin to the load side of the output trace if the pin-programmable feature is used. If the feature is not used, leave this pin floating.
3	FB	I	Feedback pin connected to the error amplifier. Although not required, a 10nF feed-forward capacitor from FB to OUT is recommended to maximize the regulator ac performance.
4	PG	O	Active-high, power-good pin. An open-drain output indicates when the output voltage reaches 88% of the target. A 10kΩ to 100kΩ external pullup resistor is required. This pin can be left floating or connected to GND if not used.
5	50mV	I	Pin-Programmable voltage setting pins. Connect these pins to ground, SNS, or leave floating. Connecting these pins to ground increases the output voltage, whereas connecting these pins to SNS increases the resolution of the pin-programmable network but decreases the range of the network; multiple pins can be simultaneously connected to ground or SNS to select the desired output voltage. Leave these pins floating (open) when not in use.
6	100mV		
7	200mV		
9	400mV		

10	800mV		
11	1.6V		
12	BIAS	I	BIAS supply voltage. This pin enables the use of low-input voltage, low-output voltage conditions (that is, V_{IN} = 1.2V, V_{OUT} = 1V) to reduce the power dissipation in the die. The use of a BIAS voltage improves dc and ac performance for Vin < 2.2V. A 10uF capacitor or larger must be connected between this pin and ground. If not used, this pin must be left floating or tied to ground.
8, 18	GND	-	Ground pin.
13	NR/SS	O	Noise reduction pin. A 100nF or larger capacitor from NR to GND is recommended to maximize the performance Enable pin.
14	EN	I	Enable pin. Drive EN high to turn on the LDO and drive the EN low to turn off the LDO. The EN pin can be connected to IN for automatic startup
15 – 17	IN	I	Input supply voltage pin. A 47μF or larger ceramic capacitor from IN to GND is recommended
-	Exposed Pad	-	Exposed Pad must be connected to a large-area ground plane to get maximum electrical and thermal performance.

Package/Ordering Information

DEVICE	PACKAGE TYPE	MARKING	PACKING OPTION
TPS7A8400RGRR	VQFN-20-EP(3.5x3.5)	11CI	Tape and Reel, 1000

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
IN, BIAS, PG and EN Pins	IN, BIAS, PG, EN	−0.3 to 7	V
SNS and OUT Pin	SNS, OUT	-0.3 to V_{IN} + 0.3	V
NR/SS and FB Pins	NR/SS, FB	-0.3 to V_{OUT} + 0.3	V
50mV, 100mV, 200mV, 400mV, 800mV, 1,6V		-0.3 to V_{OUT} + 0.3	V
Storage temperature range	T_{STG}	−65 to +150	°C
Output current	I_{OUT}	3	A

Notes:

1. Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

ESD Ratings

			Value	Unit
V_{ESD}	Electrostatic Discharge	HBM (Human Body Model)	3000	V
		CDM (Charge Device Model)	1000	

Recommended Operation Conditions

Over operating temperature range unless otherwise noted

Parameter	Symbol	Min	Max	Unit
Input Supply Voltage	V_{IN}	1.1	6.5	V
BIAS Supply Voltage	V_{BIAS}	3.0	6.5	V
Output Voltage	V_{OUT}	0.8	5.15	V
Output Capacitance	C_{OUT}	22		μF
Output Current	I_{OUT}	0	3	A
Operating Junction Temperature	T_J	-40	125	°C

Thermal Information

Package	$R_{\theta JA}$	$R_{\theta JC(Bottom)}$	Unit
3.5mmx3.5mm 20-PIN VQFN	45	6.5	°C/W

Electrical Characteristics

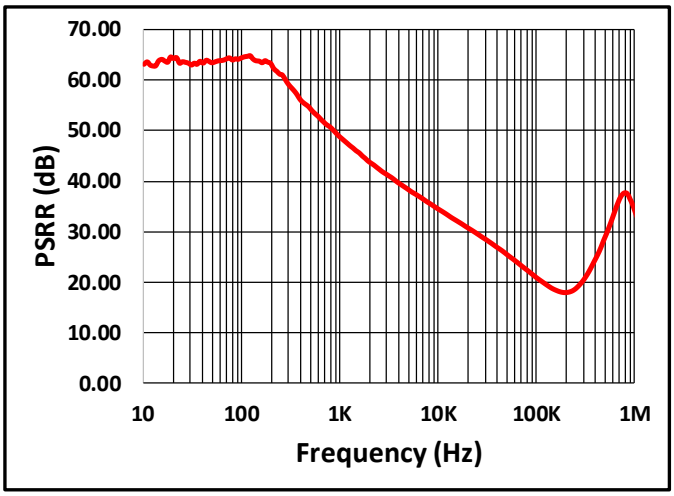
V_{IN} = 1.4V or V_{IN} = V_{OUT} + 0.4V (whichever is greater), V_{BIAS} = open, V_{OUT} = 0.8V, V_{EN} = 1.1V, C_{IN} = 10µF, C_{OUT} = 47µF, C_{NR} = 1µF, C_{FF} = open, PG pin pulled up to V_{IN} with 100 kΩ resistor, T_A = −40 to +125°C unless otherwise noted

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
Input Voltage	V_{IN}	With V_{BIAS}	1.1	-	6.5	V
		Without V_{BIAS}	1.4	-	6.5	V
Bias Supply Voltage	V_{BIAS}	V_{IN} = 1.1V	3.0	-	6.5	V
Reference Voltage	V_{REF}			0.8		V
Input Supply UVLO with BIAS	$V_{UVLO1(IN)}$	V_{IN} rising with V_{BIAS} = 3.0V		1.0		V
$V_{UVLO1(IN)}$ Hysteresis	$V_{HYS1(IN)}$	V_{BIAS} = 3.0V		110		mV
Input Supply UVLO without BIAS	$V_{UVLO1(IN)}$	V_{IN} rising		1.32		V
$V_{UVLO2(IN)}$ Hysteresis	$V_{HYS2(IN)}$			110		mV
BIAS Supply UVLO	$V_{UVLO(BIAS)}$	V_{BIAS} rising, V_{IN} = 1.1V		2.8		V
$V_{UVLO(BIAS)}$ Hysteresis	$V_{HYS(BIAS)}$	V_{IN} = 1.1V		110		mV
Output Voltage Accuracy		5mA ≤ I_{OUT} ≤ 3A	-1.0	0	1.0	%
GND Pin Current	I_{GND}	V_{IN} = 1.4V, V_{OUT} = 0.8V, I_{OUT} = 5mA		0.95		mA
		V_{IN} = 6.5V, V_{OUT} = 0.8V, I_{OUT} = 5mA		1.05		mA
Shutdown Current	I_{SHDN}	V_{IN} = 6.5V, V_{EN} = 0V			25	µA
BIAS Pin Current	I_{BIAS}	V_{IN} =1.1V, V_{BIAS} =6.5V, V_{OUT} = 0.8V, I_{OUT} = 3A, PG Floating		1.1		mA
Dropout Voltage	V_{DO}	V_{IN} = 1.4V, I_{OUT} = 3A, V_{FB} = 0.8 – 3%		95		mV
		V_{IN} = 5.4V, I_{OUT} = 3A, V_{FB} = 0.8 – 3%		102		mV
		V_{IN} = 1.1V, V_{BIAS} = 5.0V, I_{OUT} = 3A, V_{FB} = 0.8 – 3%		85		mV
Output Current Limit	I_{LIM}	V_{OUT} forced at 0.9 x $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 0.4V		4.8		A
Line Regulation	ΔV_{OUT} /ΔV_{IN}	V_{IN} = 1.4 – 6.5V, I_{OUT} = 5mA		0.01		mV/V
Load Regulation	ΔV_{OUT} /ΔI_{OUT}	V_{IN} = 1.1V, V_{BIAS} = 3 – 6.5V, I_{OUT} = 5mA to 3A,		0.3		mV/A
EN pin low-level input voltage (device disabled)	$V_{IL(EN)}$		0		0.5	V

EN pin high-level input voltage (device enabled)	$V_{IH(EN)}$		1.1		6.5	V
EN PIN Leakage Current	I_{EN}	V_{IN} = 6.5V, 0V ≤ V_{EN} ≤ 6.5V	-0.2		0.2	µA
FB PIN Leakage Current	I_{FB}	V_{IN} = 6.5V, V_{FB} = 0.8V	-0.2		0.2	µA
PG Pin Threshold	V_{PG}	V_{OUT} Falling, PG Transitioning Low Expressed as a Percentage of $V_{OUT(TARGET)}$		88%		
PG Pin Hysteresis	$V_{hys(PG)}$	V_{OUT} Rising, PG Transitioning High Expressed as a Percentage of $V_{OUT(TARGET)}$		1.2%		
PG Pin Low Level Output Voltage	$V_{OL(PG)}$	V_{OUT} < V_{PG}, Source 1mA to PG Pin			0.4	V
PG Pin Leakage Current	I_{PG}	V_{OUT} > V_{PG}, Apply 6.5V to PG Pin			1	µA
Power Supply Ripple Rejection	PSRR	V_{IN} - V_{OUT} = 0.4V, I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, C_{NR} = 1µF, C_{FF} = 10nF; f = 10kHz, V_{OUT} = 0.8V, V_{BIAS} = 5.0V		48		dB
		f = 500kHz, V_{OUT} = 0.8V, V_{BIAS} = 5.0V		38		
		f = 10kHz, V_{OUT} =5.0V		41		
		f = 500kHz, V_{OUT} =5.0V		26		
Output Noise Voltage	V_N	BW = 10Hz to 100kHz, V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, C_{NR} = 1µF, C_{FF} = 10nF		6.5		μV_{RMS}
Thermal Shutdown Temperature	TSD			160		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

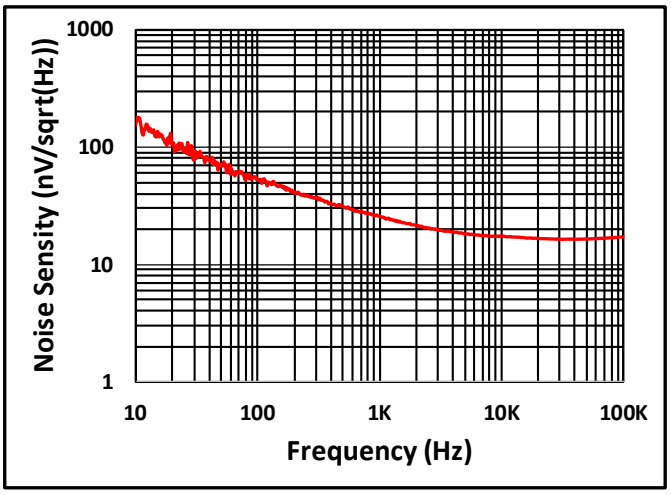
Typical Characteristics

V_{IN} = 1.4V or V_{IN} = V_{OUT} + 0.4V (whichever is greater), V_{BIAS} = open, V_{OUT} = 0.8V, V_{EN} = 1.1V, C_{IN} = 10µF, C_{OUT} = 47µF, C_{NR} = 1µF, C_{FF} = open, T_A = −40 to +125°C unless otherwise noted



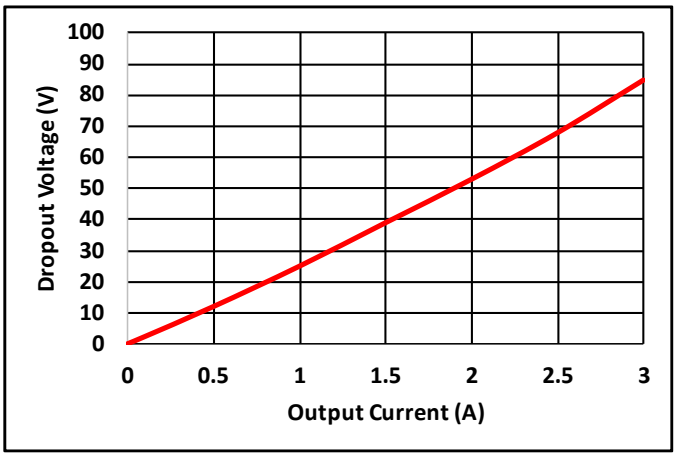
V_{IN} = 4V, V_{BIAS} = open, V_{OUT} = 3.3V, I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, C_{NR} = 1µF, C_{FF} = open

Fig. 1 PSRR



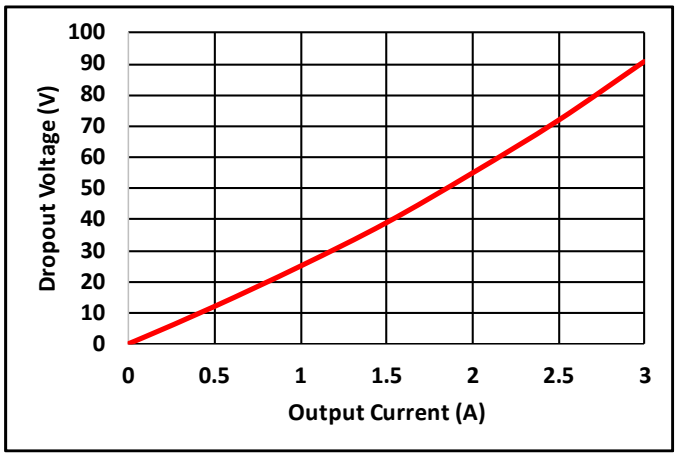
V_{IN} = 4V, V_{BIAS} = open, V_{OUT} = 3.3V, I_{OUT} = 3A, C_{OUT} = 47µF || 10µF || 10µF, C_{NR} = 1µF, C_{FF} = open

Fig. 2 Output Noise Density



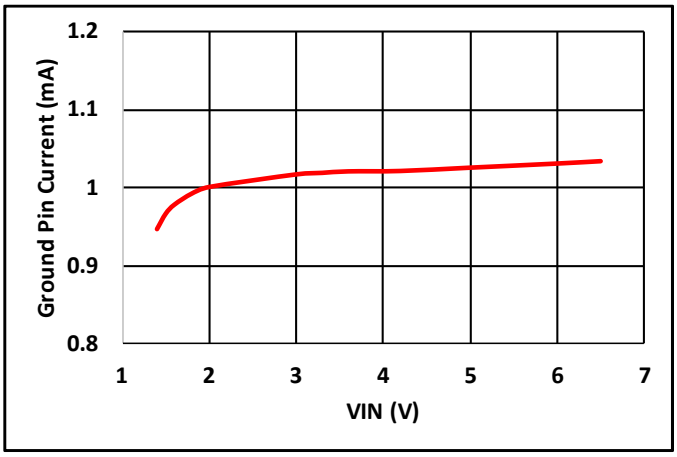
V_{IN} = 1.1V, V_{BIAS} = 3.3V

Fig. 3 Dropout Voltage with BIAS



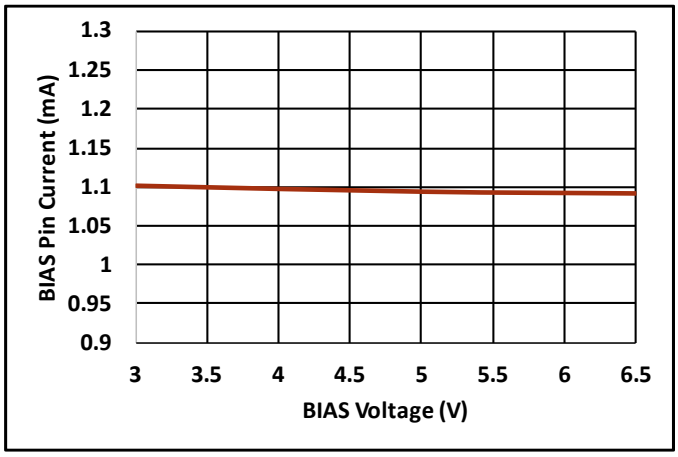
V_{IN} = 1.4V, V_{BIAS} = 0V

Fig. 4 Dropout Voltage without BIAS



V_{BIAS} = 0V, I_{OUT} = 5mA

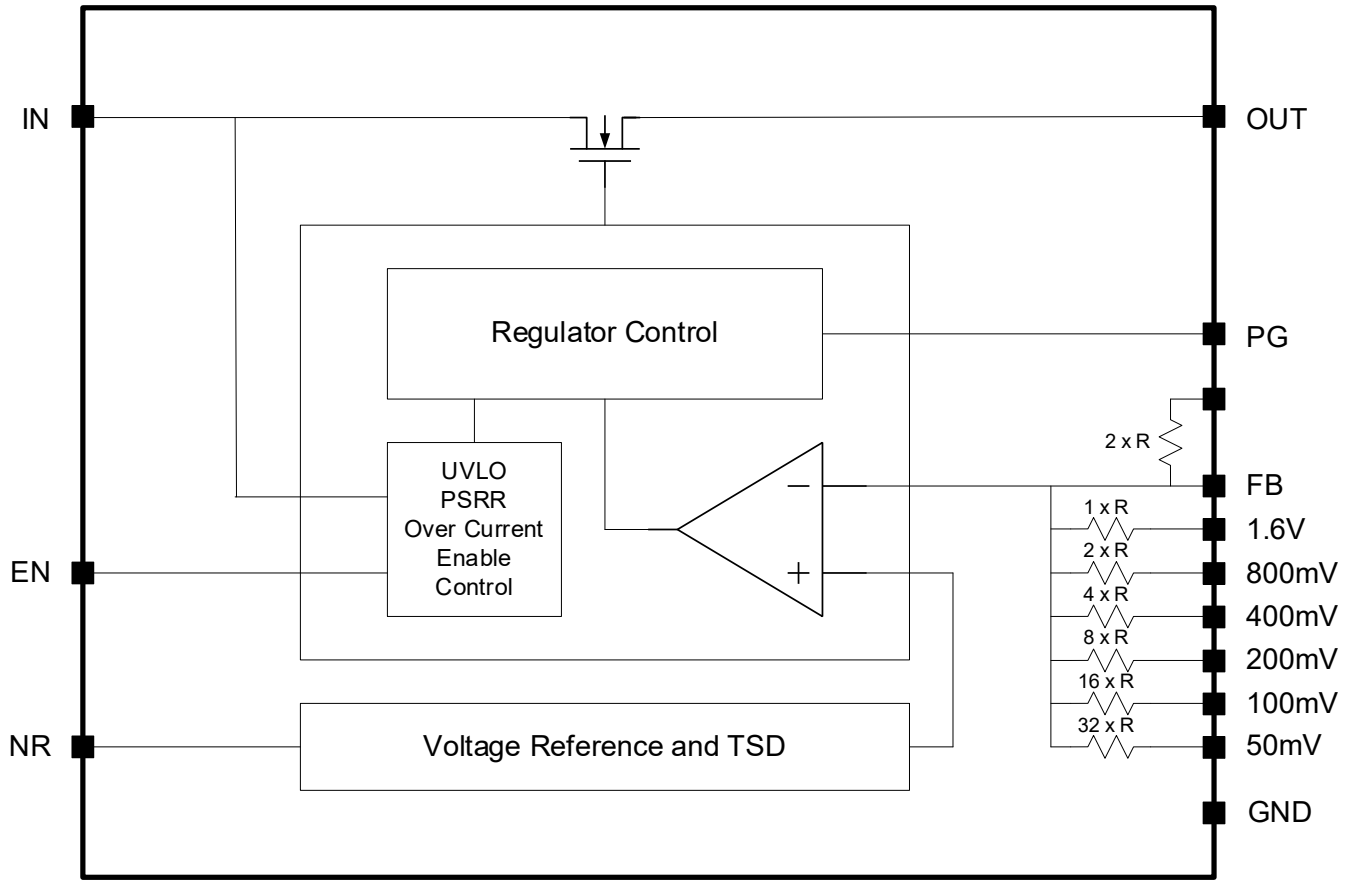
Fig. 5 Ground Current vs Input Voltage



V_{IN} = 1.1V, I_{OUT} = 5mA, PG Floating

Fig. 6 BIAS Pin Current vs BIAS Voltage

Functional Block Diagram



Feature Description

Enable

The enable pin for the device is active high. The device is enabled when the enable pin voltage is greater than $V_{IH(EN)}$ and disabled with the enable pin voltage less than $V_{IL(EN)}$. If independent control of chip enable is not needed, then connect the enable pin to the input. The device has an internal pulldown MOSFET that connects a discharge resistor from VOUT to ground when the device is disabled to actively discharge the output voltage.

Integrated Resistance Network (Pin-Programmable Output)

In internal feedback resistance network is provided, allowing the device output voltage to be programmed easily between 0.8V to 3.95V with a 50mV step by tying the programmable pins to ground. Tying the programmable pins to SNS increases the resolution but limits the range of the output voltage. Excellent accuracy across output voltage and temperature can be achieved using the integrated resistance network.

Bias Rail

The device features a bias rail to enable low-input voltage, low-output (LILO) voltage operation by providing power to the internal circuitry of the device. The bias rail is required for operation with V_{IN} < 1.4V.

Internal Current Limit

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. During a current-limit event, the LDO sources constant current; therefore, the output voltage falls with decreased load impedance. Thermal shutdown can activate during a current limit event because of the high power dissipation typically found in these conditions. To ensure proper operation of the current limit, minimize the inductances to the input and load. Continuous operation in current limit is not recommended.

Output Voltage Accuracy

Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent. The device features an output voltage accuracy of 2% that includes the errors introduced by the internal reference, load regulation, and line regulation variance across the full range of rated load and the line operating conditions over temperature.

Undervoltage Lockout (UVLO)

The device uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

Power-Good Function

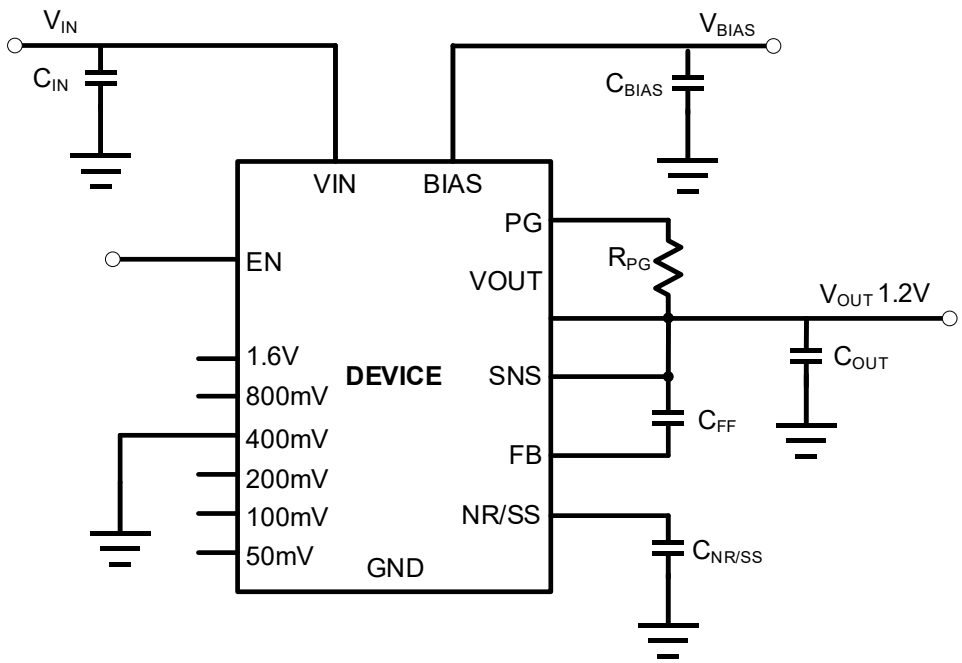
The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the feedback pin voltage falls below the PG threshold voltage, the PG pin open-drain output engages and pulls the PG pin close to ground. When the feedback voltage exceeds the threshold by an amount greater than $V_{HYS(PG)}$, the PG pin becomes high impedance. By connecting a pullup resistor to an external supply, and downstream device can receive power-good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices. Using a pullup resistor from 10kΩ to 100kΩ is recommended.

Thermal Protection

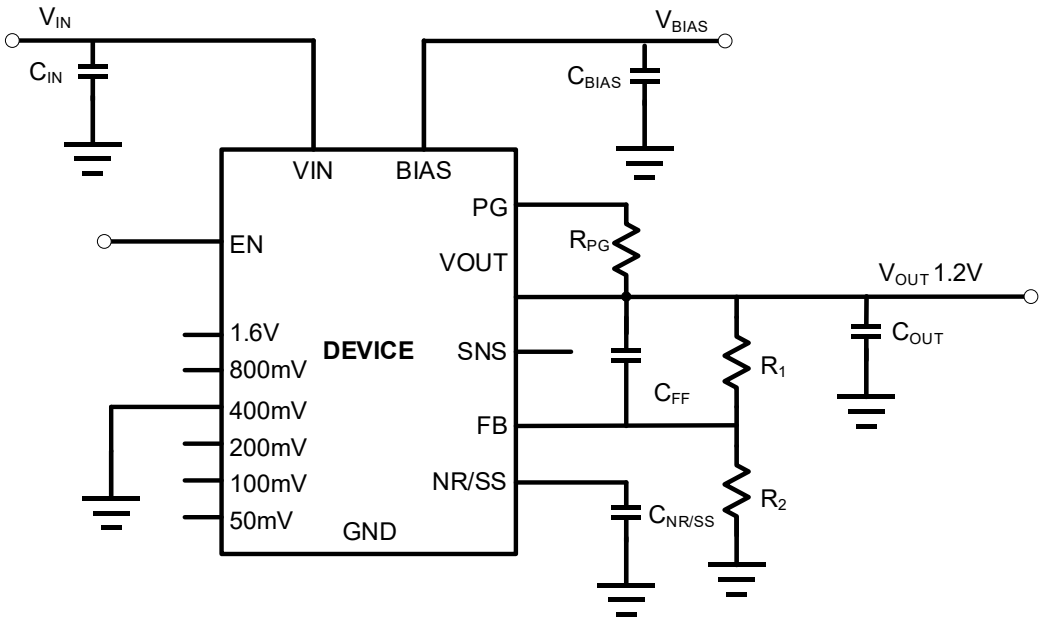
The device contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO.

Application Information

Typical Application for Pin-Programmable Output Voltage



Typical Application for Adjustable Output Voltage



Input Capacitor and Output Capacitor

The device is designed and characterized for operation with ceramic capacitors of 10μF or greater at the input and 22μF or greater at the output. Locate the input and output capacitors as near as practical to the input and output pins to minimize the trace inductance from the capacitor to the device.

Feed-Forward Capacitor (C_{FF})

Although a feed-forward capacitor (C_{FF}), from the FB pin to the OUT pin is not required to achieve stability, a 10nF, feed-forward capacitor improves noise and PSRR performance.

Pin-Programmable Output Voltage

The output voltage of the device can be set by the internally-matched pin-programmable feedback resistor network. Each of the programmable pins from 5 to 11 can be connected to ground (active) or left open (floating), or connected to SNS. The output is set as the internal reference voltage by Equation 1 plus the accumulated sum of the respective voltages assigned to each active pin.

$$V_{OUT} = 0.8V + (\Sigma\, Programmable\ Pins\ to\ Ground) \quad (1)$$

Table 1. Pin-Programmable Output Voltage

PROGRAMMABLE PINS (Active Low)	ADDITIVE OUTPUT VOLTAGE LEVEL
Pin 5 (50mV)	50mV
Pin 6 (100mV)	100mV
Pin 7 (200mV)	200mV
Pin 9 (400mV)	400mV
Pin 10 (800mV)	800mV
Pin 11 (1.6V)	1.6V

The voltage setting pins have a binary weight; therefore the output voltage can be programmed to any value from 0.8V to 3.95V in 50mV steps when tying these pins to ground. As with the adjustable operation, the output voltage is set according to Equation 2 except that R1 and R2 are internally integrated and matched for higher accuracy. Tying any of the programmable pins to SNS can increase the resolution of the internal feedback network by lowering the value of R1.

Adjustable Output Voltage

The output voltage of the device can be adjusted from 0.8V to 5.2V according to the following equation.

$$V_{OUT} = 0.8V \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

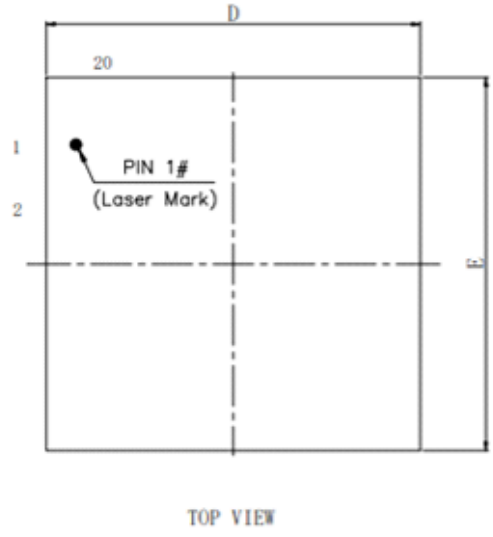
The table below lists the resistor combination required to achieve a few of the most common rails using commercially available, 0.1%-tolerance resistors.

Table 2. Adjustable Output Voltage

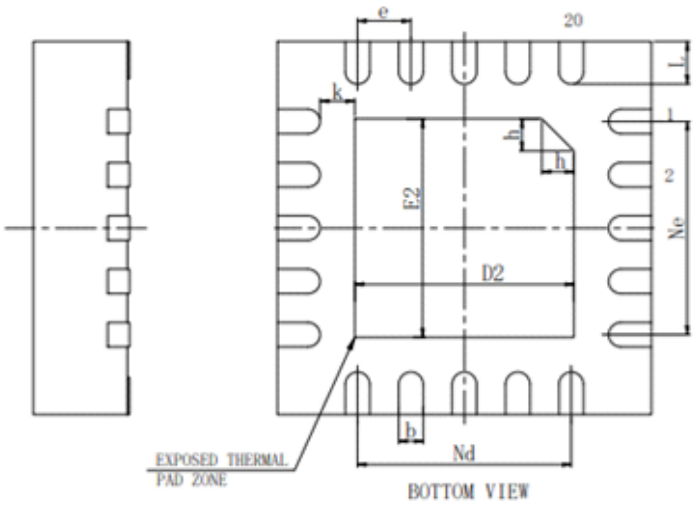
VOUT(TARGET) (V)	FEEDBACK RESISTOR VALUES		CALCULATED OUTPUT VOLTAGE (V)
	R1 (kΩ)	R2 (kΩ)	
0.8	Short	Open	0.800
1.00	12.4	49.9	0.999
1.20	12.4	24.9	1.198
1.50	12.4	14.3	1.494
1.80	12.4	10	1.798
2.50	12.4	5.9	2.48
3.00	12.1	4.42	2.990
3.30	11.8	3.74	3.324
5.00	12.4	2.37	4.985

PACKAGE OUTLINE DIMENSIONS

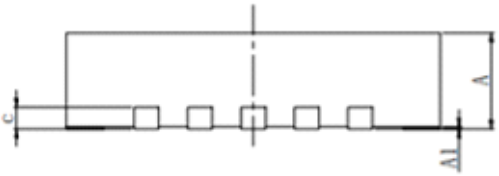
VQFN-20-EP(3.5x3.5)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.06
b	0.18	0.23	0.30
c		0.203REF	
D	3.40	3.50	3.60
D2	1.95	2.05	2.15
e		0.50BSC	
Nd		2.00BSC	
E	3.40	3.50	3.60
E2	1.95	2.05	2.15
Ne		2.00BSC	
L	0.35	0.40	0.45
K	0.275	0.325	0.375
h	0.25	0.30	0.35