

## 2channel MOSFET Drive Switching Regulator IC for Buck Converter

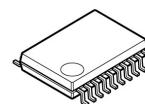
### ■ GENERAL DESCRIPTION

The **NJW4162A** is a 2 channel MOSFET Drive switching regulator IC for buck converter that operates wide input voltage range from 4.3V to 40V. The oscillating frequency range can set within 100kHz to 1MHz by external resistor. It also has an external synchronous function.

It has individual Standby functions, Soft Start functions and Power Good functions for each channel, therefore a start-up control and/or operating condition monitoring are available with a microcomputer.

The **NJW4162A** is suitable for a logic voltage generating circuit from high input voltage such as Automotive. Office Automation and Industrial applications.

### ■ PACKAGE OUTLINE



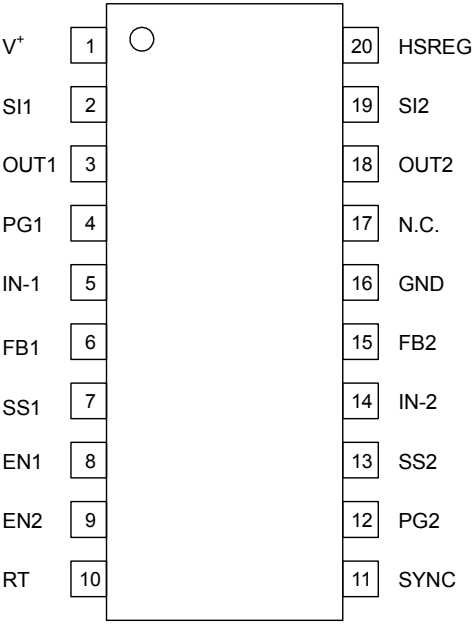
**NJW4162AVC3**

### ■ FEATURES

- Pch MOSFET Driving                      Driving Voltage  $V^+$ -10V(typ.)
- Maximum Rating Input Voltage        45V
- Wide Operating Voltage Range        4.3V to 40V
- PWM Control
- Maximum Duty Cycle 100%
- Wide Oscillating Frequency Range    100kHz to 1MHz
- External Synchronization Function    1,500kHz (max.)
- Anti-Phase switching
- Adjustable Soft Start Function
- UVLO (Under Voltage Lockout)
- Over Current Protection (Hiccup type)
- Thermal Shutdown Protection
- Standby Function
- Power Good Function
- Package Outline                            NJW4162AVC3 : SSOP20-C3

# NJW4162A

## PIN CONFIGURATION

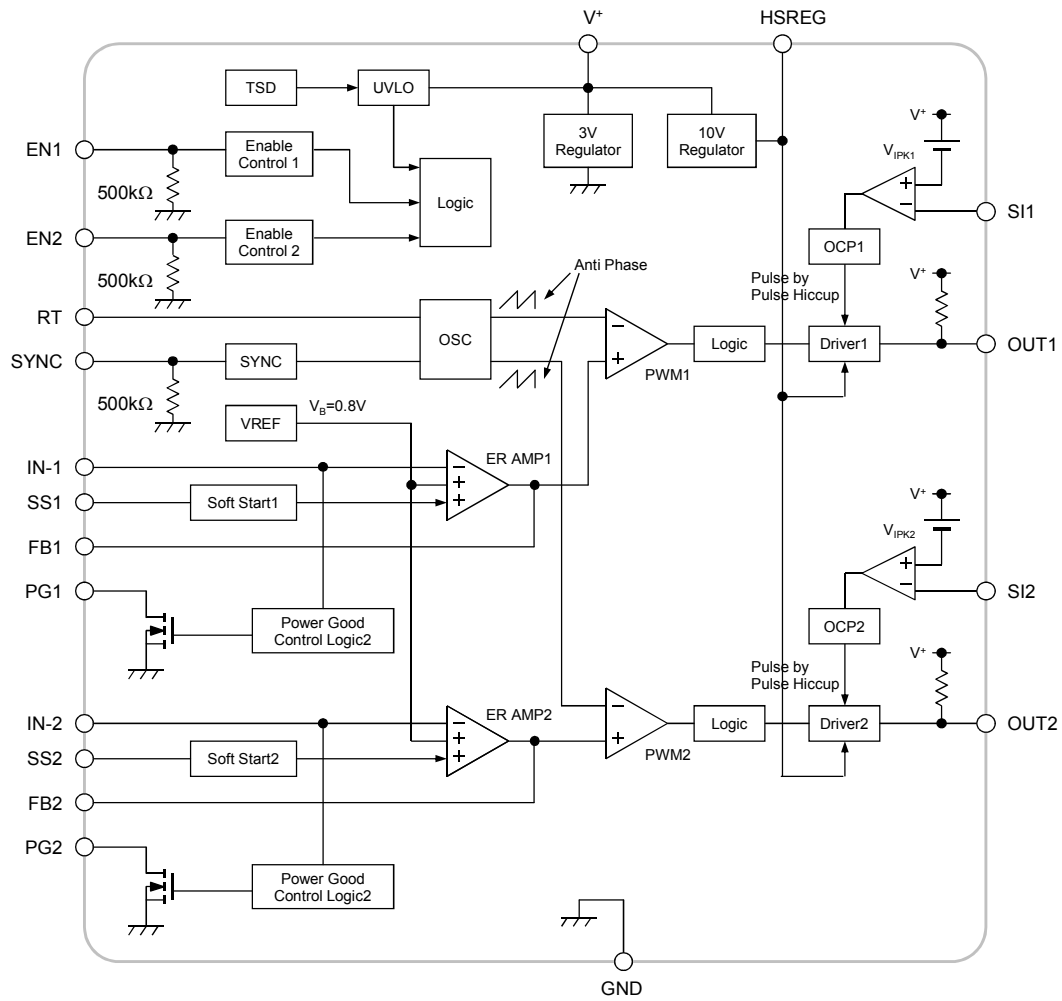


(Top View)  
**NJW4162AVC3**

## ■ PIN DESCRIPTIONS

| PIN NAME       | PIN NUMBER | FUNCTION                                                                                                                                                                                                                                                                                           |
|----------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sup>+</sup> | 1          | Power Supply pin                                                                                                                                                                                                                                                                                   |
| SI1<br>SI2     | 2<br>19    | Current Sensing pin<br>When voltage difference between the V <sup>+</sup> pin and the SI pin exceeds 150mV(typ.), over current protection operates.                                                                                                                                                |
| OUT1<br>OUT2   | 3<br>18    | Output pin for Power MOSFET Driving<br>The OUT pin Voltage is clamped with V <sup>+</sup> -10V(typ.) at the time of Low level, in order to protect a gate of Pch MOSFET.                                                                                                                           |
| PG1<br>PG2     | 4<br>12    | Power Good pin. An open drain output that goes high impedance when the IN- pin voltage is stable around $\pm 10\%$ .                                                                                                                                                                               |
| IN-1<br>IN-2   | 5<br>14    | Output Voltage Detecting pin<br>Connects output voltage through the resistor divider tap to this pin in order to voltage of the IN- pin become 0.8V.                                                                                                                                               |
| FB1<br>FB2     | 6<br>15    | Feedback Setting pin<br>The feedback resistor and capacitor are connected between the FB pin and the IN- pin.                                                                                                                                                                                      |
| SS1<br>SS2     | 7<br>13    | Soft Start timer setting pin.<br>Soft start time is controlled by a capacitor.                                                                                                                                                                                                                     |
| EN1<br>EN2     | 8<br>9     | Standby Control pin<br>The EN pin internally pulls down with 500k $\Omega$ . Normal Operation at the time of High Level. Standby Mode at the time of Low Level or OPEN.                                                                                                                            |
| RT             | 10         | Oscillating Frequency Setting pin by Timing Resistor.<br>Oscillating Frequency should set between 100kHz and 1MHz.                                                                                                                                                                                 |
| SYNC           | 11         | External Clock Input pin. The SYNC pin internally pulls down with 500k $\Omega$ .<br>It operates by inputting clock signal at the oscillatory frequency that synchronized with the input signal.<br>When not using the external synchronization function, make the SYNC pin the Low level or open. |
| GND            | 16         | GND pin                                                                                                                                                                                                                                                                                            |
| N.C.           | 17         | Non Connection                                                                                                                                                                                                                                                                                     |
| HSREG          | 20         | Output pin of the high side regulator.<br>Connect a bypass capacitor to stabilize a driver circuit.                                                                                                                                                                                                |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

| PARAMETER                   | SYMBOL         | MAXIMUM RATINGS                 | UNIT |
|-----------------------------|----------------|---------------------------------|------|
| Supply Voltage              | $V^+$          | -0.3 to +45                     | V    |
| OUT1,2 pin Voltage          | $V_{OUT1,2}$   | $V^+ - 11$ to $V^+$ (*1)        | V    |
| EN1,2 pin Voltage           | $V_{EN1,2}$    | -0.3 to +45                     | V    |
| IN-1,2 pin Voltage          | $V_{IN-1,2}$   | -0.3 to +6                      | V    |
| Power Good1,2 pin Voltage   | $V_{PG1,2}$    | -0.3 to +6                      | V    |
| SYNC pin Voltage            | $V_{SYNC}$     | -0.3 to +6                      | V    |
| OUT pin Peak Current        | $I_{O\ PEAK+}$ | 1,000 (Source)                  | mA   |
|                             | $I_{O\ PEAK-}$ | 1,000 (Sink)                    | mA   |
| Power Dissipation           | $P_D$          | SSOP20 1,000 (*2)<br>1,500 (*3) | mW   |
| Junction Temperature Range  | $T_j$          | -40 to +150                     | °C   |
| Operating Temperature Range | $T_{opr}$      | -40 to +125                     | °C   |
| Storage Temperature Range   | $T_{stg}$      | -50 to +150                     | °C   |

(\*1): When Supply voltage is less than +11V, the absolute maximum rating is -0.3 to  $V^+$ .

(\*2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(\*3): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers),

internal Cu area: 74.2×74.2mm

## ■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER                  | SYMBOL      | MIN.                 | TYP. | MAX.       | UNIT |
|----------------------------|-------------|----------------------|------|------------|------|
| Supply Voltage             | $V^+$       | 4.3                  | —    | 40         | V    |
| Timing Resistor            | $R_T$       | 4.3                  | —    | 56         | kΩ   |
| Oscillating Frequency      | $f_{OSC}$   | 100                  | —    | 1,000      | kHz  |
| Power Good pin Voltage     | $V_{PG}$    | 0                    | —    | 5.5        | V    |
| External Clock Input Range | $f_{SYNC}$  | $f_{OSC} \times 1.1$ | —    | 1,500 (*4) | kHz  |
| HSREG Capacitor            | $C_{HSREG}$ | 0.01                 | 0.22 | 1          | μF   |

(\*4): Use the external synchronization frequency in the range below x2 of internal oscillating frequency

(Maximum: 1.5 MHz).

## ■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted,  $V^+=V_{EN}=12V$ ,  $R_T=10k\Omega$ , Common to CH1 and CH2,  $T_a=25^\circ C$ )

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-----------|--------|----------------|------|------|------|------|
|-----------|--------|----------------|------|------|------|------|

### Under Voltage Lockout Block

|                       |              |                       |      |      |      |    |
|-----------------------|--------------|-----------------------|------|------|------|----|
| ON Threshold Voltage  | $V_{T\_ON}$  | $V^+=L \rightarrow H$ | 4.00 | 4.15 | 4.30 | V  |
| OFF Threshold Voltage | $V_{T\_OFF}$ | $V^+=H \rightarrow L$ | 3.85 | 4.00 | 4.15 | V  |
| Hysteresis Voltage    | $V_{HYS}$    |                       | 100  | 150  | —    | mV |

### Soft Start Block

|                |           |  |   |   |    |         |
|----------------|-----------|--|---|---|----|---------|
| Charge Current | $I_{CHG}$ |  | 6 | 8 | 10 | $\mu A$ |
|----------------|-----------|--|---|---|----|---------|

### Oscillator Block

|                                       |                |                                |     |     |     |     |
|---------------------------------------|----------------|--------------------------------|-----|-----|-----|-----|
| Oscillating Frequency                 | $f_{OSC}$      | $V_{IN}=0.75V$ , $V_{FB}=0.7V$ | 450 | 500 | 550 | kHz |
| Oscillating Frequency<br>OCP operates | $f_{OSC\_LIM}$ | $V_{IN}=0.55V$ , $V_{FB}=0.7V$ | —   | 125 | —   | kHz |

### Error Amplifier Block

|                       |           |                              |       |     |       |         |
|-----------------------|-----------|------------------------------|-------|-----|-------|---------|
| Reference Voltage     | $V_B$     |                              | -1.0% | 0.8 | +1.0% | V       |
| Input Bias Current    | $I_B$     |                              | -0.1  | —   | 0.1   | $\mu A$ |
| Output Source Current | $I_{OM+}$ | $V_{FB}=0V$ , $V_{IN}=0.75V$ | 16    | 32  | 48    | $\mu A$ |
| Output Sink Current   | $I_{OM-}$ | $V_{FB}=1V$ , $V_{IN}=0.9V$  | 1     | 2   | 4     | mA      |

### PWM Compare Block

|                    |                 |                |     |   |   |   |
|--------------------|-----------------|----------------|-----|---|---|---|
| Maximum Duty Cycle | $M_{AX}D_{UTY}$ | $V_{IN}=0.75V$ | 100 | — | — | % |
|--------------------|-----------------|----------------|-----|---|---|---|

### Output Block

|                                    |                |                     |          |          |         |          |
|------------------------------------|----------------|---------------------|----------|----------|---------|----------|
| Output High Level<br>ON Resistance | $R_{OH}$       | $I_O = -50mA$       | —        | 2        | 4       | $\Omega$ |
| Output Low Level<br>ON Resistance  | $R_{OL}$       | $I_O = +50mA$       | —        | 2        | 4       | $\Omega$ |
| HSREG Output Current               | $I_O\_{HSREG}$ | HSREG pin= $V^+-8V$ | 100      | 150      | —       | mA       |
| Output pin Limiting Voltage        | $V_{OLIM}$     |                     | $V^+-11$ | $V^+-10$ | $V^+-9$ | V        |

### Enable Control Block

|                      |                  |                          |     |     |       |           |
|----------------------|------------------|--------------------------|-----|-----|-------|-----------|
| ON Control Voltage   | $V_{ON}$         | $V_{EN}=L \rightarrow H$ | 1.9 | —   | $V^+$ | V         |
| OFF Control Voltage  | $V_{OFF}$        | $V_{EN}=H \rightarrow L$ | 0   | —   | 0.5   | V         |
| Pull-down Resistance | $R_{PD\_ON/OFF}$ | $I_{EN}=5\mu A$          | —   | 500 | —     | $k\Omega$ |

### Current Limit Detection Block

|                                    |             |  |     |     |     |    |
|------------------------------------|-------------|--|-----|-----|-----|----|
| Current Limit Detection<br>Voltage | $V_{IPK}$   |  | 139 | 150 | 161 | mV |
| Delay Time                         | $t_{DELAY}$ |  | —   | 100 | —   | ns |

## ■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted,  $V^+=V_{EN}=12V$ ,  $R_T=10k\Omega$ , Common to CH1 and CH2,  $T_a=25^\circ C$ )

| PARAMETER                    | SYMBOL         | TEST CONDITION | MIN. | TYP. | MAX. | UNIT     |
|------------------------------|----------------|----------------|------|------|------|----------|
| Power Good Block             |                |                |      |      |      |          |
| High Level Detection Voltage | $V_{THH\ PG}$  |                | 107  | 110  | 115  | %        |
| Low Level Detection Voltage  | $V_{THL\ PG}$  |                | 85   | 90   | 93   | %        |
| Hysteresis Region            | $V_{HYS\ PG}$  |                | —    | 2    | —    | %        |
| Power Good ON Resistance     | $R_{ON\ PG}$   | $I_{PG}=10mA$  | —    | 100  | —    | $\Omega$ |
| Leak Current at OFF State    | $I_{LEAK\ PG}$ | $V_{PG}=6V$    | —    | —    | 0.1  | $\mu A$  |

## External Synchronization Block

|                        |                 |  |     |     |     |           |
|------------------------|-----------------|--|-----|-----|-----|-----------|
| High Threshold Voltage | $V_{THH\ SYNC}$ |  | 1.6 | —   | 5.5 | V         |
| Low Threshold Voltage  | $V_{THL\ SYNC}$ |  | 0   | —   | 0.5 | V         |
| Pull-down Resistance   | $R_{PD\ SYNC}$  |  | —   | 500 | —   | $k\Omega$ |

## General Characteristics

|                   |               |                                            |   |   |    |         |
|-------------------|---------------|--------------------------------------------|---|---|----|---------|
| Quiescent Current | $I_{DD}$      | $R_L=no\ load, V_{IN-}=0.75V, V_{FB}=0.7V$ | — | 4 | 6  | mA      |
| Standby Current   | $I_{DD\ STB}$ | $V_{EN1,2}=0V$                             | — | — | 10 | $\mu A$ |

## ■ THERMAL CHARACTERISTICS

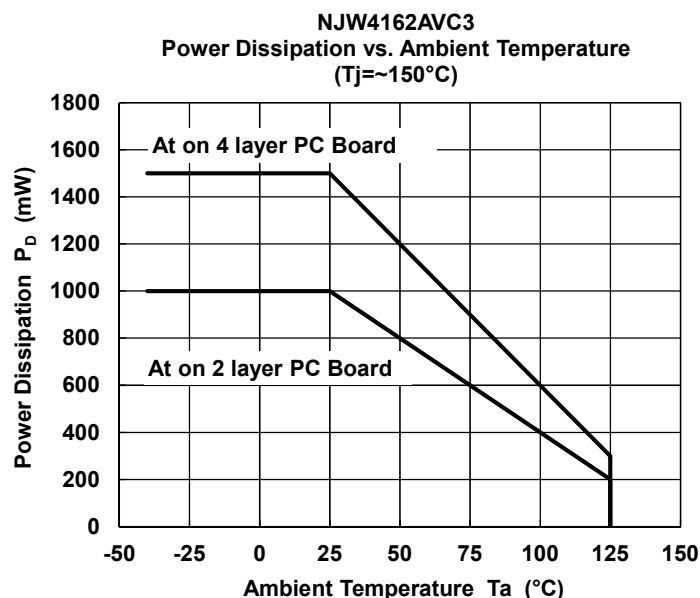
| PARAMETER                                             | SYMBOL        | VALUE    | UNIT         |
|-------------------------------------------------------|---------------|----------|--------------|
| Junction-to-ambient thermal resistance                | $\theta_{ja}$ | 125 (*4) | $^\circ C/W$ |
|                                                       |               | 83 (*5)  |              |
| Junction-to-Top of package characterization parameter | $\psi_{jt}$   | 13 (*4)  | $^\circ C/W$ |
|                                                       |               | 9 (*5)   |              |

(\*4): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

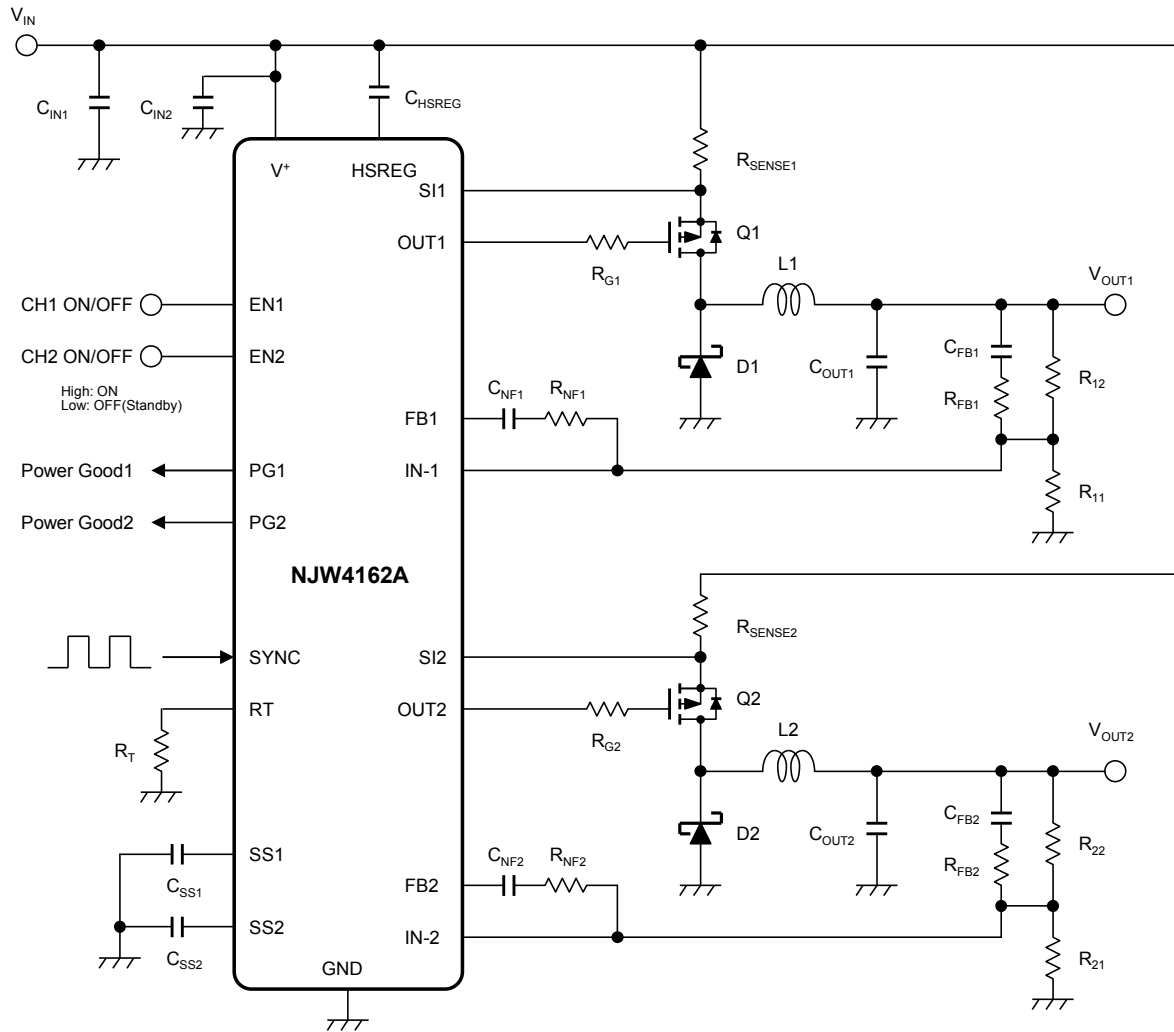
(\*5): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers),

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## ■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

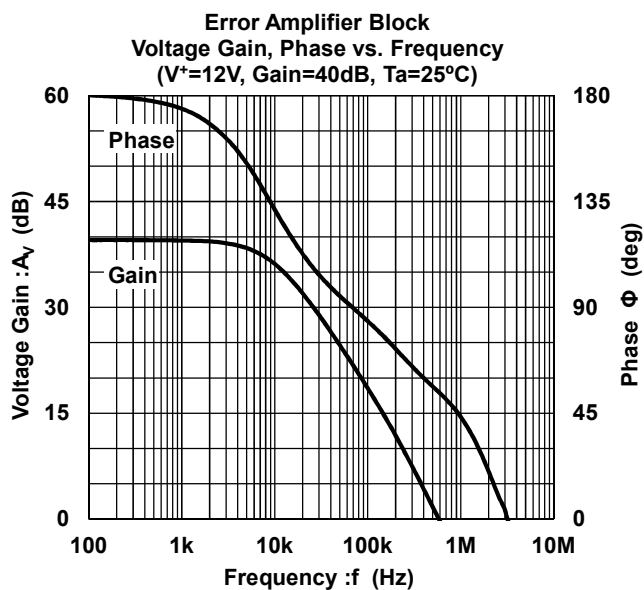
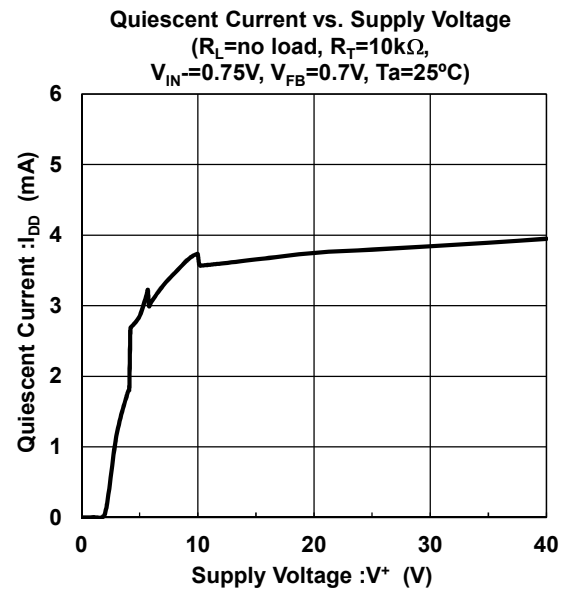
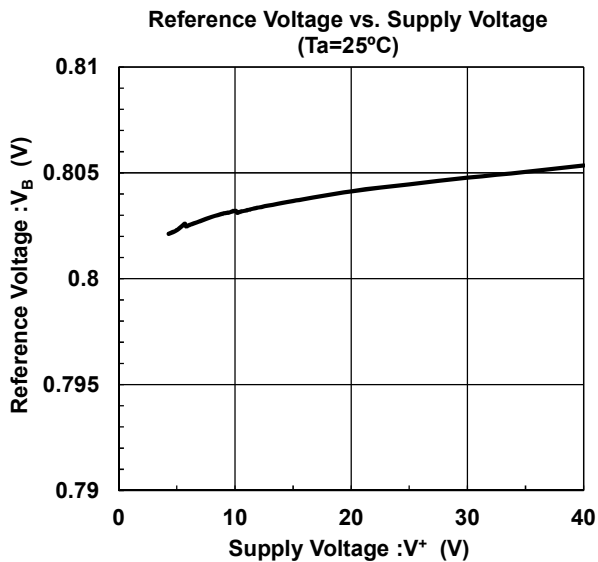
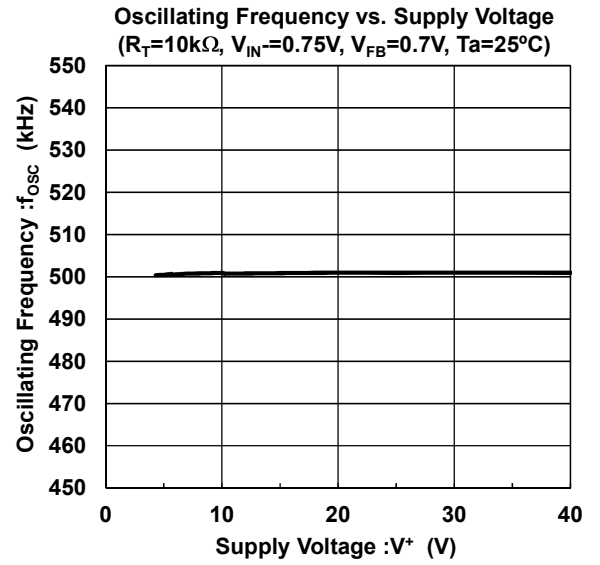
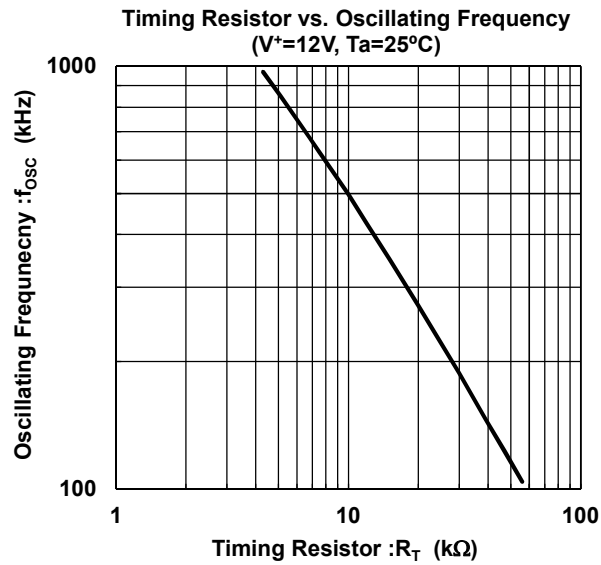


## ■ TYPICAL APPLICATIONS

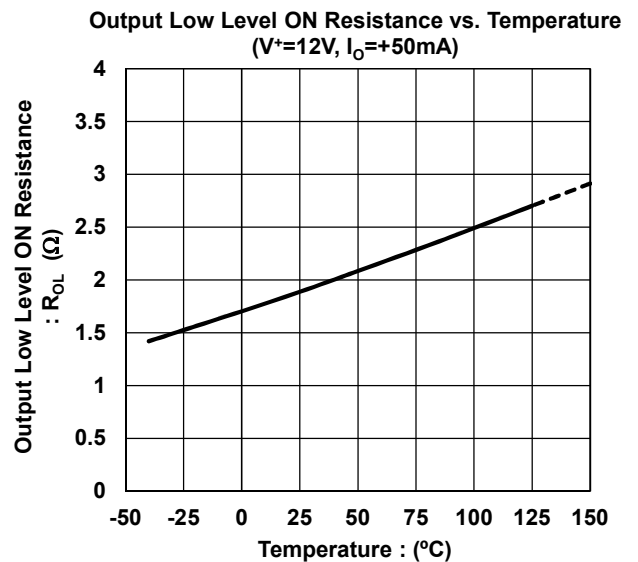
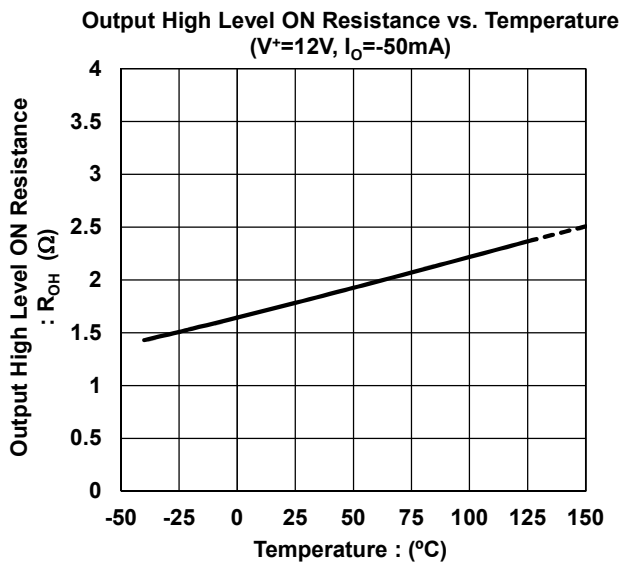
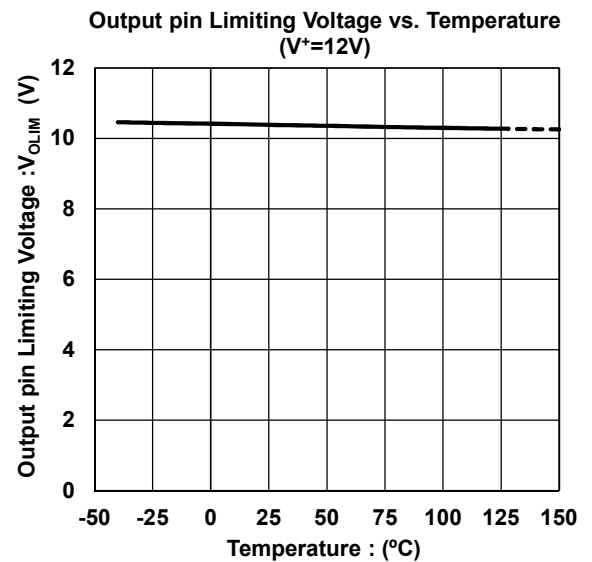
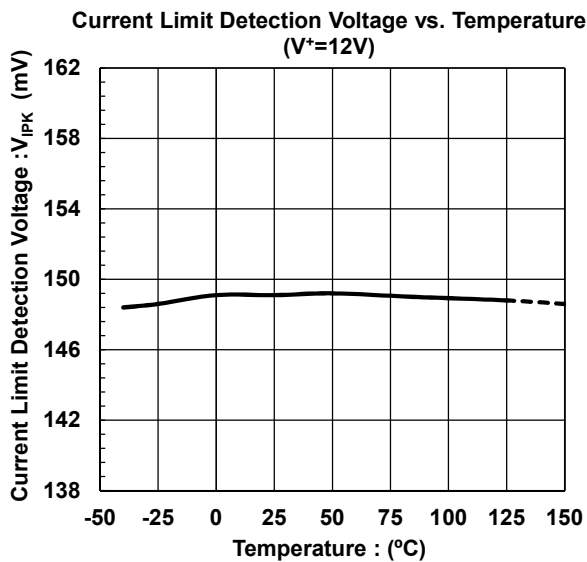
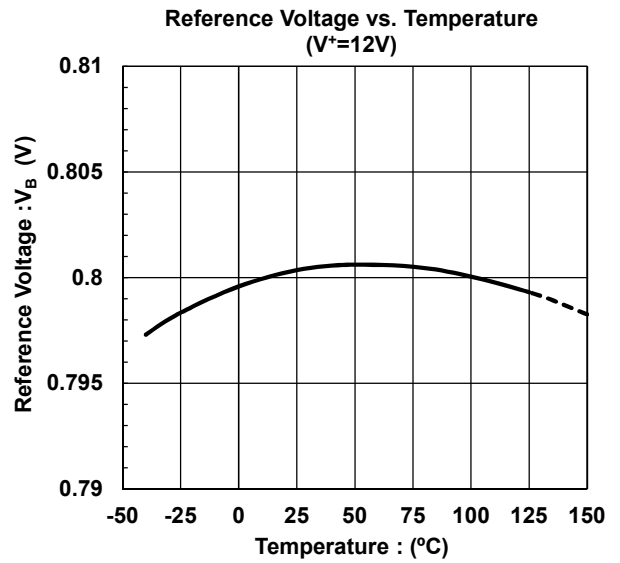
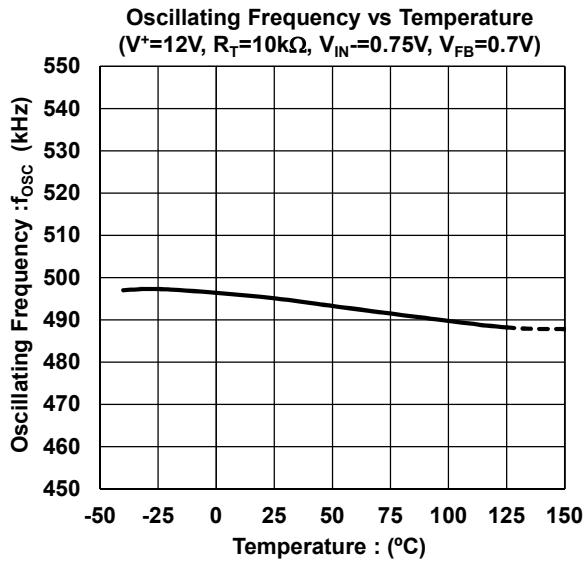




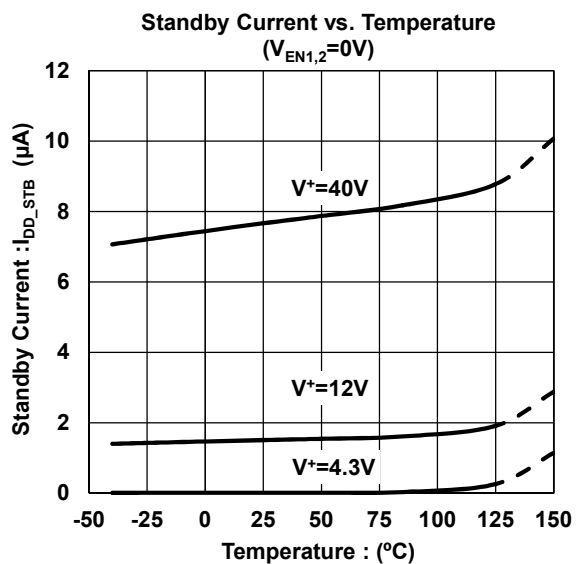
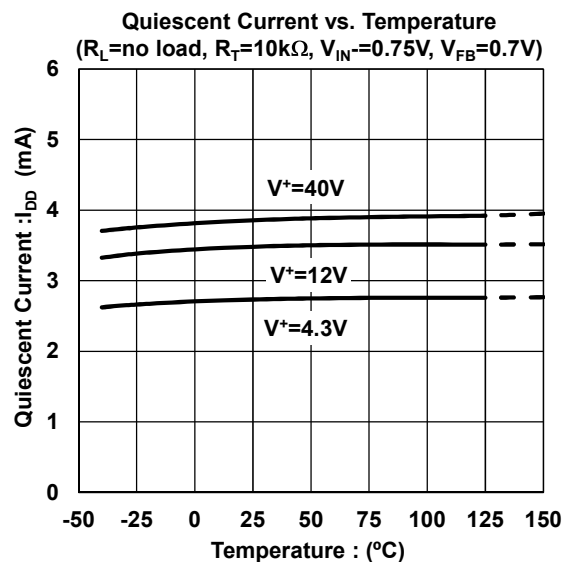
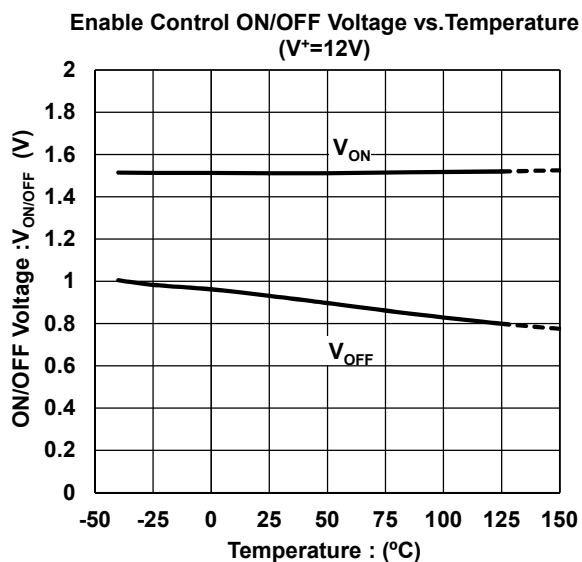
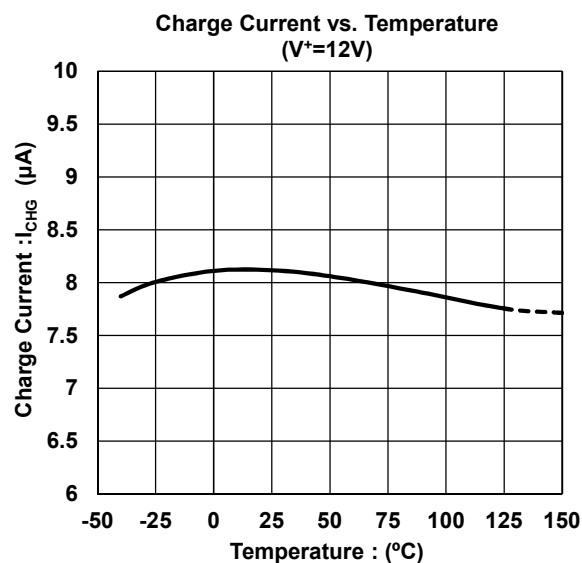
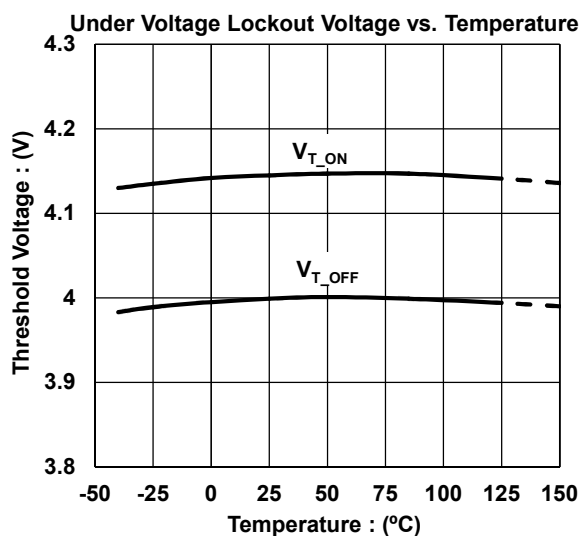
## ■ TYPICAL CHARACTERISTICS



## ■ TYPICAL CHARACTERISTICS



## ■ TYPICAL CHARACTERISTICS



## MEMO

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