

The documentation and process conversion measures necessary to comply with this document shall be completed by 7 November 2020.

INCH-POUND

MIL-PRF-19500/396M
w/AMENDMENT 1
7 August 2020
SUPERSEDING
MIL-PRF-19500/396M
29 May 2015

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, PNP, SILICON, SWITCHING, ENCAPSULATED (THROUGH HOLE AND SURFACE MOUNT) AND UNENCAPSULATED, RADIATION HARDNESS ASSURANCE, DEVICE TYPES 2N3762, 2N3763, 2N3764, AND 2N3765, QUALITY LEVELS JAN, JANTX, JANTXV, JANS, JANHC AND JANKC, JANHCA, AND JANKCA

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP silicon switching transistors. Four levels of product assurance (JAN, JANTX, JANTXV and JANS) are provided for each encapsulated device type as specified in [MIL-PRF-19500](#) and two levels of product assurance (JANHC and JANKC) are provided for each unencapsulated device type. RHA level designators "M", "D", "P", "L", "R", "F", "G", and "H" are appended to the device prefix to identify devices, which have passed RHA requirements.

1.2 Package outlines and die topography. The device packages for the encapsulated device types are as follows: (2N3762L and 2N3763L) (TO-5) in accordance with [figure 1](#), (2N3762 and 2N3763) (TO-39) in accordance with [figure 1](#), 2N3764 and 2N3765 (TO-46) in accordance with [figure 2](#), (U4) in accordance with [figure 3](#), (UA) in accordance with [figure 4](#). The dimensions and topography for JANHC and JANKC unencapsulated die is as follows: The A version die in accordance with [figure 5](#).

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Types	P_T $T_A = +25^\circ\text{C}$ (1)	P_T $T_C = +25^\circ\text{C}$ (1)	P_T $T_{SP(AM)} = +25^\circ\text{C}$ (1)	P_T $T_{SP(IS)} = +25^\circ\text{C}$ (1)	$R_{\theta JA}$ Steel (2)	$R_{\theta JA}$ Kovar (2)	$R_{\theta JC}$ Steel (2)	$R_{\theta JC}$ Kovar	$R_{\theta JSP(AM)}$ (2)	$R_{\theta JSP(IS)}$ (2)	T_J and T_{STG}
2N3762, L	<u>W</u> 1.0	<u>W</u> 2	<u>W</u>	<u>W</u>	<u>°C/W</u> 175	<u>°C/W</u> 175	<u>°C/W</u> 30	<u>°C/W</u> 50	<u>°C/W</u>	<u>°C/W</u>	<u>°C</u>
2N3762U4		10					15				
2N3762UA			5	1.94					35	90	
2N3763, L	1.0	2			175	175	30	50			
2N3763U4		10					15				
2N3763UA			5	1.94					35	90	
2N3764	0.5	2			325	350	70	60			
2N3765	0.5	2			325	350	70	60			

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* 1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$. - Continued.

Types	V_{CBO}	V_{CEO}	V_{EBO}	I_C
2N3762, L, 2N3762U4, 2N3762UA, 2N3764 2N3763, L, 2N3763U4, 2N3763UA, 2N3765	<u>V</u> dc -40 -60	<u>V</u> dc -40 -60	<u>V</u> dc -5 -5	<u>A</u> dc -1.5 -1.5

(1) For derating, see [figure 6](#), [figure 7](#), [figure 8](#), [figure 9](#), [figure 10](#), [figure 11](#), and [figure 12](#).

(2) For thermal curves, see [figure 13](#), [figure 14](#), [figure 15](#), [figure 16](#), [figure 17](#), [figure 18](#), and [figure 19](#).

* 1.4 Primary electrical characteristics. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Limits	h_{FE1} $V_{CE} = -1.0 \text{ V dc}$ $I_C = -10 \text{ mA dc}$	h_{FE3} $V_{CE} = -1.0 \text{ V dc}$ $I_C = -500 \text{ mA dc}$	$h_{FE5} (1)$ $V_{CE} = -5.0 \text{ V dc}$; $I_C = -1.5 \text{ A dc}$	
			2N3762 2N3762L 2N3764	2N3763 2N3763L 2N3765
Min Max	35	40 140	30	20

Limits	$ h_{FE} $		$V_{CE(\text{SAT})3}$ $I_C = -500 \text{ mA dc}$ $I_B = -50 \text{ mA dc}$ (1)	C_{obo} $V_{CE} = -10 \text{ V dc}$ $I_E = 0$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	Pulse response	
	See figure 20	See figure 21				
Min Max	2N3762 2N3764	2N3763 2N3765	<u>V</u> dc 0.5	<u>pF</u> 25	t_d <u>ns</u> 8	t_r <u>ns</u> 35
	1.8 6.0	1.5 6.0			t_s <u>ns</u> 80	t_f <u>ns</u> 35

(1) Pulsed (see [4.5.1](#)).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.5](#) for PIN construction example and [6.6](#) for a list of available PINs.

1.5.1 JAN certification mark and quality level.

1.5.1.1 Quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS".

1.5.1.2 Quality level designators for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANHC" and "JANKC".

1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest for JANTXV and JANS quality levels are as follows: "M", "D", "P", "L", "R", "F", "G", and "H".

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "3762", "3763", "3764", and "3765".

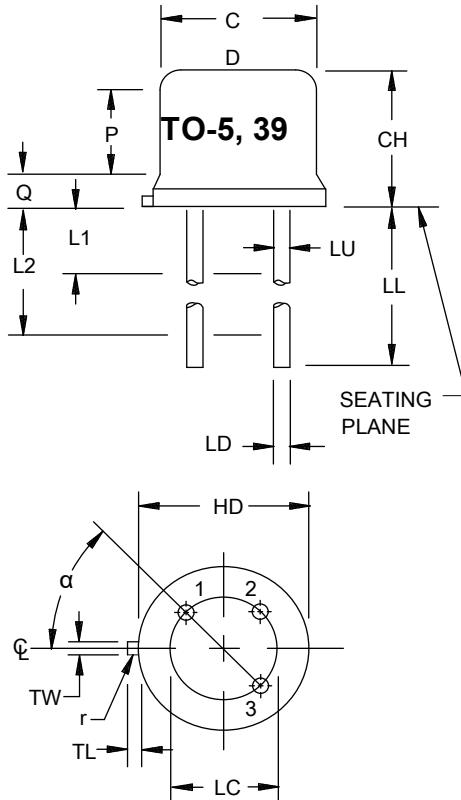
* 1.5.4 Suffix symbols. The following suffix letters are incorporated in the PIN in the order listed in the table as applicable:

	A blank suffix symbol for device types 2N3762 and 2N3763 indicates a through-hole mount package TO-39 metal can (see figure 1). A blank suffix symbol for device types 2N3764 and 2N3765 indicates a through-hole mount package TO-46 metal can (see figure 2).
L	An L suffix for device types 2N3762 and 2N3763 Indicates a through-hole mount package TO-5 metal can with longer lead lengths than blank second suffix symbol device (see figure 1).
U4	Indicates a surface mount.
UA	Indicates a surface mount.

1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on [QML-19500](#).

1.5.6 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifier that is applicable for this specification sheet is "A".

Symbol	Dimensions				Note	
	Inches		Millimeters			
	Min	Max	Min	Max		
CD	.305	.335	7.75	8.51	6	
CH	.240	.260	6.10	6.60		
HD	.335	.370	8.51	9.40		
LC	.200 TP		5.08 TP		7	
LD	.016	.019	0.41	0.48	8,9	
LL	See note 14					
LU	.016	.019	0.41	0.48	8,9	
L ₁		.050		1.27	8,9	
L ₂	.250		6.35		8,9	
P	.100		2.54		7	
Q		.030		0.76	5	
TL	.029	.045	0.74	1.14	3,4	
TW	.028	.034	0.71	0.86	3	
r		.010		0.25	10	
α	45° TP		45° TP		7	

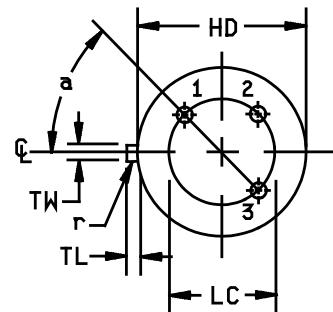
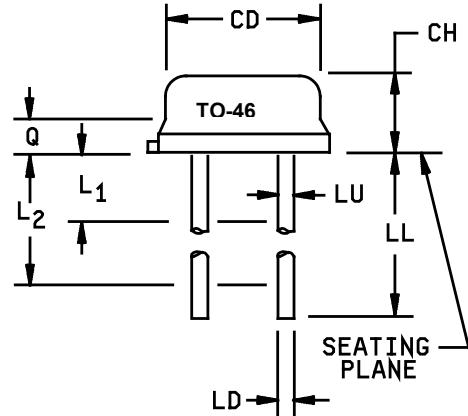


NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. CD shall not vary more than .010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
7. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by gauging procedure.
8. Dimension LU applies between L₁ and L₂. Dimension LD applies between L₂ and LL minimum. Diameter is uncontrolled in and beyond LL minimum.
9. All three leads.
10. The collector shall be internally connected to the case.
11. Dimension r (radius) applies to both inside corners of tab.
12. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.
13. Lead 1 = emitter, lead 2 = base, lead 3 = collector.
14. For L-suffix devices (TO-5), dimension LL = 1.5 inches (38.10 mm) min. and 1.75 inches (44.45 mm) max. For non L suffix devices (TO-39), dimension LL = .5 inch (12.70 mm) min. and .750 inch (19.05 mm) max.

FIGURE 1. Physical dimensions 2N3762L and 2N3763L (TO-5), 2N3762 and 2N3763 (TO-39).

Ltr.	Dimensions				Notes	
	Inches		Millimeters			
	Min	Max	Min	Max		
CD	.178	.195	4.52	4.95		
CH	.065	.085	1.65	2.16		
HD	.209	.230	5.31	5.84		
LC	.100 TP		2.54 TP		5	
LD	.016	.021	0.41	0.53		
LL	.500	.750	12.70	19.05	6	
LU	.016	.019	0.41	0.48	6	
L ₁		.050		1.27	6	
L ₂	.250		6.35		6	
Q		.040		1.02	3	
TL	.028	.048	0.71	1.22	8	
TW	.036	.046	0.91	1.17	4	
r		.010		0.25	9	
α	45° TP		45° TP		5	

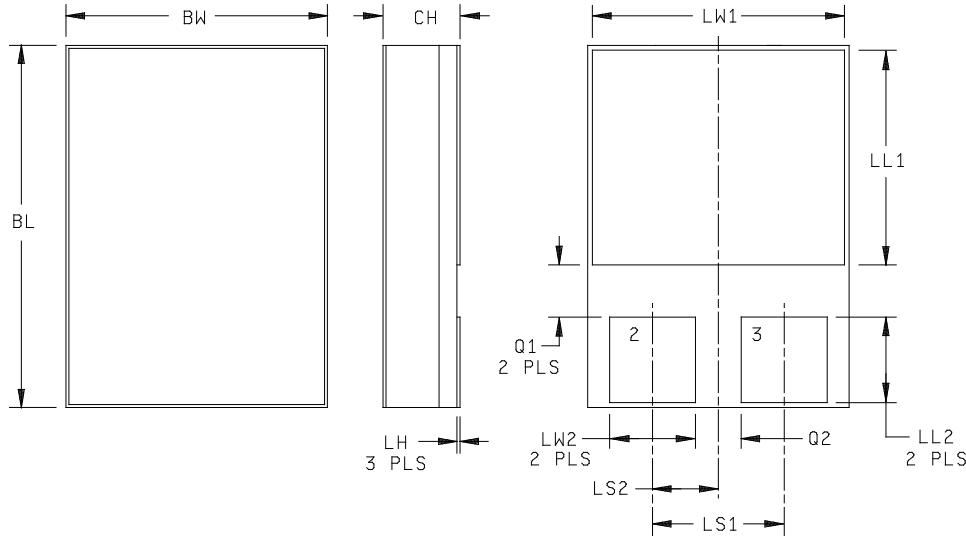


NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of TP relative to tab. Device may be measured by direct methods or by gauge.
6. Symbol LU applies between L₁ and L₂. Dimension LD applies between L₂ and LL minimum.
7. Lead number three is electrically connected to case.
8. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
9. Symbol r applied to both inside corners of tab.
10. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
11. Lead 1 is emitter, lead 2 is base, and lead 3 is collector.

FIGURE 2. Physical dimensions - 2N3764 and 2N3765 (TO-46).

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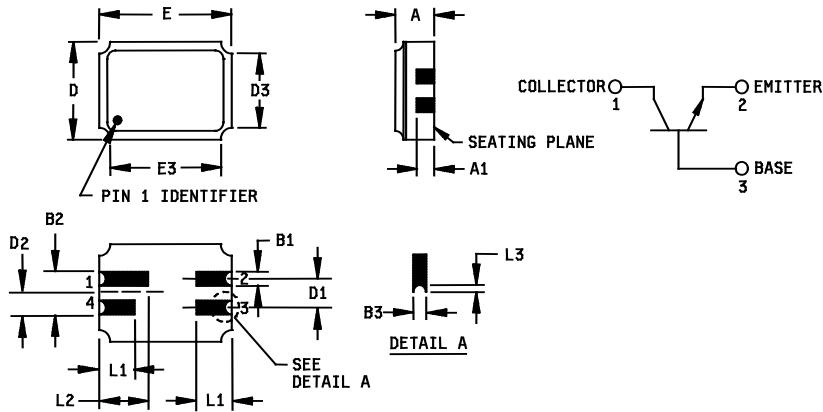


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	0.215	0.225	5.46	5.72
BW	0.145	0.155	3.68	3.94
CH	0.049	0.075	1.24	1.91
LH	-	0.020	-	0.508
LL1	0.085	0.125	2.16	3.17
LL2	0.045	0.075	1.14	1.90
LS1	0.070	0.095	1.48	2.41
LS2	0.035	0.048	0.889	1.21
LW1	0.135	0.145	3.43	3.68
LW2	0.047	0.057	1.19	1.45
Q1	0.030	0.070	0.762	1.78
Q2	0.020	0.035	0.508	0.88
Terminal	BIPOLEAR			
1	Collector			
2	Base			
3	Emitter			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 3. Physical dimensions and configuration (U4).

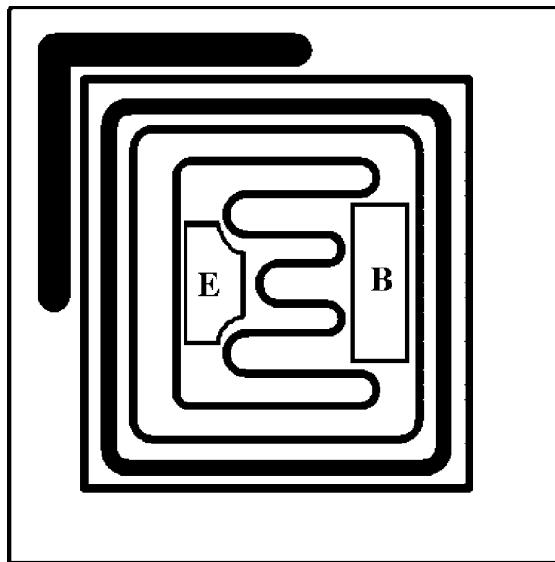


Symbol	Dimensions				Note	
	Inches		Millimeters			
	Min	Max	Min	Max		
A	.061	.075	1.55	1.90	3	
A1	.029	.041	0.74	1.04		
B1	.022	.028	0.56	0.71		
B2	.075 REF		1.91 REF			
B3	.006	.022	0.15	0.56	5	
D	.145	.155	3.68	3.93		
D1	.045	.055	1.14	1.39		
D2	.0375 BSC		.952 BSC			
D3		.155		3.93		
E	.215	.225	5.46	5.71		
E3		.225		5.71		
L1	.032	.048	0.81	1.22		
L2	.072	.088	1.83	2.23		
L3	.003		0.08		5	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension "A" controls the overall package thickness. When a window lid is used, dimension "A" must increase by a minimum of .010 inch (0.254 mm) and a maximum of .040 inch (1.020 mm).
4. The corner shape (square, notch, radius) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions "B3" minimum and "L3" minimum and the appropriately castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimension "B3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
6. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 4. Physical dimensions, surface mount (UA version).



NOTES:

1. Chip size .040 inch (1.02 mm) x .040 inch (1.02 mm) $\pm .001$ inch (0.03 mm).
2. Chip thickness .010 $\pm .0015$ inch.
3. Top metal Aluminum 15,000 \AA minimum, 18,000 \AA nominal.
4. Back metal Gold 3,500 \AA minimum, 5,000 \AA nominal.
5. Backside Collector.
6. Bonding pad B = .006 inch (0.15 mm) x .008 inch (0.2 mm),
E = .006 inch (0.15 mm) x .004 inch (0.1 mm).

FIGURE 5. JANHCA and JANKCA die dimensions.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) – Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and on [figure 1](#), [figure 2](#), [figure 3](#), [figure 4](#), and [figure 5](#) herein.

3.4.1 Lead finish. Lead finish shall be solderable as defined in [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.5 Radiation hardness assurance (RHA). Radiation hardness assurance requirements, PIN designators, and test levels shall be as defined in [MIL-PRF-19500](#).

3.6 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#) herein.

3.7 Electrical test requirements. The electrical test requirements shall be the subgroups specified in [table I](#).

3.8 Marking. Devices shall be marked in accordance with [MIL-PRF-19500](#). The radiation hardened designator M, D, P, L, R, F, G, or H shall immediately precede (or replace) the device "2N" identifier (depending upon degree of abbreviation required).

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [table I](#) and [table II](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and [6.3](#) herein.

4.2.1 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with [MIL-PRF-19500](#).

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANTX, JANTXV and JANS only). Screening shall be in accordance with table E-IV of [MIL-PRF-19500](#), and as specified herein. The following measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screen	Measurement	
	JANS level	JANTX and JANTXV level
3a 3b (1) 3c	Required Not applicable Required method 3131 of MIL-STD-750 . See 4.3.3 .	Required Not applicable Required method 3131 of MIL-STD-750 . See 4.3.3 .
9	I_{CBO2} , h_{FE3} read and record	Not applicable
10	24 hours minimum	24 hours minimum
11	I_{CBO2} ; h_{FE3} ; $\Delta I_{CBO2} = 100$ percent of initial value or -10 nA dc, whichever is greater. $\Delta h_{FE3} = \pm 15$ percent	I_{CBO2} ; h_{FE3}
12	See 4.3.1 240 hours minimum	See 4.3.1
13	Subgroups 2 and 3 of table I herein; $\Delta I_{CBO2} = 100$ percent of initial value or -10 nA dc, whichever is greater; $\Delta h_{FE3} = \pm 15$ percent (2)	Subgroup 2 of table I herein; $\Delta I_{CBO2} = 100$ percent of initial value or -10 nA dc, whichever is greater; $\Delta h_{FE3} = \pm 15$ percent

- (1) Shall be performed any time after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.
- (2) PDA = 5 percent for screen 13, applies to ΔI_{CBO2} , Δh_{FE3} , I_{CBO2} , h_{FE3} . Thermal impedance (Z_{0JX}) is not required in screen 13.

* 4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: $V_{CB} = -10$ - -30 V dc; power shall be applied to achieve the required junction temperature, $T_J = +135^\circ\text{C}$ minimum using a minimum power dissipation = 75 percent of maximum rated P_T (see [1.3](#)). NOTE: No heat sink or forced air cooling on the devices shall be permitted. Power burn-in conditions for "L", "U4", and "UA" suffix devices are identical to their corresponding non-suffix devices.

4.3.2 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with [MIL-PRF-19500](#), "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.3.3 Thermal impedance (Z_{0JX} measurements). The Z_{0JX} measurements shall be performed in accordance with method 3131 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{MD} (and V_C where appropriate). The Z_{0JX} limit used in screen 3c of [4.3](#) shall comply with the thermal impedance graph on figures 13 through 19 (less than or equal to the curve value at the same t_H time) or shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein. If alternate screening is being performed in accordance with [MIL-PRF-19500](#), a sample of screened devices shall be submitted to and pass the requirements of [table I](#), subgroups 1 and A2, inspection only (table E-VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with [4.4.2](#) herein).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of [MIL-PRF-19500](#) and [table I](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) of [MIL-PRF-19500](#) and [4.4.2.1](#) herein. Delta requirements shall be in accordance with [table I](#), subgroup 2 and [4.5.2](#) herein except for thermal impedance. See [4.4.2.2](#) for JAN, JANTX, and JANTXV group B testing. Delta requirements for JAN, JANTX, and JANTXV shall be after each step in [4.4.2.2](#) and shall be in accordance with [table I](#), subgroup 2 and [4.5.2](#) herein.

* 4.4.2.1 Group B inspection, table E-VIA (JANS) of [MIL-PRF-19500](#)

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B4	1037	$V_{CB} = -10 \text{ - } -30 \text{ V dc.}$
*	B5	(NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.) $V_{CB} = -10 \text{ V dc, } P_D \geq 100 \text{ percent of maximum rated } P_T$ (see 1.3).
		Option 1: 96 hours minimum, sample size in accordance with table E-VIa of MIL-PRF-19500 adjust T_A or P_D to achieve $T_J = +275^\circ\text{C}$ minimum.
		Option 2: 216 hrs minimum, sample size = 45, $c = 0$; adjust T_A or P_D to achieve $T_J = +225^\circ\text{C}$ minimum.
B6	3131	$R_{\theta JA}$ for TO-5, UA, $R_{\theta JC}$ for U4.

* 4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of [MIL-PRF-19500](#) shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
*	1	Steady-state life: Test condition B, 1,000 hours minimum, $V_{CB} = -10 \text{ V dc}$, power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 75 \text{ percent of maximum rated } P_T$ as defined in 1.3 . $n = 45$ devices, $c = 0$.
2	1039	HTRB: Test condition A, 48 hours minimum. $n = 45$ devices, $c = 0$.
3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$. $n = 22$, $c = 0$.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See [MIL-PRF-19500](#).
- Must be chosen from an inspection lot that has been submitted to and passed [table I](#), subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#), and in [4.4.3.1](#) (JANS) and [4.4.3.2](#) (JAN, JANTX, and JANTXV) herein for group C testing. Delta requirements shall be in accordance with [table I](#), subgroup 2 and [4.5.2](#) herein.

* [4.4.3.1 Group C inspection, table E-VII \(JANS\) of MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E. (Does not apply to U4 and UA)
* C6	1027	1,000 hours at $V_{CB} = -10$ V dc; $T_J = +150^\circ\text{C}$ min. External heating of the device under test to achieve $T_J = +150^\circ\text{C}$ minimum is allowed provided that a minimum of 75 percent of rated power is dissipated. No heat sink or forced-air cooling on device shall be permitted.

[4.4.3.2 Group C inspection, table E-VII \(JAN, JANTX, and JANTXV\) of MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E. (Does not apply to U4 and UA)
C5	3131	Thermal resistance see figures 13 through 19 (only applies to $R_{\theta JA}$ for TO-39, TO-5, TO-46, and $R_{\theta JC}$ for U4). See 4.3.3 .
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes [table I](#) tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group D inspection. Conformance inspection for hardness assured JANS and JANTXV types shall include the group D tests specified in [table II](#) herein. These tests shall be performed as required in accordance with [MIL-PRF-19500](#) and method 1019 of [MIL-STD-750](#), for total ionizing dose or method 1017 of [MIL-STD-750](#) for neutron fluence as applicable (see [6.2](#) herein), except group D, subgroup 2 may be performed separate from other subgroups. Group D inspection may also be performed ahead of the screening lot using die selected in accordance with [MIL-PRF-19500](#) and related documents. Alternate package options may also be substituted for the testing provided there is no adverse effect to the fluence profile.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#), [table III](#) herein. Delta requirements shall be in accordance with [table I](#), subgroup 2 and [4.5.2](#) herein.

[4.5 Method of inspection](#). Methods of inspection shall be as specified in the appropriate tables and as follows.

[4.5.1 Pulse measurements](#). Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

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* 4.5.2 Delta requirements. Delta requirements shall be as specified below:

Step	Inspection	MIL-STD-750		Symbol	Limit
		Method	Conditions		
1	Collector-base cutoff current 2N3762, L, U4, UA; 2N3764 2N3763, L, U4, UA; 2N3765	3036	Bias condition D $V_{CB} = -20$ V dc $V_{CB} = -30$ V dc	ΔI_{CB02} (1)	100 percent of initial value or ± 10 nA dc, whichever is greater.
2	Forward current transfer ratio	3076	$V_{CE} = -1.0$ V dc; $I_c = -150$ mA dc; pulsed see 4.5.1	Δh_{FE2} (1)	± 25 percent change from initial reading.
3	Collector to emitter voltage (saturated)	3071	$I_c = -500$ mA dc; $I_b = -50$ mA dc; pulsed (see 4.5.1)	$\Delta V_{CE(SAT)3}$ (2)	± 50 mV dc change from previous measured value

(1) Devices which exceed the [table I](#) limits for this test shall not be accepted.

(2) Applies to JANS only.

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* TABLE I. Group A inspection

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 2/</u>						
Visual and mechanical inspection 3/	2071					
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0 (not required for laser marked devices)				
Salt atmosphere 4/	1041	Sample size = 6 devices, c = 0, (laser marked devices only).				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal 4/ Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements 4/		Table I , subgroup 2				
Bond strength 3/ 4/	2037	Precondition $T_A = + 250^\circ\text{C}$ at $t = 24$ hours or $T_A = + 300^\circ\text{C}$ at $t = 2$ hours n = 11 wires, c = 0				
Decap internal visual (design verification)	2075	n = 1 device, c = 0				
<u>Subgroup 2</u>						
Thermal Impedance 6/	3131	See 4.3.3	Z_{0JX}			°C/W
Collector to base, cutoff current.	3036	Bias condition D	I_{CBO1}	-10		μA dc
2N3762, 2N3764 2N3763, 2N3765		$V_{CB} = -40$ V dc $V_{CB} = -60$ V dc				
Emitter to base, cutoff current. 2N3762, 2N3764 2N3763, 2N3765	3061	Bias condition D. $V_{EB} = -5$ V dc	I_{EBO1}	10		μA dc
Breakdown voltage collector to emitter. 2N3762, 2N3764 2N3763, 2N3765	3011	Bias condition D; $I_C = -10$ mA dc Pulsed (see 4.5.1)	$V_{(BR)CEO}$	-40		V dc
				-60		

See footnotes at end of table.

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* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> Continued						
Collector to base cutoff current. 2N3762, 2N3764 2N3763, 2N3765	3036	Bias condition D $V_{CB} = -20$ V dc $V_{CB} = -30$ V dc	I_{CBO2}		-100	nA dc
Collector to emitter cutoff current. 2N3762, 2N3764 2N3763, 2N3765	3041	Bias condition A; $V_{EB} = 2.0$ V dc $V_{CE} = 20$ V dc $V_{CE} = 30$ V dc	I_{CEX1}		100	nA dc
Emitter to base cutoff current	3061	Bias condition D; $V_{EB} = -2.0$ V dc	I_{EBO2}		-200	nA dc
Forward - current transfer ratio	3076	$V_{CE} = -1.0$ V dc; $I_C = -10$ mA dc	h_{FE1}	35		
Forward - current transfer ratio	3076	$V_{CE} = -1.0$ V dc; $I_C = -150$ mA dc; pulsed (see 4.5.1)	h_{FE2}	40		
Forward - current transfer ratio	3076	$V_{CE} = -1.0$ V dc; $I_C = -500$ mA dc; pulsed (see 4.5.1)	h_{FE3}	40	140	
Forward - current transfer ratio. 2N3762, 2N3764 2N3763, 2N3765	3076	$V_{CE} = -1.5$ V dc; $I_C = -1.0$ A dc; pulsed (see 4.5.1)	h_{FE4}	30 20	120 80	
Forward - current transfer ratio. 2N3762, 2N3764 2N3763, 2N3765	3076	$V_{CE} = -5.0$ V dc; $I_C = -1.5$ A dc; pulsed (see 4.5.1)	h_{FE5}	30 20		
Collector to emitter voltage (saturated)	3071	$I_C = -10$ mA dc; $I_B = -1$ mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)1}$		-0.10	V dc
Collector to emitter voltage (saturated)	3071	$I_C = -150$ mA dc; $I_B = -15$ mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)2}$		-0.22	V dc
Collector to emitter voltage (saturated)	3071	$I_C = -500$ mA dc; $I_B = -50$ mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)3}$		-0.50	V dc
Collector to emitter voltage (saturated)	3071	$I_C = -1.0$ A dc; $I_B = -100$ mA dc; pulsed (see 4.5.1)	$V_{CE(SAT)4}$		-0.90	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = -10$ mA dc; $I_B = 1$ mA dc	$V_{BE(SAT)1}$		-0.80	V dc

See footnotes at end of table.

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* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> Continued						
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = -150$ mA dc; $I_B = -15$ mA dc; pulsed (see 4.5.1)	V _{BE(SAT)2}		-1.0	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = -500$ mA dc; $I_B = -50$ mA dc, pulsed (see 4.5.1)	V _{BE(SAT)3}		-1.2	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = -1.0$ A dc; $I_B = -100$ mA dc, pulsed (see 4.5.1)	V _{BE(SAT)4}	-.90	-1.40	V dc
<u>Subgroup 3</u>						
High-temperature operation		$T_A = +150^\circ\text{C}$				
Collector to emitter cutoff current.	3041	Bias condition A; $V_{EB} = 2$ V dc;	I _{CEX2}		150	μA dc
2N3762, 2N3764 2N3763, 2N3765		$V_{CE} = 20$ V dc; $V_{CE} = 30$ V dc				
Low-temperature operation		$T_A = -55^\circ\text{C}$				
Forward-current transfer ratio	3076	$V_{CE} = -1.0$ V dc; $I_C = -500$ mA dc; pulsed (see 4.5.1)	h _{FE6}	20		
<u>Subgroup 4</u>						
Magnitude of common emitter, small - signal short - circuit forward - current transfer ratio.	3306	$V_{CE} = -10$ V dc; $I_C = -50$ mA dc; $f = 100$ MHz	h _{fe}			
2N3762, 2N3764 2N3763, 2N3765				1.8 1.5	6.0 6.0	
Open circuit output capacitance	3236	$V_{CB} = -10$ V dc; $I_E = 0$; 100 kHz $\leq f \leq 1$ MHz	C _{obo}		25	pF
Input capacitance (output open - circuited)	3240	$V_{EB} = -.5$ V dc; $I_C = 0$; 100 kHz $\leq f \leq 1$ MHz	C _{ibo}		80	pF

See footnotes at end of table.

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* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4 Continued</u>						
Pulse response						
Pulse delay time	3251	See figure 20	t_d		8	ns
Pulse rise time	3251	See figure 20	t_r		35	ns
Pulse storage time	3251	See figure 21	t_s		80	ns
Pulse fall time	3251	See figure 21	t_f		35	ns
<u>Subgroups 5 and 6</u>						
Not applicable						

- 1/ For sampling plan, see [MIL-PRF-19500](#). Electrical characteristics for "L", "U4", "and "UA" suffix devices are identical to their corresponding non-suffix devices.
- 2/ For resubmission of failed [table I](#) subgroup 1, double the sample size of the failed test or sequence of tests. A failure in [table I](#), subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.
- 3/ Separate samples may be used.
- 4/ Not required for JANS devices.
- 5/ Not required for laser marked devices.
- * 6/ For end-point measurements, this test is required for the following subgroups:
 - Group B, subgroups 3, 4 and 5 (JANS).
 - Group B, step 1(JAN, JANTX, JANTXV).
 - Group C, subgroups 2 and 6.
 - Group E, subgroup 1.

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* TABLE II. Group D inspection.

Inspection <u>1/ 2/ 3/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 4/</u>						
Neutron irradiation	1017	Neutron exposure $V_{CES} = 0$ V				
Collector to base, cutoff current. 2N3762, 2N3764 2N3763, 2N3765	3036	Bias condition D $V_{CB} = -40$ V dc $V_{CB} = -60$ V dc	I_{CBO1}		-20	μ A dc
Emitter to base, cutoff current. 2N3762, 2N3764 2N3763, 2N3765	3061	Bias condition D. $V_{EB} = -5$ V dc	I_{EBO1}		-20	μ A dc
Breakdown voltage collector to emitter. 2N3762, 2N3764 2N3763, 2N3765	3011	Bias condition D; $I_C = -10$ mA dc	$V_{(BR)CEO}$			V dc
Collector to base cutoff current 2N3762, 2N3764 2N3763, 2N3765	3036	Bias condition D; $V_{CB} = -20$ V dc $V_{CB} = -30$ V dc	I_{CBO2}		-40 -60	nA dc nA dc
Collector to emitter cutoff current. 2N3762, 2N3764 2N3763, 2N3765	3041	Bias condition A; $V_{EB} = 2.0$ V dc $V_{CE} = 20$ V dc $V_{CE} = 30$ V dc	I_{CEX1}		200	nA dc
Emitter to base cutoff current	3061	Bias condition D; $V_{EB} = -2.0$ V dc	I_{EBO2}		-400	nA dc
Forward-current transfer ratio 2N3762, 2N3764 2N3763, 2N3765	3076	$V_{CE} = -1.0$ V dc; $I_C = -10$ mA dc	$[h_{FE1}]$ 5/		[17.5] [17.5]	
Forward-current transfer ratio 2N3762, 2N3764 2N3763, 2N3765	3076	$V_{CE} = -1.0$ V dc; $I_C = -150$ mA dc	$[h_{FE2}]$ 5/		[20] [20]	
Forward-current transfer ratio 2N3762, 2N3764 2N3763, 2N3765	3076	$V_{CE} = -1.0$ V dc; $I_C = -500$ mA dc	$[h_{FE3}]$ 5/		[20] [20]	
Forward-current transfer ratio 2N3762, 2N3764 2N3763, 2N3765	3076	$V_{CE} = -1.5$ V dc; $I_C = -1.0$ A dc	$[h_{FE4}]$ 5/		[15] [10]	
Forward-current transfer ratio 2N3762, 2N3764 2N3763, 2N3765	3076	$V_{CE} = -5$ V dc; $I_C = -1.5$ A dc	$[h_{FE5}]$ 5/		[15] [10]	

See footnotes at end of table.

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* TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 - Continued.</u>						
Collector-emitter saturation voltage	3071	$I_C = -10 \text{ mA dc}$; $I_B = -1 \text{ mA dc}$	$V_{CE(sat)1}$		-.12	V dc
Collector-emitter saturation voltage	3071	$I_C = -150 \text{ mA dc}$; $I_B = -15 \text{ mA dc}$	$V_{CE(sat)2}$		-.25	V dc
Collector-emitter saturation voltage	3071	$I_C = -500 \text{ mA dc}$; $I_B = -50 \text{ mA dc}$	$V_{CE(sat)3}$		-.58	V dc
Collector-emitter saturation voltage	3071	$I_C = -1.0 \text{ mA dc}$; $I_B = -100 \text{ mA dc}$	$V_{CE(sat)4}$		-1.1	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = 10 \text{ mA dc}$; $I_B = 1 \text{ mA dc}$	$V_{BE(SAT)1}$		0.92	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = 150 \text{ mA dc}$; $I_B = 15 \text{ mA dc}$; pulsed (see 4.5.1)	$V_{BE(SAT)2}$		1.15	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = 500 \text{ mA dc}$; $I_B = 50 \text{ mA dc}$, pulsed (see 4.5.1)	$V_{BE(SAT)3}$		1.38	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = 1.0 \text{ A dc}$; $I_B = 100 \text{ mA dc}$, pulsed (see 4.5.1)	$V_{BE(SAT)4}$.90	1.61	V dc
<u>Subgroup 2</u>						
Total dose irradiation 2N3762, 2N3764 2N3763, 2N3765	1019	Gamma exposure $V_{CES} = 32 \text{ V}$ $V_{CES} = 48 \text{ V}$				
Collector to base, cutoff current. 2N3762, 2N3764 2N3763, 2N3765	3036	Bias condition D $V_{CB} = -40 \text{ V dc}$ $V_{CB} = -60 \text{ V dc}$	I_{CBO1}		-20	$\mu\text{A dc}$
Emitter to base, cutoff current. 2N3762, 2N3764 2N3763, 2N3765	3061	Bias condition D. $V_{EB} = -5 \text{ V dc}$	I_{EBO1}		-20	$\mu\text{A dc}$
Breakdown voltage collector to emitter. 2N3762, 2N3764 2N3763, 2N3765	3011	Bias condition D; $I_C = -10 \text{ mA dc}$	$V_{(BR)CEO}$			V dc
Collector to base cutoff current 2N3762, 2N3764 2N3763, 2N3765	3036	Bias condition D; $V_{CB} = -20 \text{ V dc}$ $V_{CB} = -30 \text{ V dc}$	I_{CBO2}	-40 -60	-200 -200	nA dc nA dc
Collector to emitter cutoff current. 2N3762, 2N3764 2N3763, 2N3765	3041	Bias condition A; $V_{EB} = -2.0 \text{ V dc}$ $V_{CE} = 20 \text{ V dc}$ $V_{CE} = 30 \text{ V dc}$	I_{CEX1}		-200	nA dc

See footnotes at end of table.

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* TABLE II. Group D inspection - Continued.

Inspection <u>1/ 2/ 3/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2 - Continued.</u>						
Emitter to base cutoff current	3061	Bias condition D; $V_{EB} = -2.0$ V dc	I_{EBO2}		-400	nA dc
Forward-current transfer ratio 2N3762, 2N3764 2N3763, 2N3765	3076	$V_{CE} = -1.0$ V dc; $I_C = -10$ mA dc	$[h_{FE1}] \underline{5/}$	[17.5] [17.5]		
Forward-current transfer ratio 2N3762, 2N3764 2N3763, 2N3765	3076	$V_{CE} = -1.0$ V dc; $I_C = -150$ mA dc	$[h_{FE2}] \underline{5/}$	[20] [20]		
Forward-current transfer ratio 2N3762, 2N3764 2N3763, 2N3765	3076	$V_{CE} = -1.0$ V dc; $I_C = -500$ mA dc	$[h_{FE3}] \underline{5/}$	[20] [20]		
Forward-current transfer ratio 2N3762, 2N3764 2N3763, 2N3765	3076	$V_{CE} = -1.5$ V dc; $I_C = -1.0$ A dc	$[h_{FE4}] \underline{5/}$	[15] [10]		
Forward-current transfer ratio 2N3762, 2N3764 2N3763, 2N3765	3076	$V_{CE} = -5.0$ V dc; $I_C = -1.5$ A dc	$[h_{FE5}] \underline{5/}$	[15] [10]		
Collector-emitter saturation voltage	3071	$I_C = -10$ mA dc; $I_B = -1$ mA dc;	$V_{CE(sat)1}$		-0.12	V dc
Collector-emitter saturation voltage	3071	$I_C = -150$ mA dc; $I_B = -15$ mA dc;	$V_{CE(sat)2}$		-0.25	V dc
Collector-emitter saturation voltage	3071	$I_C = -500$ mA dc; $I_B = -50$ mA dc;	$V_{CE(sat)3}$		-0.58	V dc
Collector-emitter saturation voltage	3071	$I_C = -1.0$ A dc; $I_B = -100$ mA dc;	$V_{CE(sat)4}$		-1.1	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = -10$ mA dc; $I_B = -1$ mA dc	$V_{BE(SAT)1}$		-0.92	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = -150$ mA dc; $I_B = -15$ mA dc; pulsed (see 4.5.1)	$V_{BE(SAT)2}$		-1.15	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $-I_C = 500$ mA dc; $I_B = -50$ mA dc, pulsed (see 4.5.1)	$V_{BE(SAT)3}$		-1.38	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = -1.0$ A dc; $I_B = -100$ mA dc, pulsed (see 4.5.1)	$V_{BE(SAT)4}$	-.90	-1.61	V dc

See footnotes at end of table.

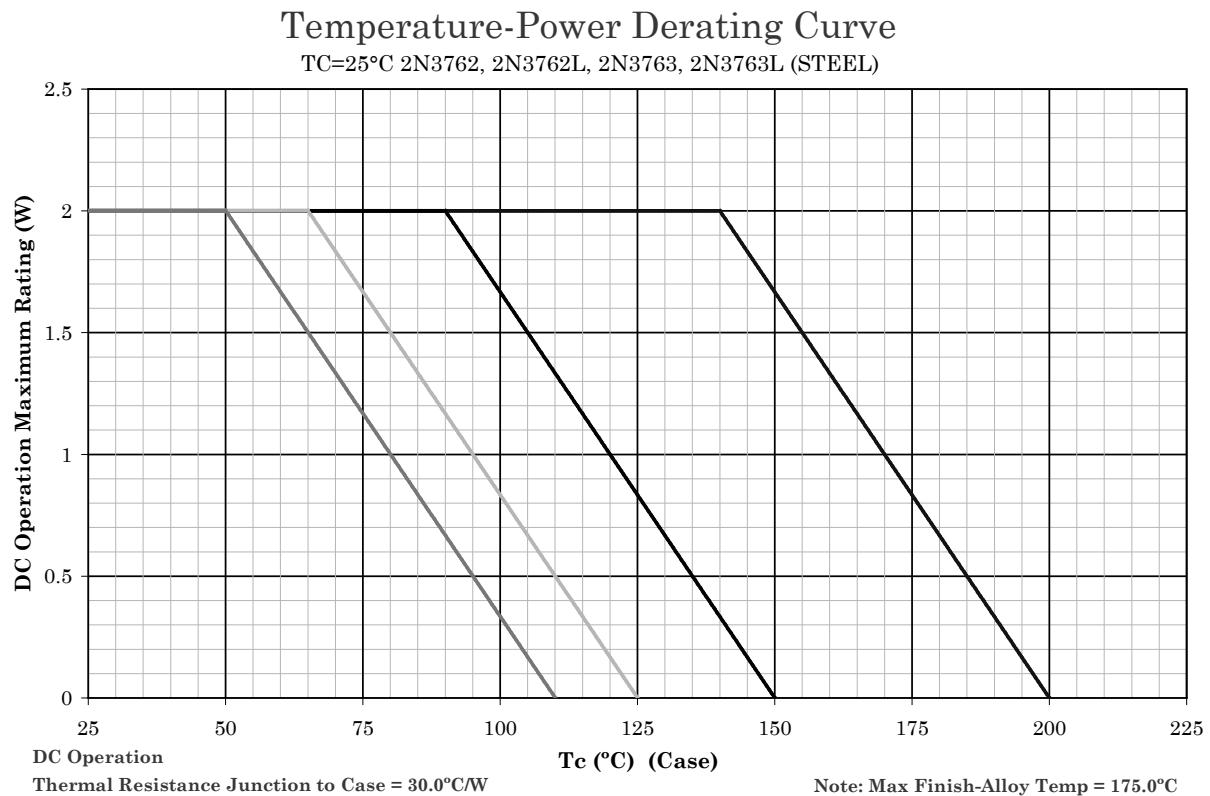
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* TABLE II. Group D inspection - Continued.

- 1/ Tests to be performed on all devices receiving radiation exposure.
- 2/ For sampling plan, see [MIL-PRF-19500](#).
- 3/ Electrical characteristics apply to the corresponding AL, UA, UB, and UBC suffix versions unless otherwise noted.
- 4/ See [6.2.g](#) herein.
- 5/ See method 1019 of [MIL-STD-750](#) for how to determine $[h_{FE}]$ by first calculating the delta ($1/h_{FE}$) from the pre- and post-radiation h_{FE} . Notice the $[h_{FE}]$ is not the same as h_{FE} and cannot be measured directly. The $[h_{FE}]$ value can never exceed the pre-radiation minimum h_{FE} that it is based upon.

* TABLE III. Group E inspection (all quality levels) - for qualification only.

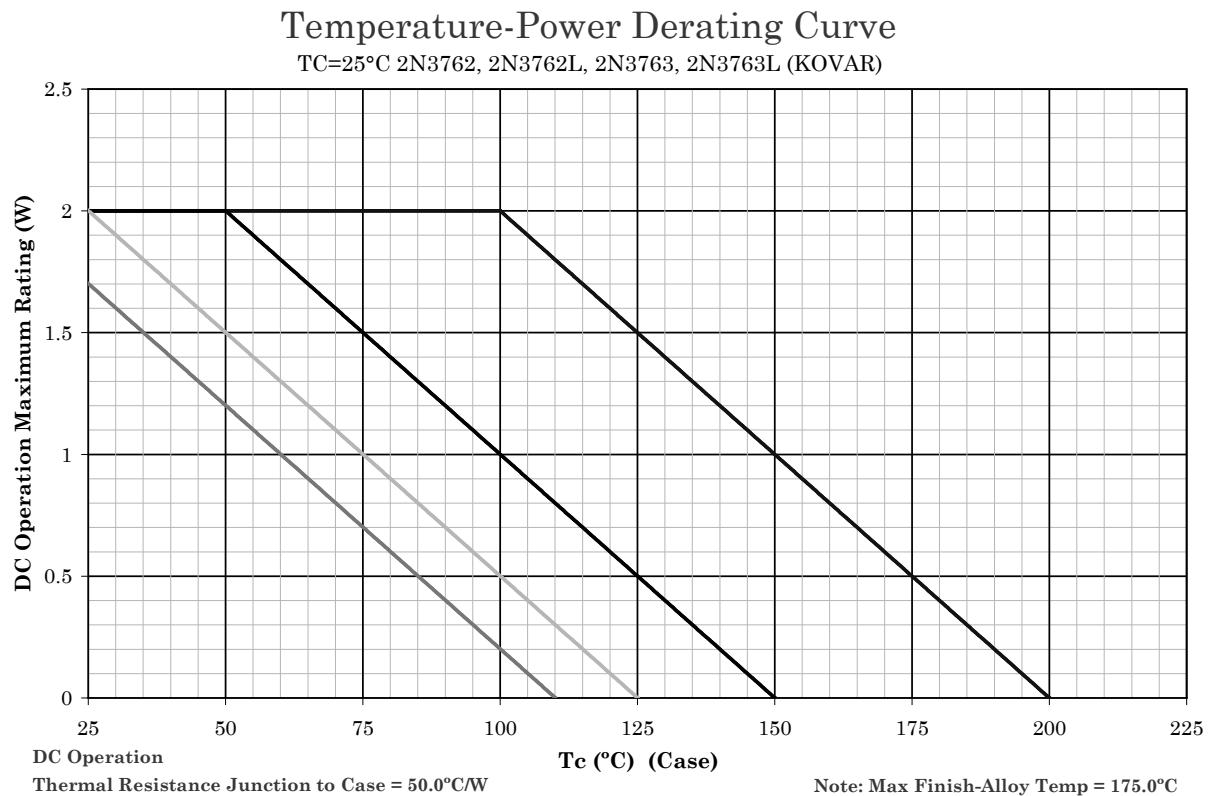
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			
Temperature cycling	1051	Test condition C, 500 cycles, sampling plan	45 devices, c = 0
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I , subgroup 2 and 4.5.2 herein.	
<u>Subgroup 2</u>			
* Intermittent operating life	1037	Intermittent operation life: $V_{CB} = -10$ V dc, 6,000 cycles. Adjust device current, or power, to achieve a minimum ΔT_J of +100°C.	45 devices, c = 0
Electrical measurements		See table I , subgroup 2 and 4.5.2 herein.	
<u>Subgroup 3</u>			
Destructive physical analysis Decap analysis only	2102		3 devices, c = 0
<u>Subgroup 4</u>			
Thermal resistance	3131	$R_{\theta JSP(IS)}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (can apply to multiple slash sheets). $R_{\theta JSP(AM)}$ need be calculated only. See MIL-PRF-19500 .	15 devices, c = 0
Thermal impedance curves			
<u>Subgroup 5</u>			
Not applicable.			
<u>Subgroup 6</u>			
ESD	1020		11 devices
<u>Subgroup 8</u>			
Reverse stability	1033	Condition B.	45 devices, c = 0



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

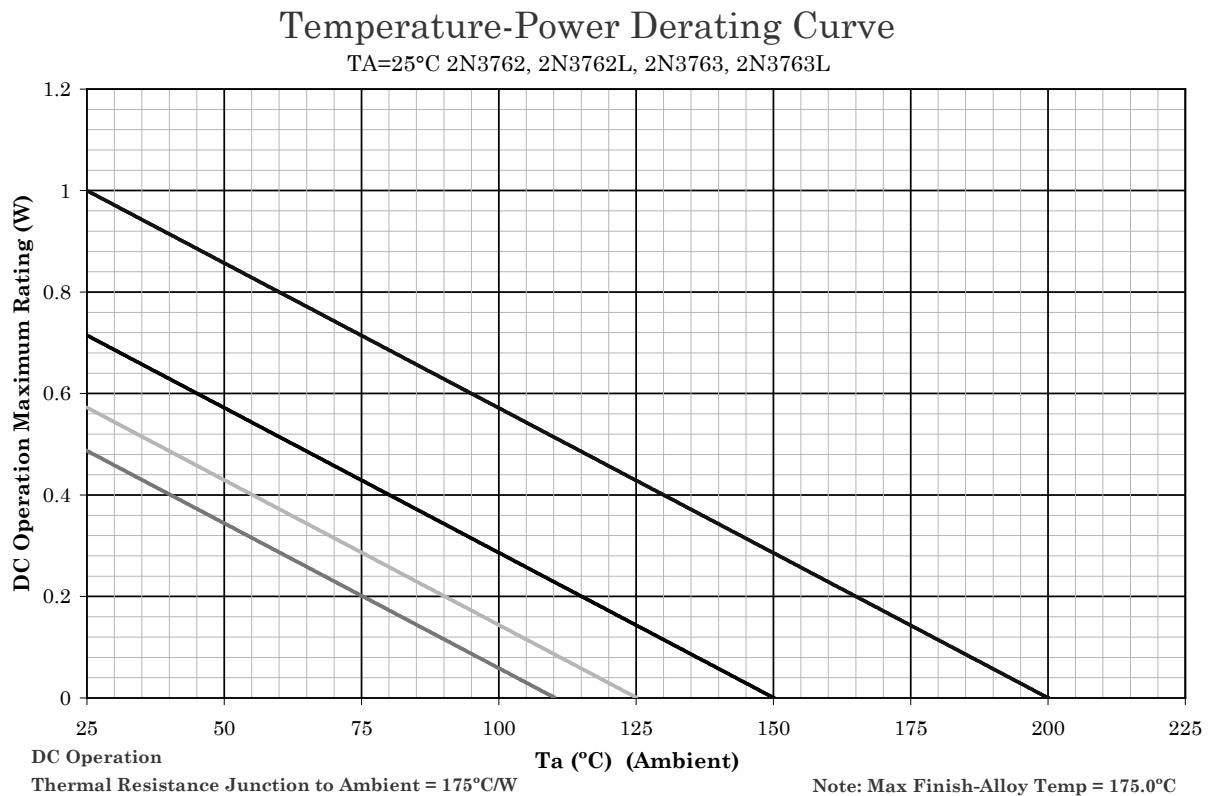
FIGURE 6A. Derating for Steel 2N3762L, 2N3763L(TO-5), and 2N3762, 2N3763(TO-39).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

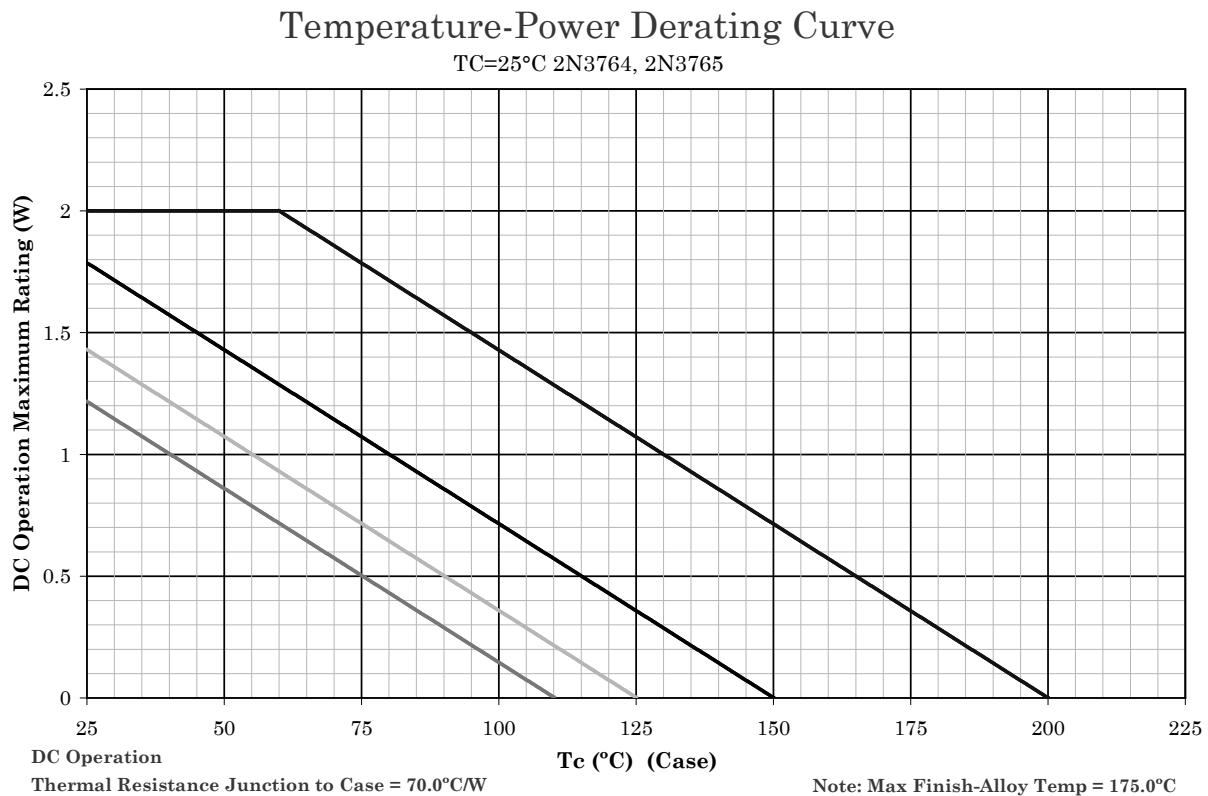
FIGURE 6B. Derating for Kovar 2N3762L, 2N3763L(TO-5), and 2N3762, 2N3763(TO-39).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

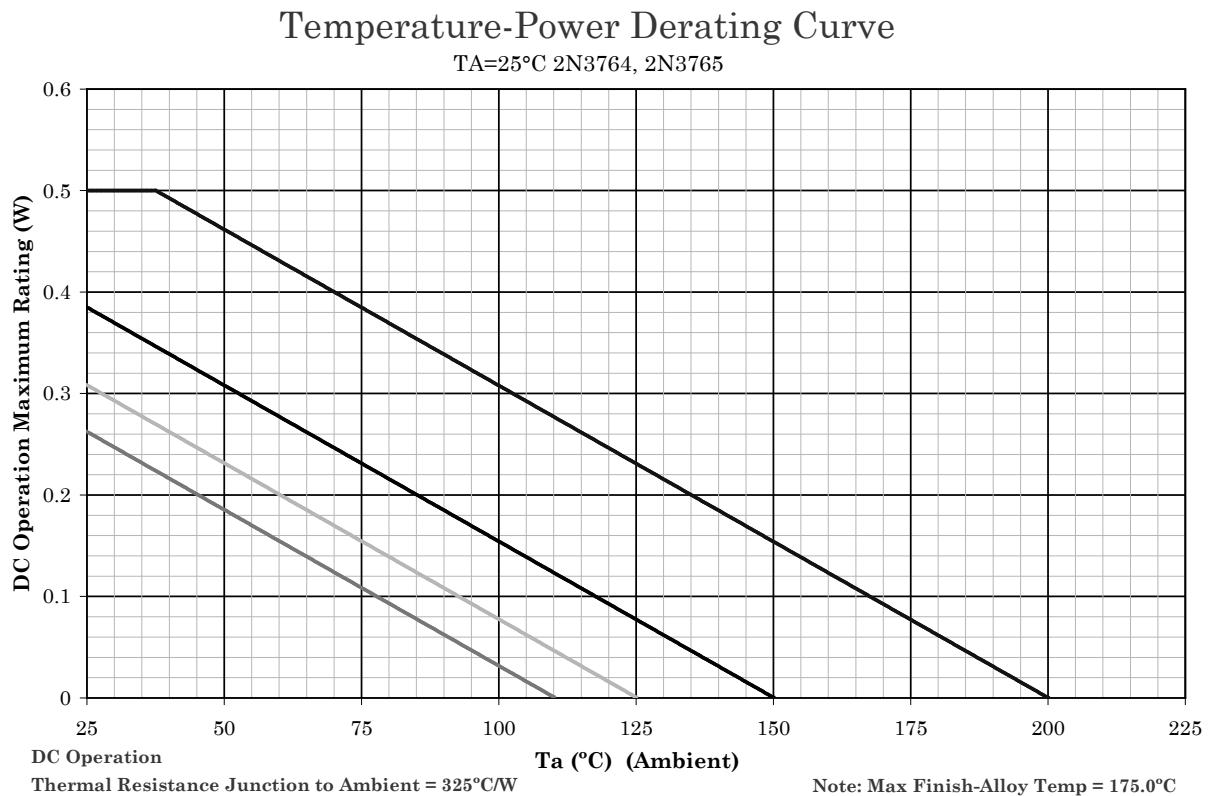
FIGURE 7. Derating for 2N3762L, 2N3763L(TO-5), and 2N3762, 2N3763(TO-39).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

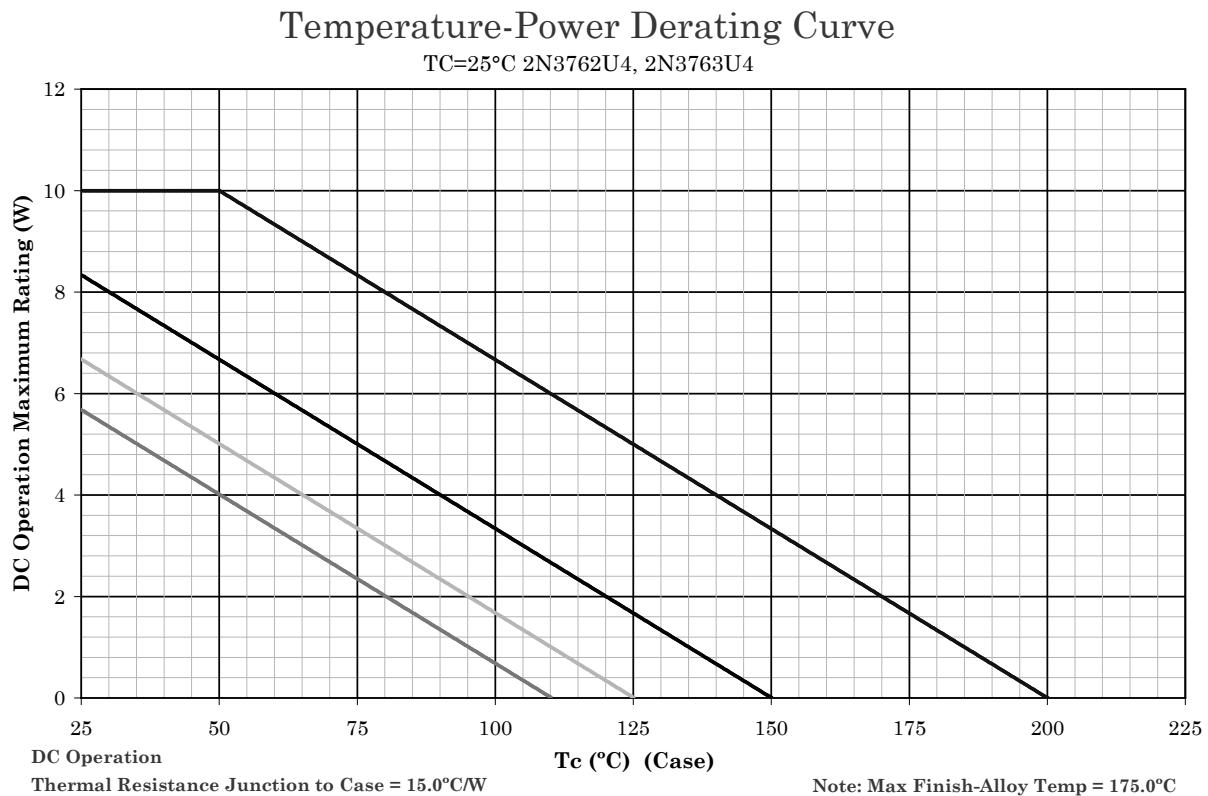
FIGURE 8. Derating for 2N3764, 2N3765 (TO-46).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See [1.3](#) herein.)
2. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
3. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

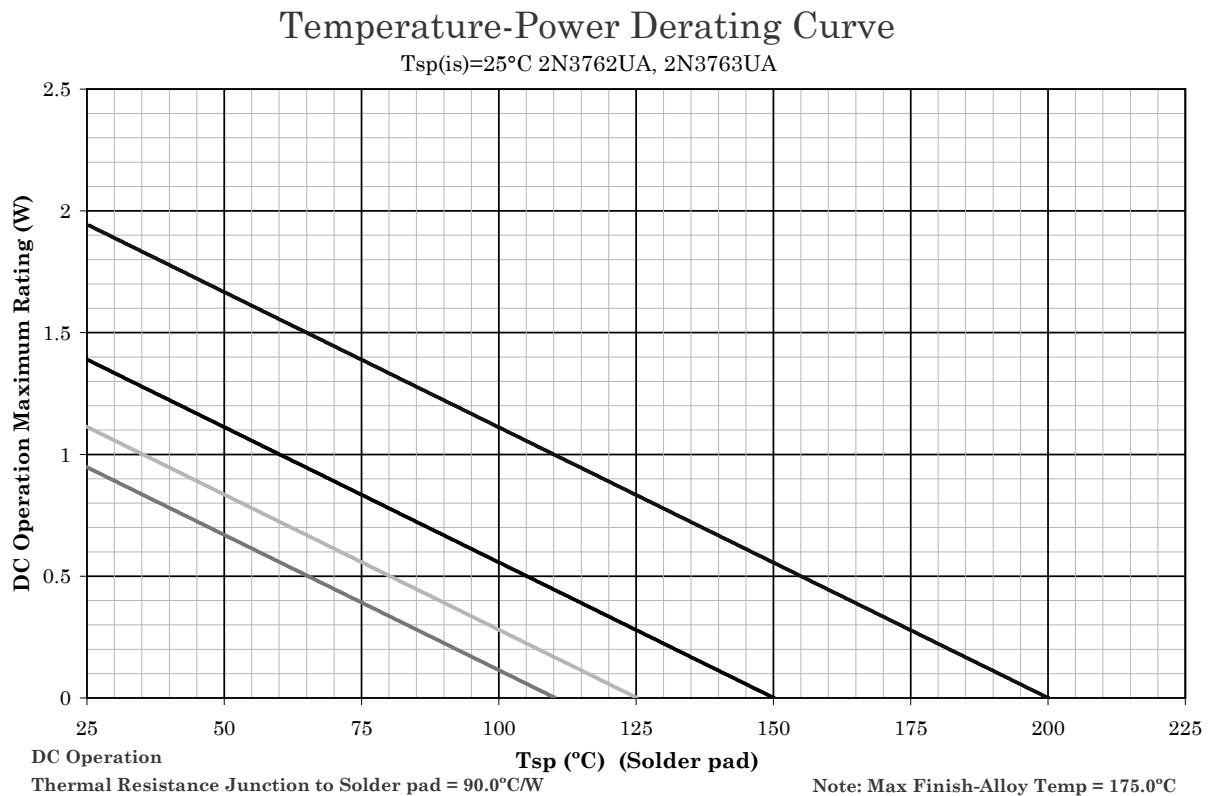
FIGURE 9. Derating for 2N3764, 2N3765(TO-46).



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

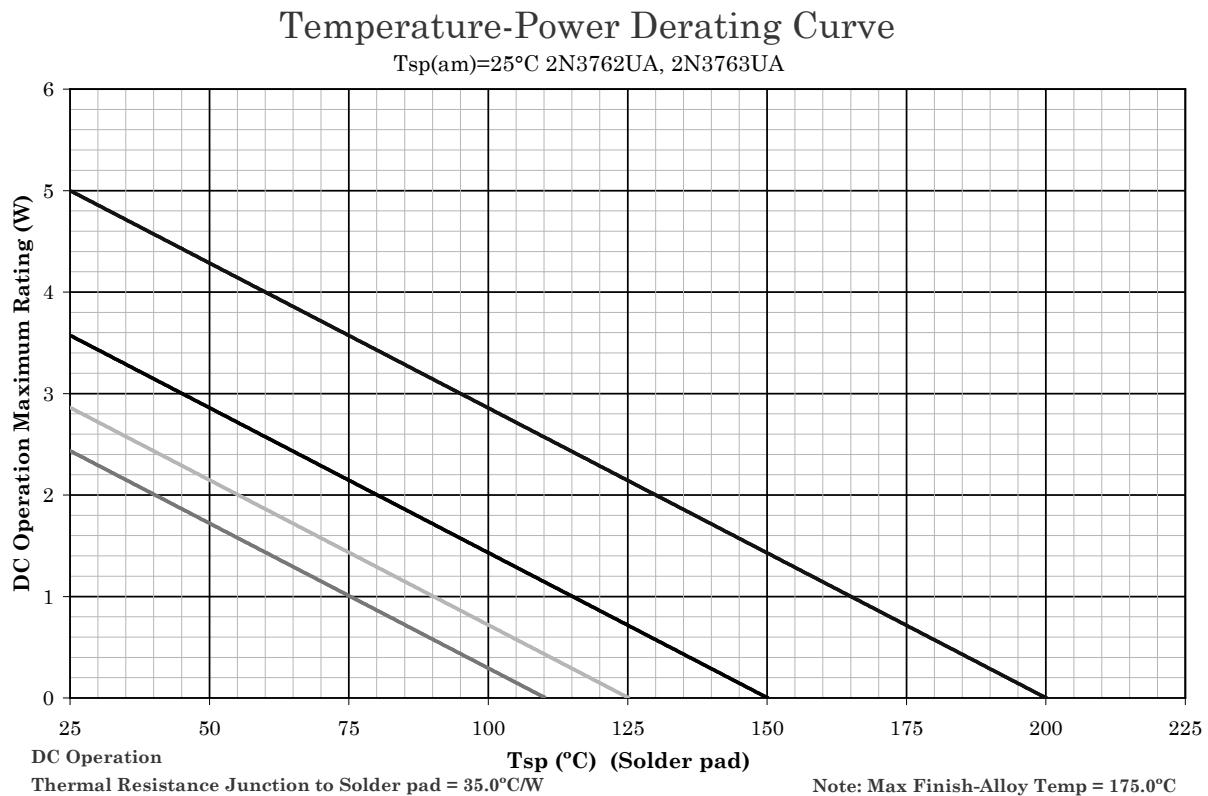
FIGURE 10. Derating for 2N3762U4, 2N3763U4.



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^{\circ}\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^{\circ}\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^{\circ}\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 11. Derating for 2N3762UA, 2N3763UA.



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 12. Derating for 2N3762UA, 2N3763UA.

Maximum Thermal Impedance
TO-5 and TO-39 Free Air Steel

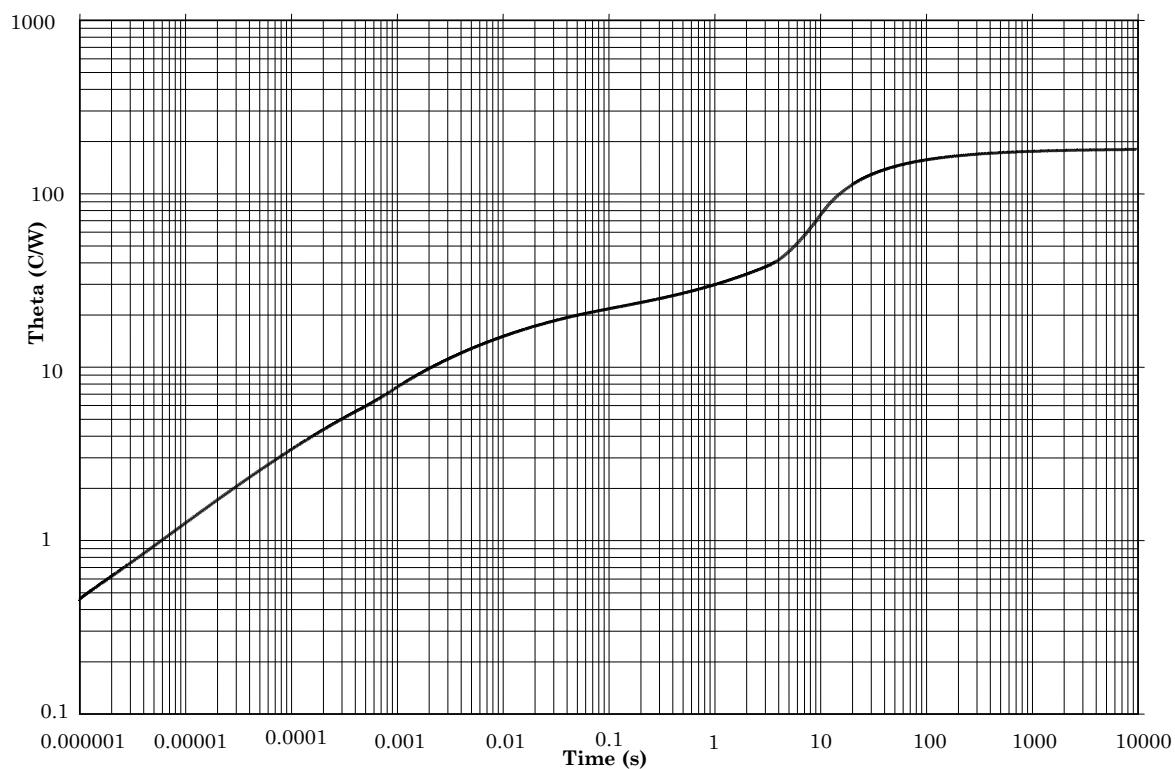


FIGURE 13A. Thermal impedance for 2N3762, 2N3763, 2N3762L, and 2N3763L (TO-5 and TO-39).

**Thermal Impedance for 2N3762, 2N3763, 2N3762L, 2N3763L
(TO-5 and TO-39 Free Air, kovar)**

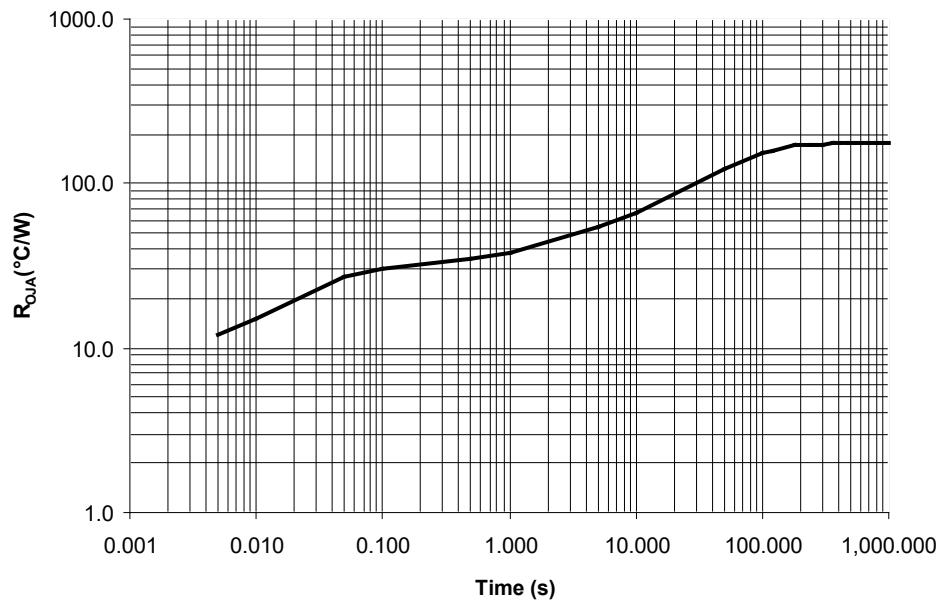


FIGURE 13B. Thermal impedance for 2N3762, 2N3763, 2N3762L, and 2N3763L (TO-5 and TO-39).

Maximum Thermal Impedance
TO-5 and TO-39 Case mount

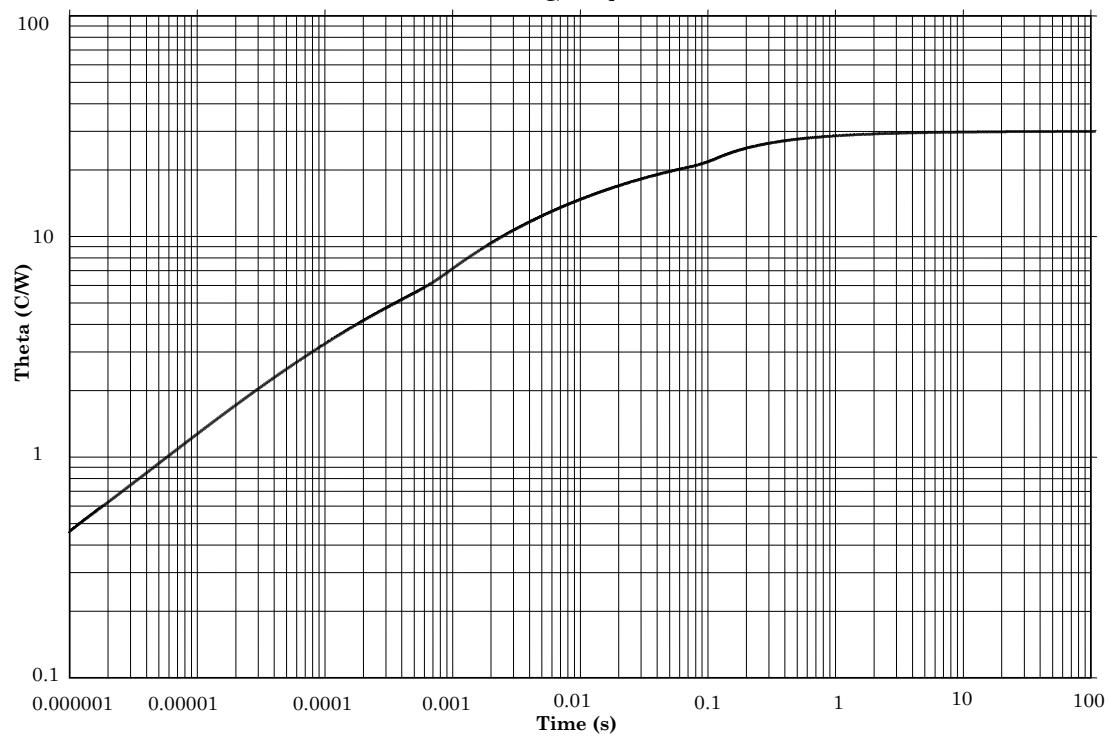


FIGURE 14A. Thermal impedance for 2N3762, 2N3763, 2N3762L, and 2N3763L (TO-5 and TO-39).

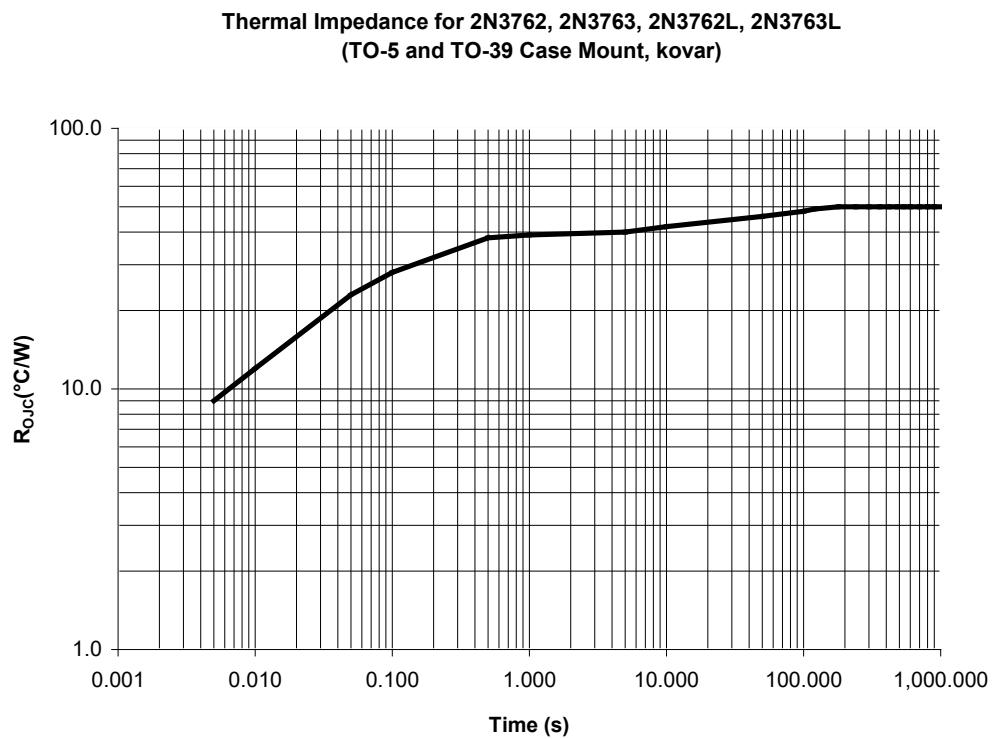


FIGURE 14B. Thermal impedance for 2N3762, 2N3763, 2N3762L, and 2N3763L (TO-5 and TO-39).

Maximum Thermal Impedance
TO-46 Free Air Steel

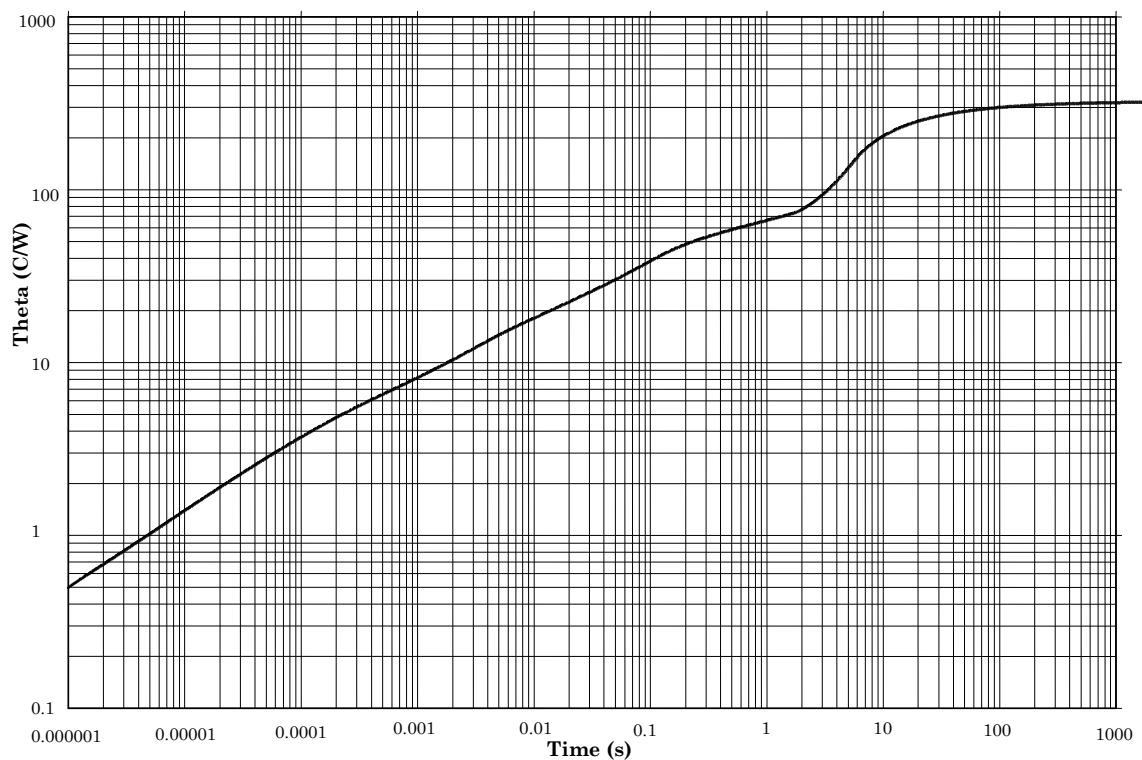


FIGURE 15A. Thermal impedance for 2N3764, 2N3765 (TO-46).

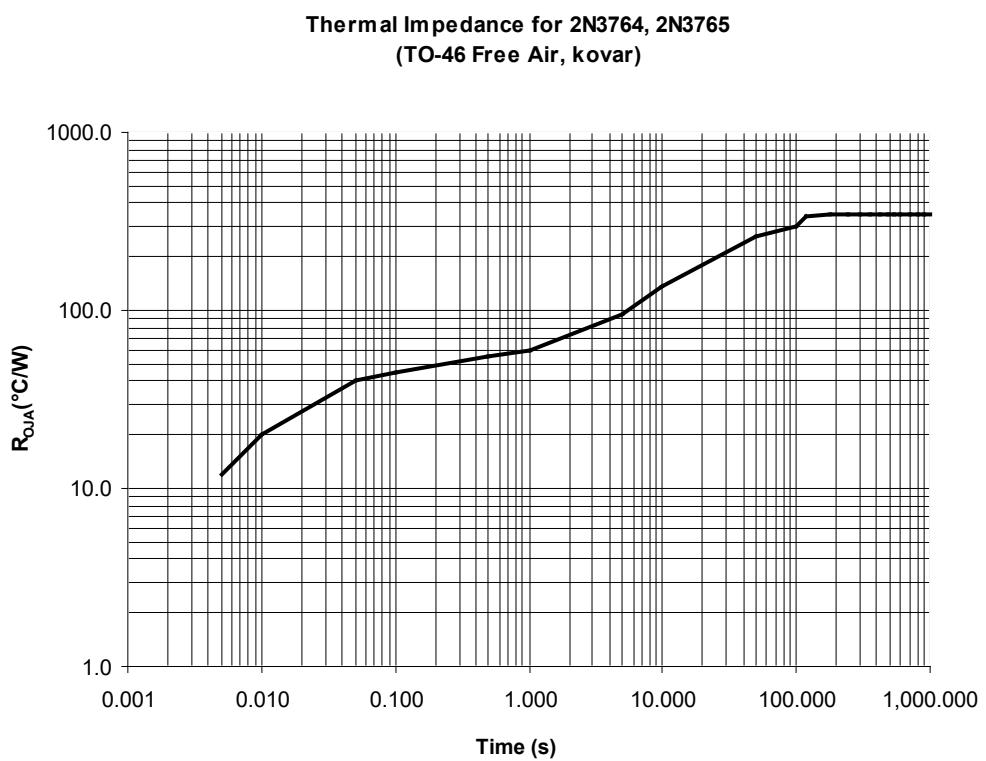


FIGURE 15B. Thermal impedance for 2N3764, 2N3765 (TO-46).

Maximum Thermal Impedance
TO-46 Case mount Steel

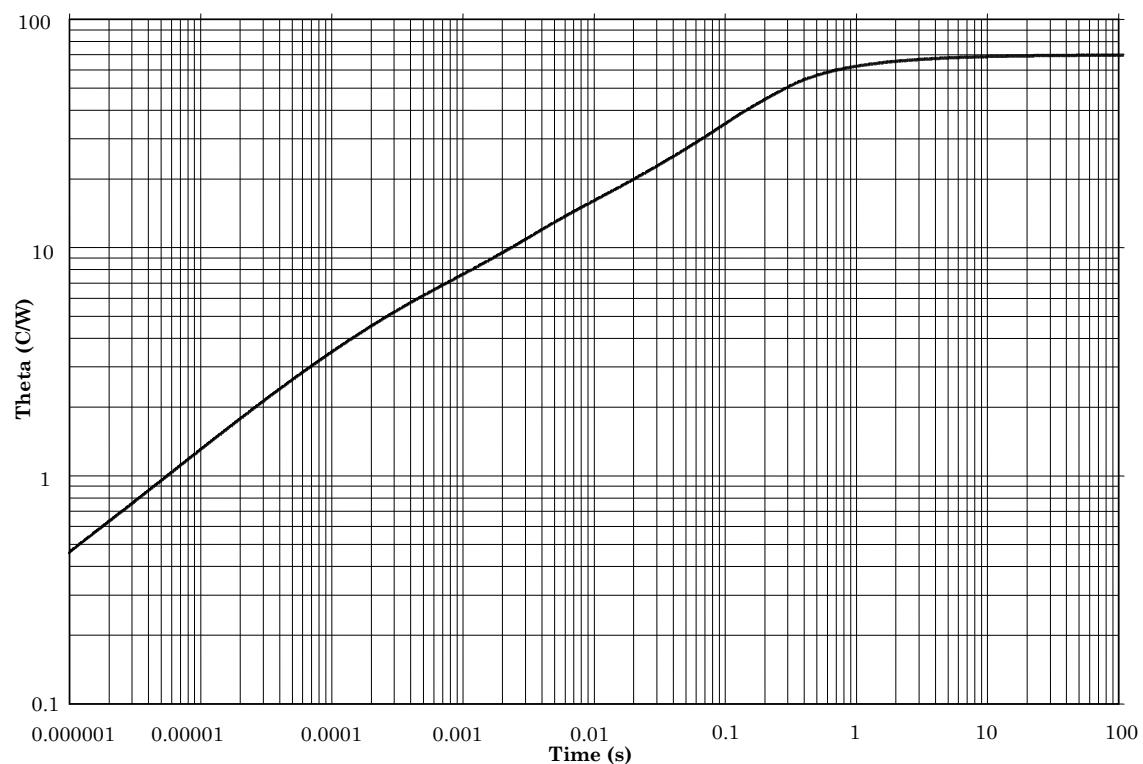


FIGURE 16A. Thermal impedance for 2N3764, 2N3765 (TO-46).

**Thermal Impedance for 2N3764, 2N3765
(TO-46 Case Mount, kovar)**

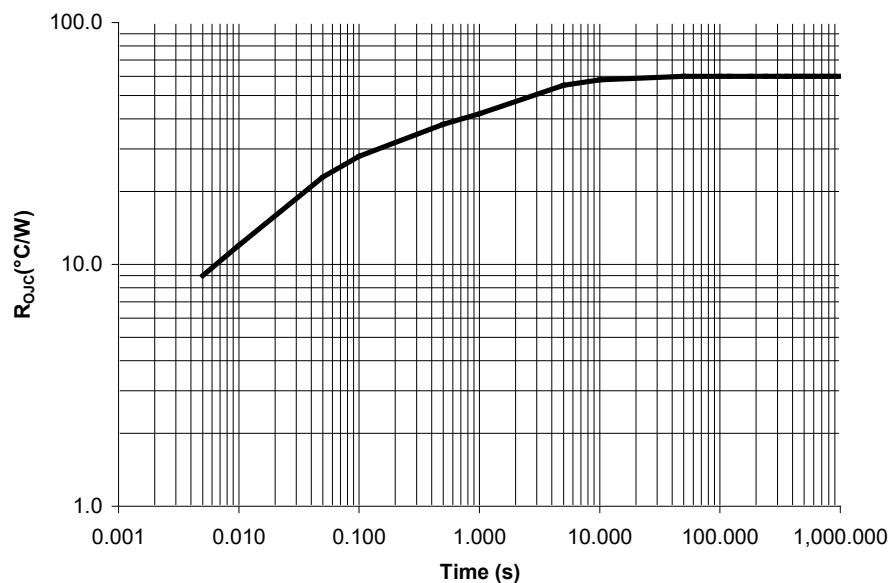


FIGURE 16B. Thermal impedance for 2N3764, 2N3765 (TO-46).

Maximum Thermal Impedance
U4 Case mount

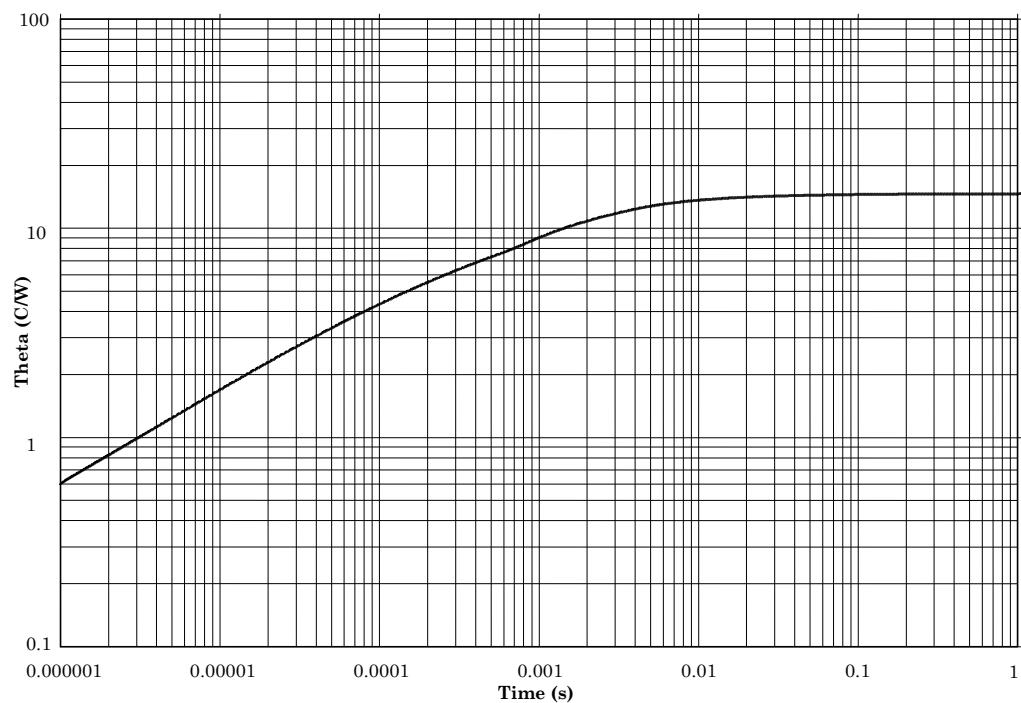


FIGURE 17. Thermal impedance for 2N3762U4, 2N3763U4 (U4).

Maximum Thermal Impedance
UA Solder Pad (Infinite Sink) mount

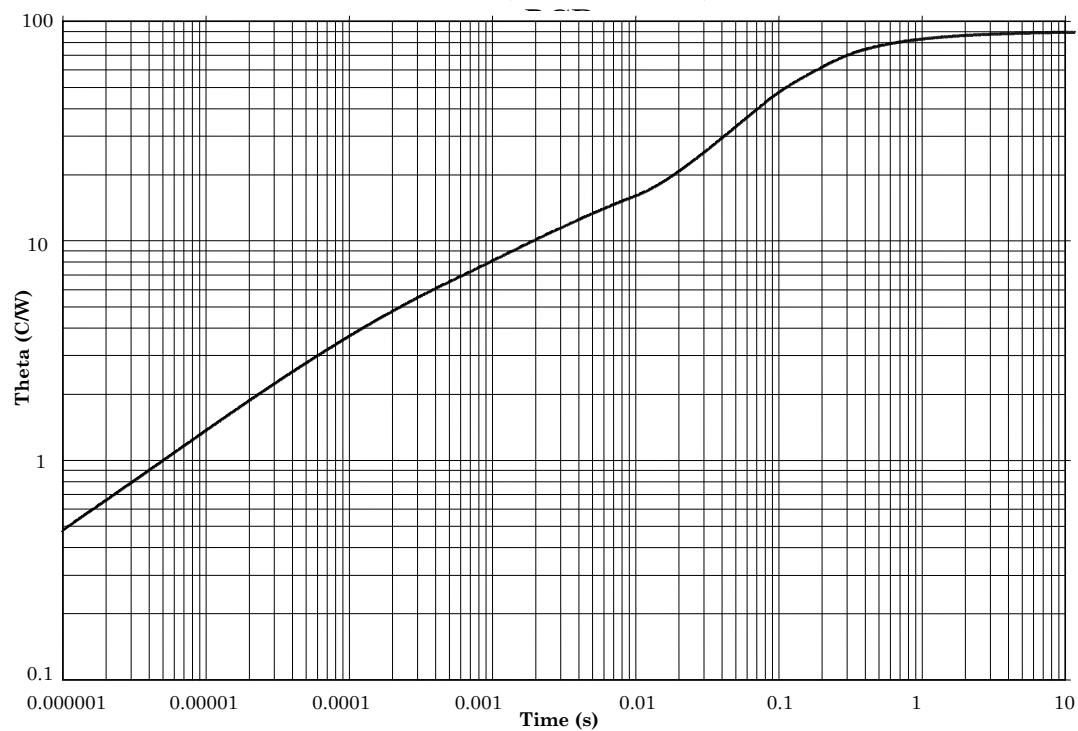


FIGURE 18. Thermal impedance for 2N3762UA, 2N3763UA (UA).

Maximum Thermal Impedance
UA Solder Pad (Adhesive Mount) to PCB

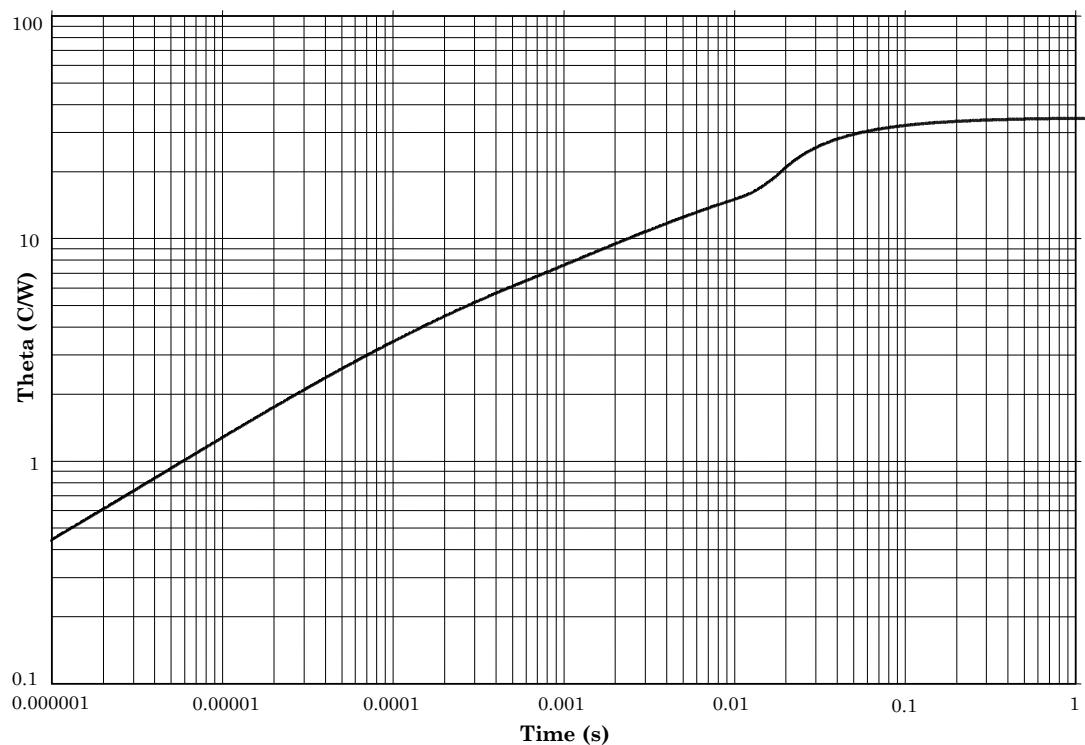
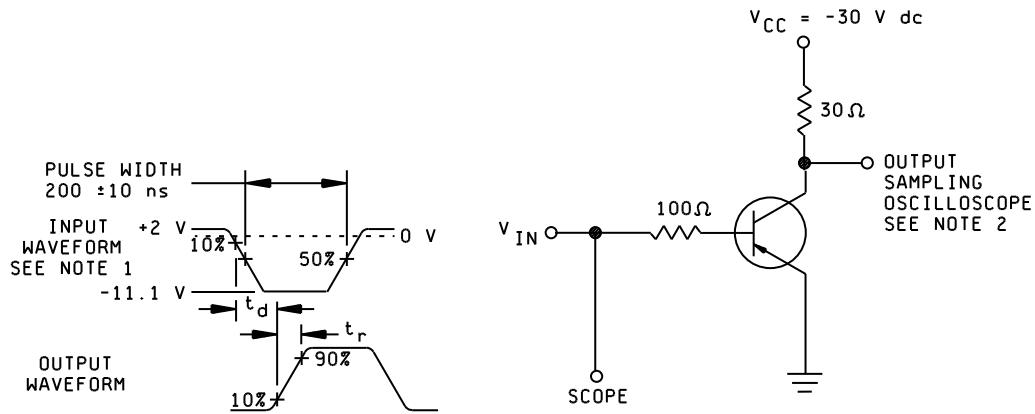


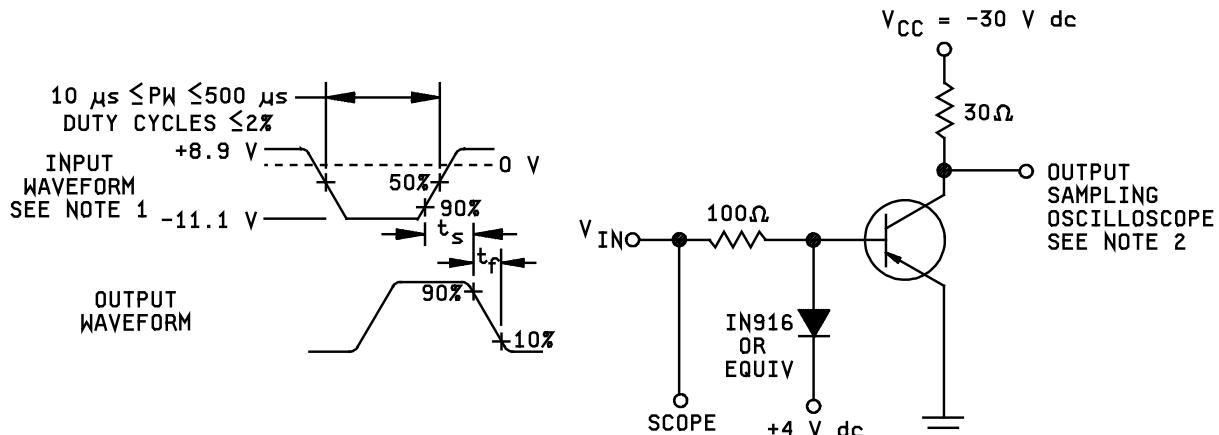
FIGURE 19. Thermal impedance for 2N3762UA, 2N3763UA (UA).



NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 2 ns, duty cycle ≤ 2 percent, and the generator source impedance shall be 50Ω .
2. Sampling oscilloscope: $Z_{in} \geq 100$ k Ω , $C_{in} \leq 12$ pF, rise time $\leq .1$ ns.
3. $I_{B1} = -100$ mA dc.

FIGURE 20. Pulse response test circuit for t_d and t_r .



NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 2 ns, duty cycle ≤ 2 percent, and the generator source impedance shall be 50Ω .
2. Sampling oscilloscope: $Z_{in} \geq 100$ k Ω , $C_{in} \leq 12$ pF, rise time $\leq .1$ ns.
3. $I_{B1} = +I_{B2} = -100$ mA dc.

FIGURE 21. Pulse response test circuit for t_s and t_f .

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.5.
- e. For acquisition of RHA designed devices, [Table II](#), subgroup 1 testing of Group D is optional. If subgroup 1 testing is desired, it must be specified in the contract.

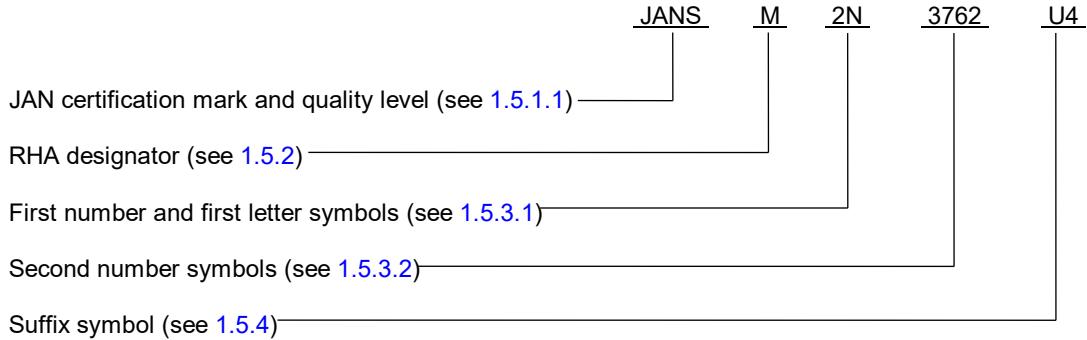
6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List ([QML-19500](#)) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: /VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

6.4 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example, JANHCA2N3762) will be identified on the [QML-19500](#).

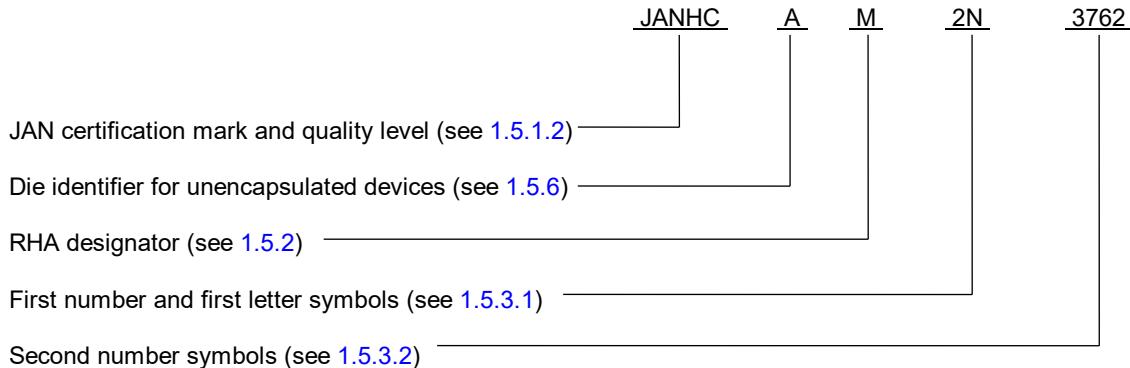
JANC ordering information		
PIN	Manufacturer	
	43611	
2N3762	JANHCA2N3762	JANKCA2N3762
2N3763	JANHCA2N3763	JANKCA2N3763
2N3764	JANHCA2N3764	JANKCA2N3764
2N3765	JANHCA2N3765	JANKCA2N3765

6.5 PIN construction example.

6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



6.5.2 Unencapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



6.6 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for types 2N3762, 2N3763, 2N3764, and 2N3765.			
JAN2N3762	JANTX2N3762	JANTXV2N3762	JANS#2N3762
JAN2N3762L	JANTX2N3762L	JANTXV2N3762L	JANS#2N3762L
JAN2N3762U4	JANTX2N3762U4	JANTXV2N3762U4	JANS#2N3762U4
JAN2N3762UA	JANTX2N3762UA	JANTXV2N3762UA	JANS#2N3762UA
JAN2N3763	JANTX2N3763	JANTXV2N3763	JANS#2N3763
JAN2N3763L	JANTX2N3763L	JANTXV2N3763L	JANS#2N3763L
JAN2N3763U4	JANTX2N3763U4	JANTXV2N3763U4	JANS#2N3763U4
JAN2N3763UA	JANTX2N3763UA	JANTXV2N3763UA	JANS#2N3763UA
JAN2N3764	JANTX2N3764	JANTXV2N3764	JANS#2N3764
JAN2N3765	JANTX2N3765	JANTXV2N3765	JANS#2N3765
JANHCA#2N3762	JANHCA#2N3764	JANKCA#2N3762	JANKCA#2N3762
JANHCA#2N3763	JANHCA#2N3765	JANKCA#2N3763	JANKCA#2N3763

(1) The number sign (#) represent one of five RHA designators available (M, D, P, L, R, F, G, or H). The PIN is also available without a RHA designator.

* 6.7 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:

Army - CR
Navy - EC
Air Force - 85
DLA - CC
NASA - NA

Preparing activity:

DLA - CC

(Project 5961-2020-048)

Review activities:

Army - MI
Navy - AS, MC
* Air Force - 19, 71

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