# Application Note: SQV256

## High Efficiency Fast Response
## 6A, 23V Input Synchronous Step Down Regulator

## General Description

The SQV256 develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 6A current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SQV256 operates over a wide input voltage range from 4V to 23V. The DC/DC regulator adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. The device provides various protection features for reliable operation. In addition, it operates at pseudo-constant frequency of 600kHz to minimize the size of inductor and capacitor.

## Ordering Information

SQV256 □(□□)□
- └ Temperature Code
- Package Code
- Optional Spec Code

| Ordering Number | Package type | Note |
|---|---|---|
| SQV256RAC | QFN3×3-20 | -- |

## Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 38/19 mΩ
- Wide Input Voltage Range: 4-23V
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal 1.3ms Soft-start Limits the Inrush Current
- Pseudo-constant Frequency: 600kHz
- 6A Output Current Capability
- ±1% Internal Reference Voltage
- PFM/PWM Selectable Light Load Operation Mode
- Optional Bypass Input
- Power Good Indicator
- Output Discharge Function
- Output Current Limit Protection
- Hiccup Mode Output Short Circuit Protection
- Output Over Voltage Protection
- Input UVLO
- Over Temperature Protection with Auto Recovery
- RoHS Compliant and Halogen Free
- Compact Package: QFN3×3-20

## Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

## Typical Applications

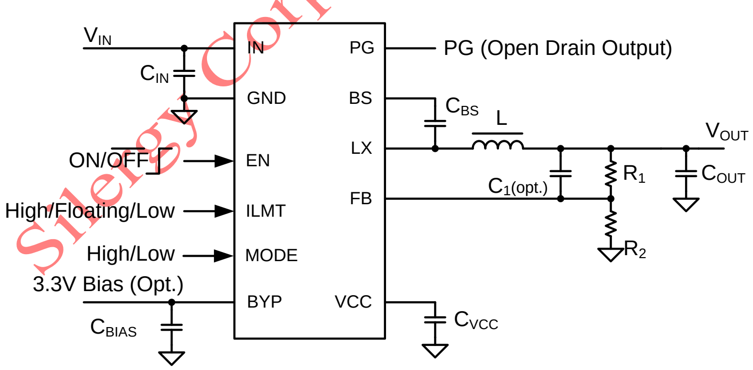



Figure1. Schematic Diagram

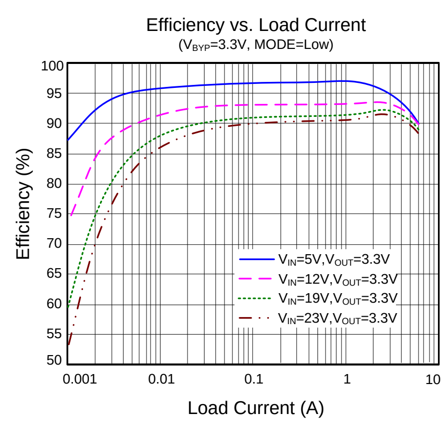
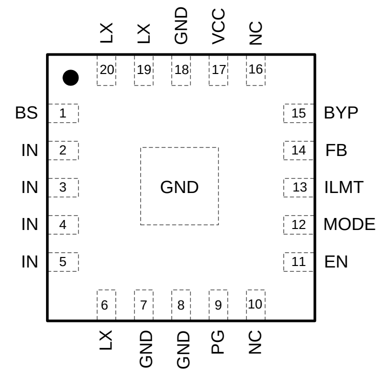



Figure2. Efficiency vs. Load Current

## **Pinout** (top view)




(QFN3×3-20)

Top Mark: DBY*xyz* **(**Device code: DBY, ***x=year code, y=week code, z= lot number code*****)**

| Pin Name | Pin Number | Pin Description |
|---|---|---|
| BS | 1 | Boot-strap pin. Supply high side gate driver. Connect a 0.1µF ceramic capacitor between the BS pin and the LX pin. |
| IN | 2,3,4,5 | Input pin. Decouple this pin to the GND pin with at least a 10µF ceramic capacitor. |
| LX | 6,19,20 | Inductor pin. Connect this pin to the switching node of the inductor. |
| GND | 7,8,18,EP | Ground pin. |
| PG | 9 | Power good Indicator. Open-drain output when the output voltage is within 90% to 120% of regulation point. |
| NC | 10, 16 | Not connected. |
| EN | 11 | Enable pin. Pull this pin high to turn on the IC. Do not leave this pin floating. |
| MODE | 12 | Operating mode selection under light load. Pull this pin low for PFM operating, and pull this pin high for PWM operation. Do not leave this pin floating. |
| ILMT | 13 | Output current limit threshold selection. |
| FB | 14 | Output feedback pin. Connected to the center point of the resistor divider. |
| BYP | 15 | External 3.3V bypass power supply input. Decouple this pin to the GND with a 1µF ceramic capacitor. Leave this pin floating if it is not used. |
| VCC | 17 | Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Decouple this pin to the GND with a 2.2µF ceramic capacitor. |

## Block Diagram

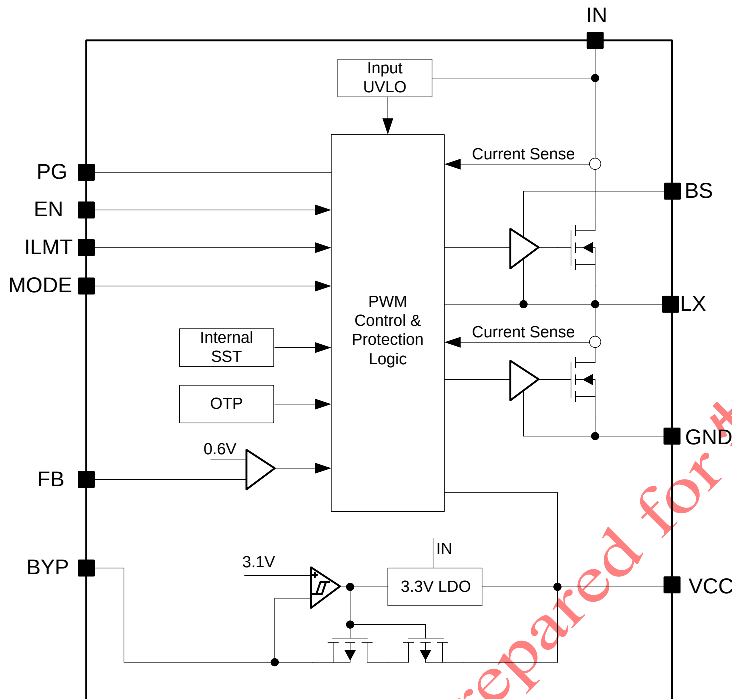



Figure3. Block Diagram



## Absolute Maximum Ratings (Note 1)

IN ---------------------------------------------------------------- 25V
BS-LX ---------------------------------------------------------------- 4V
EN, ILMT, MODE, PG, LX ---------------------------------------------------------------- 25V
VCC, FB ---------------------------------------------------------------- 4V
BYP ---------------------------------------------------------------- 6V
Power Dissipation,
$P_D$ @ $T_A$ = 25°C QFN3×3-20 ---------------------------------------------------------------- 3.3W
Package Thermal Resistance (Note 2)
$\theta_{JA}$, QFN3×3-20 ---------------------------------------------------------------- 30°C/W
$\theta_{JC}$, QFN3×3-20 ---------------------------------------------------------------- 4.5°C/W
Junction Temperature Range ---------------------------------------------------------------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------------------------------------------------------------- 260°C
Storage Temperature Range ---------------------------------------------------------------- -65°C to 150°C
Dynamic LX voltage in 10ns duration ---------------------------------------------------------------- IN+3V to GND-5V

## Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------------------------------------------------------------- 4V to 23V
Junction Temperature Range ---------------------------------------------------------------- -40°C to 125°C
Ambient Temperature Range ---------------------------------------------------------------- -40°C to 85°C

## Electrical Characteristics

($V_{IN}$ = 12V, $T_A$ = 25°C unless otherwise specified)

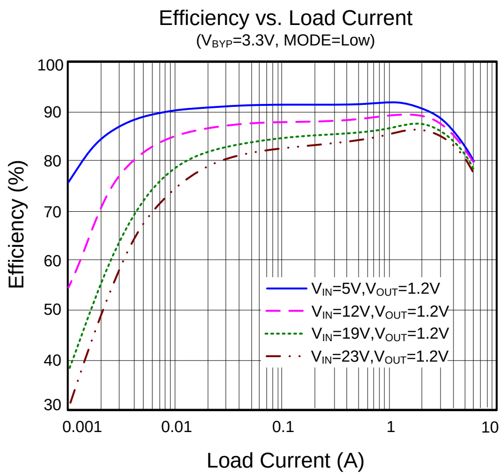
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{IN}$ | | 4 | | 23 | V |
| Input UVLO Threshold | $V_{UVLO}$ | $V_{IN}$ rising | | | 3.9 | V |
| UVLO Hysteresis | $V_{HYS}$ | | | 0.1 | | V |
| Quiescent Current | $I_Q$ | $I_{OUT}$=0, $V_{OUT}$=$V_{SET}$×105% | | 120 | 145 | μA |
| Shutdown Current | $I_{SHDN}$ | EN=0, | | 6 | 10 | μA |
| Feedback Reference Voltage | $V_{REF}$ | | 0.594 | 0.6 | 0.606 | V |
| Top FET RON | $R_{DS(ON)1}$ | | | 38 | | mΩ |
| Bottom FET RON | $R_{DS(ON)2}$ | | | 19 | | mΩ |
| Output Discharge Current | $I_{DIS}$ | | | 70 | | mA |
| Top FET Current Limit | $I_{LMT,HSFET}$ | | | 17 | | A |
| Bottom FET Current Limit | $I_{LMT, LSFET1}$ | ILMT=Low | 6.5 | 7.8 | 9.1 | A |
| | | ILMT=Floating | 9.3 | 10.6 | 11.9 | A |
| | | ILMT=High | 12 | 13.3 | 14.8 | A |
| Bottom FET Reverse Current Limit | $I_{LIM,LSFET2}$ | | 1.5 | 3 | 4.5 | A |
| Soft-start Time | $t_{SS}$ | | | 1.3 | | ms |
| EN/MODE Input Voltage High | $V_{ENH}$ | | 1 | | | V |
| EN/MODE Input Voltage Low | $V_{ENL}$ | | | | 0.4 | V |
| ILMT Input Voltage High | $V_{ILMTH}$ | | Vcc-0.5 | | | V |
| ILMT Input Voltage Low | $V_{ILMTL}$ | | | | 0.5 | V |
| Switching Frequency | $f_{OSC}$ | $V_{OUT}$=5V | 510 | 600 | 690 | kHz |
| Min ON Time | $t_{ON,MIN}$ | $V_{IN}$=$V_{INMAX}$ | | 50 | | ns |
| Min OFF Time | $t_{OFF,MIN}$ | | | 150 | | ns |
| VCC Output Voltage | $V_{CC}$ | With 1mA load | 3.15 | 3.3 | 3.45 | V |
| Output Over Voltage Threshold | $V_{OVP}$ | $V_{FB}$ rising | 115 | 120 | 125 | %$V_{REF}$ |
| Output Over Voltage Hysteresis | $V_{OVP,HYS}$ | | | 1.5 | | %$V_{REF}$ |
| Output OVP Delay | $t_{OVP,DLY}$ | | | 20 | | μs |
| Output Under Voltage Protection Threshold | $V_{UVP}$ | $V_{FB}$ falling | 57.5 | 62.5 | 67.5 | %$V_{REF}$ |
| Output UVP Delay | $t_{UVP,DLY}$ | | | 200 | | μs |
| Power Good Threshold | $V_{PG}$ | $V_{FB}$ rising (Good) | | 92 | | %$V_{REF}$ |
| Power Good Hysteresis | $V_{PG,HYS}$ | | | 1.5 | | %$V_{REF}$ |
| Power Good Delay | $t_{PG,RISING}$ | Low to high | | 200 | | μs |
| | $t_{PG,FALLING}$ | High to low | | 10 | | μs |
| Bypass Switch Turn-on Voltage | $V_{BYP}$ | | 2.97 | 3.1 | 3.21 | V |
| Bypass Switch Switchover Hysteresis | $V_{BYP,HYS}$ | | | 0.15 | | V |
| Bypass Switch OVP | $V_{BYP,OVP}$ | | | 120 | | %$V_{CC}$ |
| Thermal Shutdown Temperature | $T_{SD}$ | | | 150 | | °C |
| Thermal Shutdown hysteresis | $T_{HYS}$ | | | 15 | | °C |

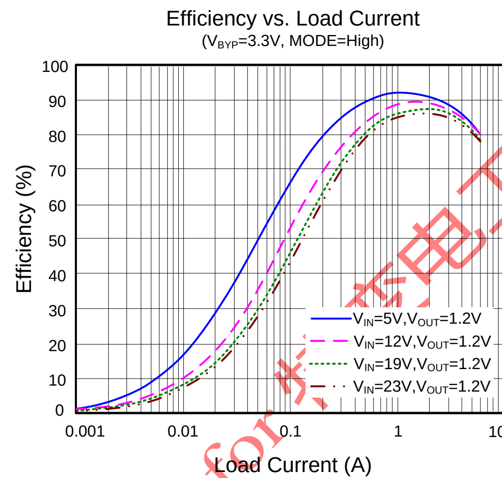
**Note 1**: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

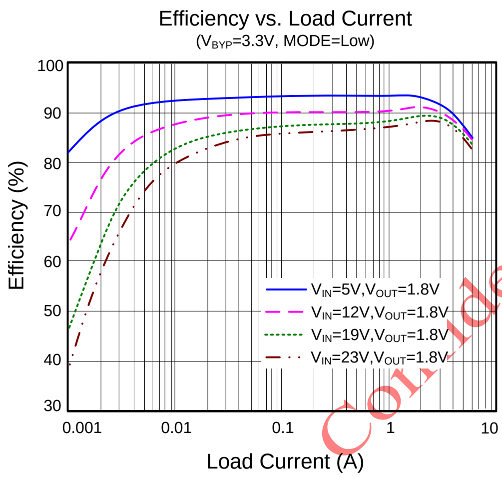
**Note 2**: Package thermal resistance is measured in the natural convection at $T_A$ = 25°C on a four-layer Silergy evaluation board.

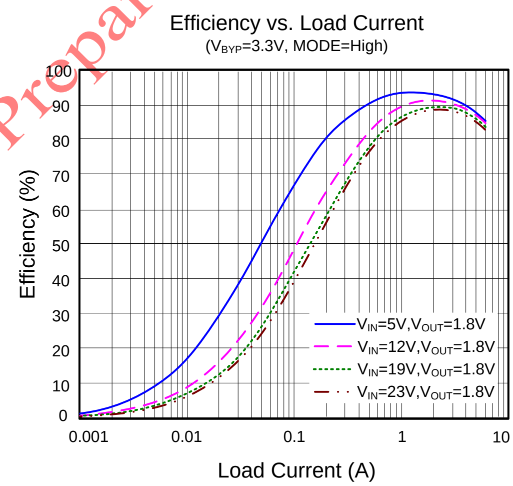
**Note 3:** The device is not guaranteed to function outside its operating conditions.

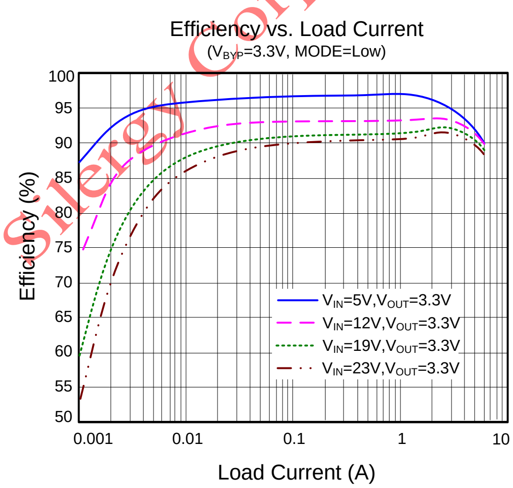
# Typical Performance Characteristics

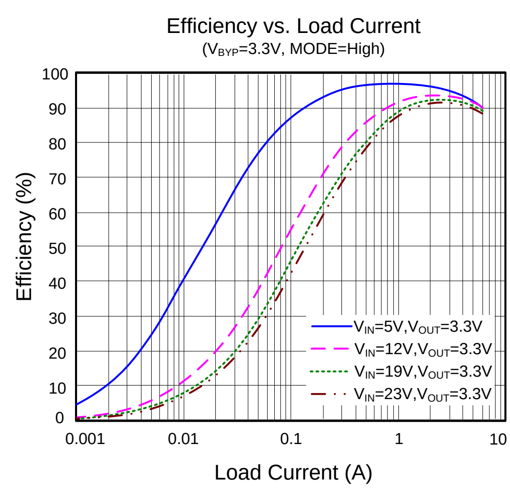


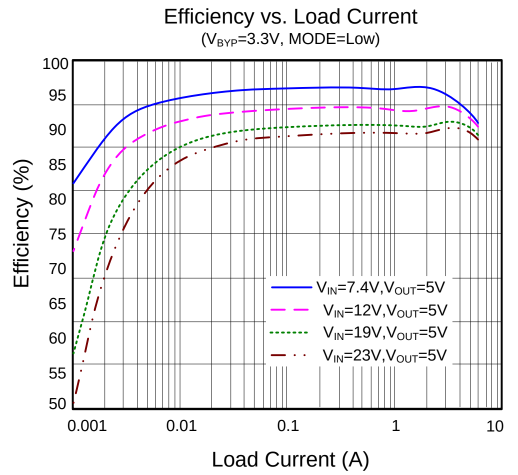



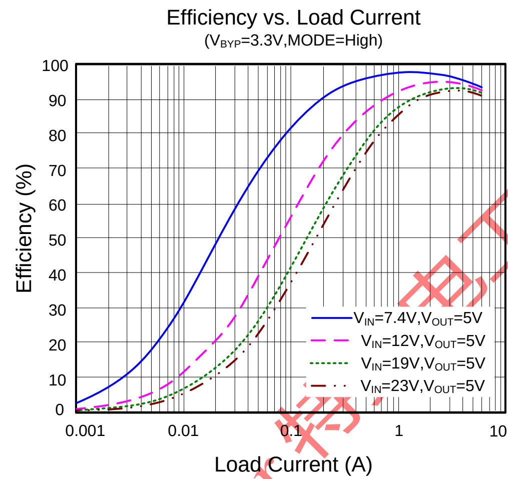



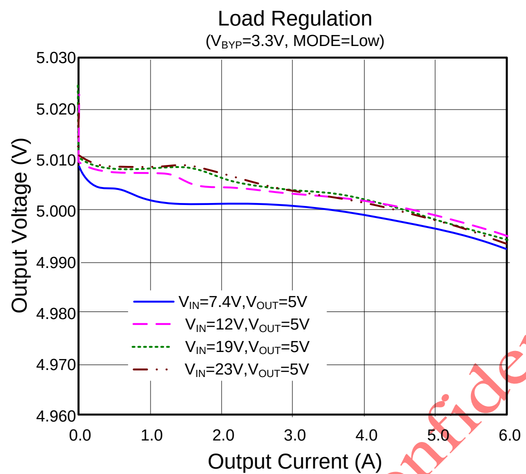



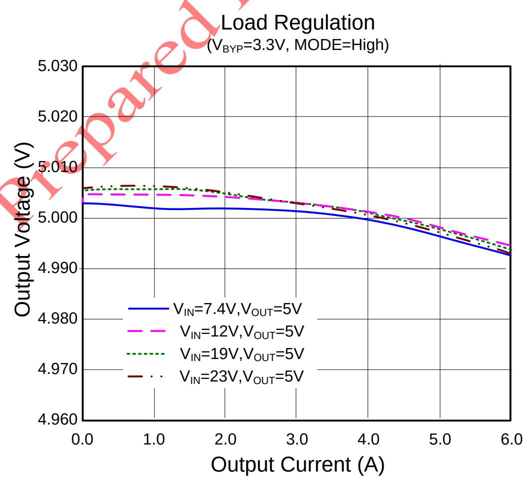



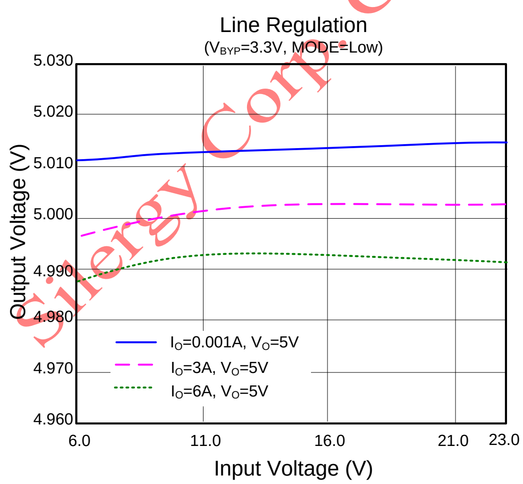



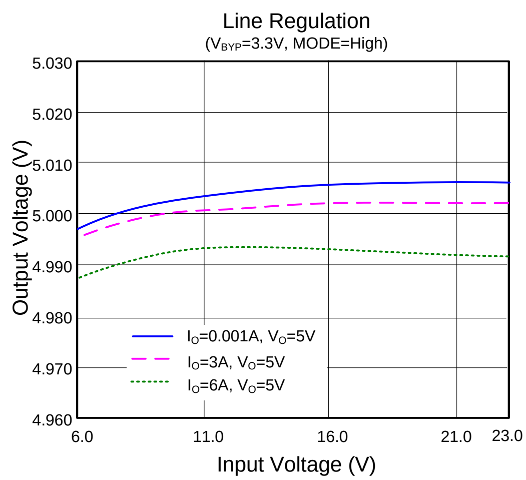

Efficiency vs. Load Current
(VBYP=3.3V, MODE=Low)
Efficiency (%)
Load Current (A)
VIN=7.4V,VOUT=5V
VIN=12V,VOUT=5V
VIN=19V,VOUT=5V
VIN=23V,VOUT=5V


Efficiency vs. Load Current
(VBYP=3.3V,MODE=High)
Efficiency (%)
Load Current (A)
VIN=7.4V,VOUT=5V
VIN=12V,VOUT=5V
VIN=19V,VOUT=5V
VIN=23V,VOUT=5V


Load Regulation
(VBYP=3.3V, MODE=Low)
Output Voltage (V)
Output Current (A)
VIN=7.4V,VOUT=5V
VIN=12V,VOUT=5V
VIN=19V,VOUT=5V
VIN=23V,VOUT=5V

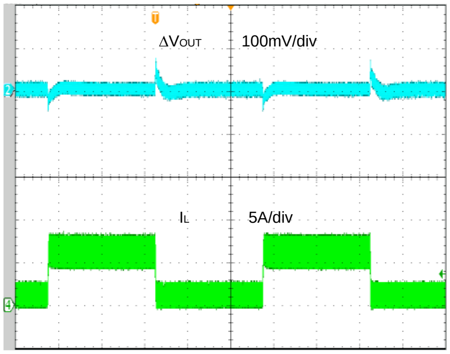

Load Regulation
(VBYP=3.3V, MODE=High)
Output Voltage (V)
Output Current (A)
VIN=7.4V,VOUT=5V
VIN=12V,VOUT=5V
VIN=19V,VOUT=5V
VIN=23V,VOUT=5V


Line Regulation
(VBYP=3.3V, MODE=Low)
Output Voltage (V)
Input Voltage (V)
IO=0.001A, VO=5V
IO=3A, VO=5V
IO=6A, VO=5V


Line Regulation
(VBYP=3.3V, MODE=High)
Output Voltage (V)
Input Voltage (V)
IO=0.001A, VO=5V
IO=3A, VO=5V
IO=6A, VO=5V

Load Transient

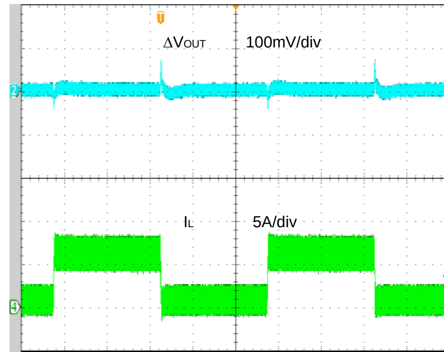
($V_{IN}$=12V, $V_{OUT}$=3.3V, $I_{OUT}$=0.6-6A, MODE=Low)




Time (200μs/div)

Load Transient

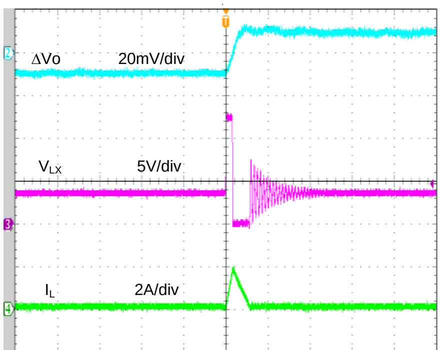
($V_{IN}$=12V, $V_{OUT}$=3.3V, $I_{OUT}$=0.6-6A, MODE=High)




Time (200μs/div)

Output Ripple

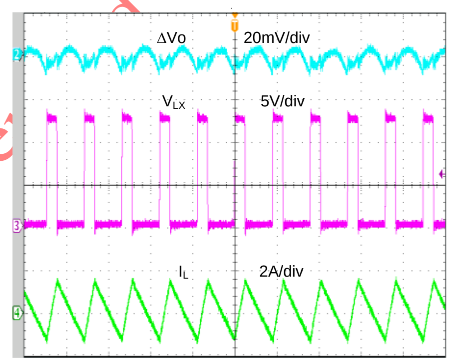
($V_{IN}$=12V, $V_O$=3.3V, $I_O$=0A, MODE=Low)




Time (2μs/div)

Output Ripple

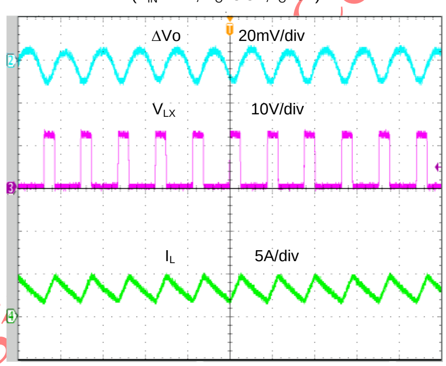
($V_{IN}$=12V, $V_O$=3.3V, $I_O$=0A, MODE=High)




Time (2μs/div)

Output Ripple

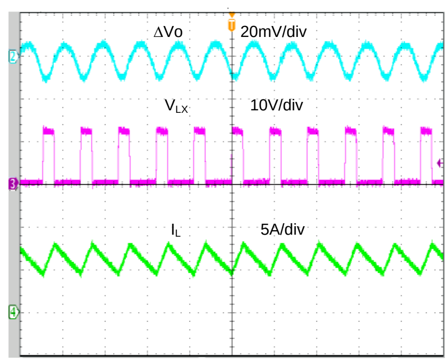
($V_{IN}$=12V, $V_O$=3.3V, $I_O$=3A)




Time (2μs/div)

Output Ripple

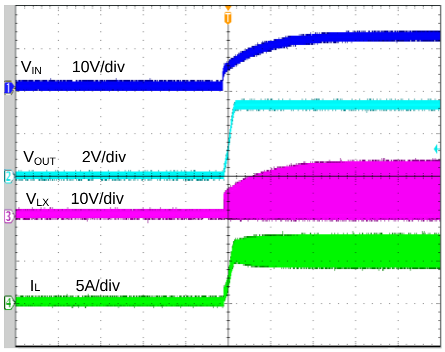
($V_{IN}$=12V, $V_O$=3.3V, $I_O$=6A)




Time (2μs/div)

Startup from $V_{IN}$

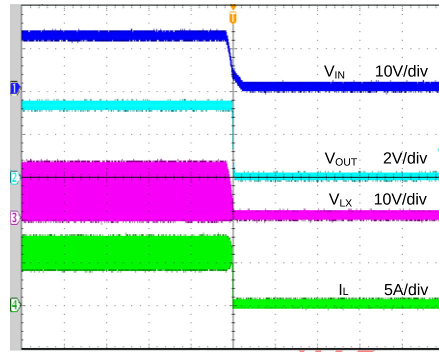
($V_{IN}$=12V, $V_{OUT}$=3.3V, $I_O$=6A)




Time (4ms/div)

Shutdown from $V_{IN}$

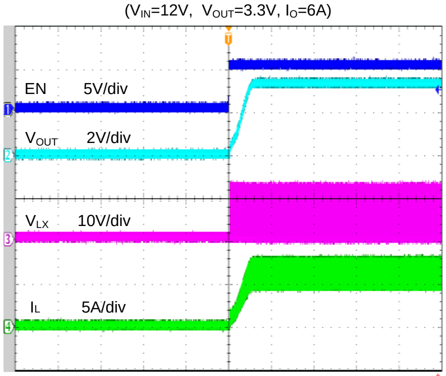
($V_{IN}$=12V, $V_{OUT}$=3.3V, $I_O$=6A)




Time (4ms/div)

Startup from Enable

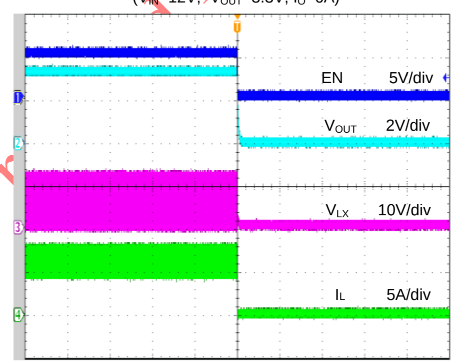
($V_{IN}$=12V, $V_{OUT}$=3.3V, $I_O$=6A)




Time (2ms/div)

Shutdown from Enable

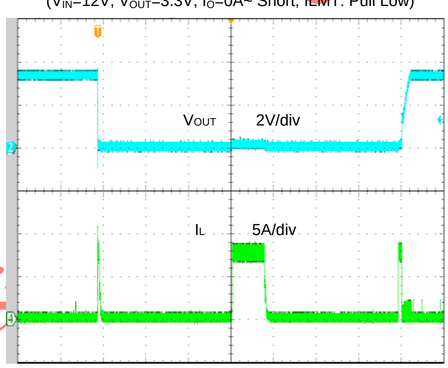
($V_{IN}$=12V, $V_{OUT}$=3.3V, $I_O$=6A)




Time (2ms/div)

Short Circuit Protection

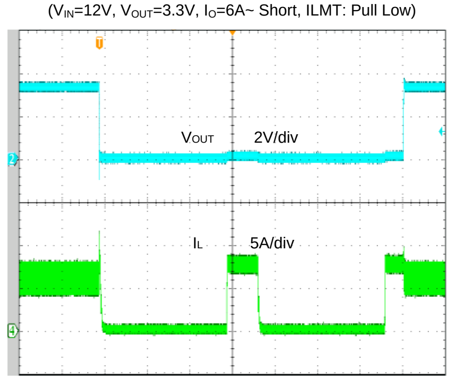
($V_{IN}$=12V, $V_{OUT}$=3.3V, $I_O$=0A~ Short, ILMT: Pull Low)




Time (4ms/div)

Short Circuit Protection

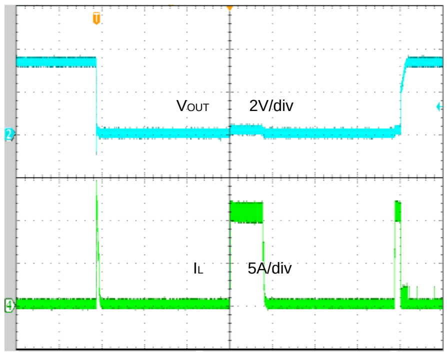
($V_{IN}$=12V, $V_{OUT}$=3.3V, $I_O$=6A~ Short, ILMT: Pull Low)




Time (4ms/div)

Short Circuit Protection

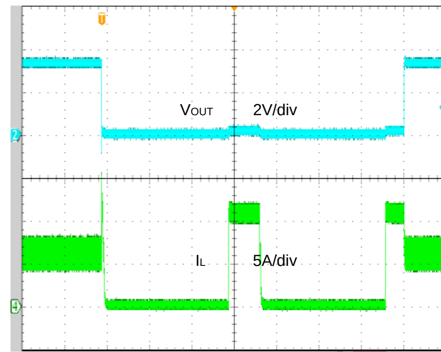
($V_{IN}$=12V, $V_{OUT}$=3.3V, $I_O$=0A~ Short, ILMT: Floating)




Time (4ms/div)

Short Circuit Protection

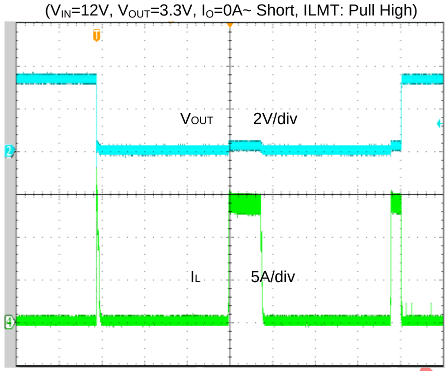
($V_{IN}$=12V, $V_{OUT}$=3.3V, $I_O$=6A~ Short, ILMT: Floating)




Time (4ms/div)

Short Circuit Protection

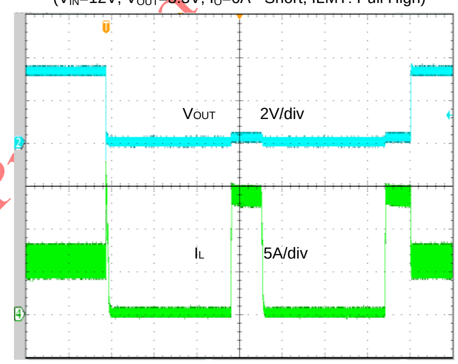
($V_{IN}$=12V, $V_{OUT}$=3.3V, $I_O$=0A~ Short, ILMT: Pull High)




Time (4ms/div)

Short Circuit Protection

($V_{IN}$=12V, $V_{OUT}$=3.3V, $I_O$=6A~ Short, ILMT: Pull High)




Time (4ms/div)

# Operation

The SQV256 develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 6A current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SQV256 operates over a wide input voltage range from 4V to 23V. The DC/DC regulator adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. The device provides various protection features for reliable operation. In addition, it operates at pseudo-constant frequency of 600kHz to minimize the size of inductor and capacitor.

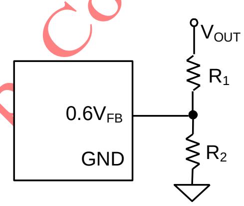
# Applications Information

Because of the high integration in the SQV256, the application circuit based on this regulator is rather simple. Only the input capacitor $C_{IN}$, the output capacitor $C_{OUT}$, the output inductor L and the feedback resistors ($R_1$ and $R_2$) need to be selected for the targeted applications specifications.

**Feedback Resistor Dividers $R_1$ and $R_2$:**

Choose $R_1$ and $R_2$ to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both $R_1$ and $R_2$. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If $V_{OUT}$ is 1.2V, $R_1$=100kΩ is chosen, then using the following equation, $R_2$ can be calculated to be 100kΩ:

$$R_2 = \frac{0.6V}{V_{OUT}-0.6V} R_1$$




**Input Capacitor $C_{IN}$:**

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}.$$

To minimize the potential noise problem, a typical X5R or better grade ceramic capacitor should be placed really close to the IN and the GND pins. Care should be taken to minimize the loop area formed by $C_{IN}$, and the IN/GND pins. In this case, a 10μF low ESR ceramic capacitor is recommended.

**Output Capacitor $C_{OUT}$:**

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For most applications, an X5R or better grade ceramic capacitor greater than 66μF capacitance can work well. The capacitance derating with DC voltage must be considered.

**Output Inductor L:**

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 30~40% of the maximum output current. In PWM mode operation, 30% of the maximum output current is suggested, in order not to trigger bottom FET reverse current limit at light load condition. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 30\%}$$

Where fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SQV256 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

**Current Limit Setting**

The SQV256 features both cycle by cycle peak and valley current limit. The high side MOSFET is turned off and low side MOSFET is turned on when peak current limit is triggered. When the valley current limit is triggered, the device will not allow high side MOSFET turning on until the valley current drops below the threshold. The valley current limit threshold is selectable by pulling the ILMT pin low, high or leaving it floating.

## Soft-start

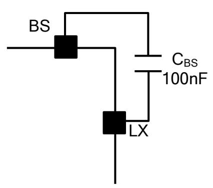
In order to limit the input inrush current, the SQV256 has a built-in soft-start circuit which controls the output voltage ramp up speed during startup. The typical soft-start time is 1.3ms.

## Enable Operation

Pulling the EN pin low will shut down the device. During shutdown mode, the SQV256 shutdown current drops to lower than 10μA. Driving the EN pin high will turn on the IC again.

## External Bootstrap Capacitor

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.




## VCC LDO and BYP Input

The 3.3V VCC LDO provides the power supply for internal control and drive circuit. Bypass this pin to ground with a 2.2μF ceramic capacitor. The control and drive circuit can also be powered by external 3.3V power supply. When a 3.3V external power supply is connected to the BYP pin, the VCC LDO is turned off and the switch between BYP and VCC is turned on. The overall efficiency may be improved by connecting the BYP pin to external 3.3V switching power supply. Leave the BYP pin floating if this feature is not used.

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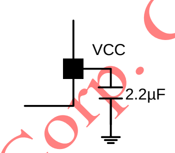



## Power Good Indication

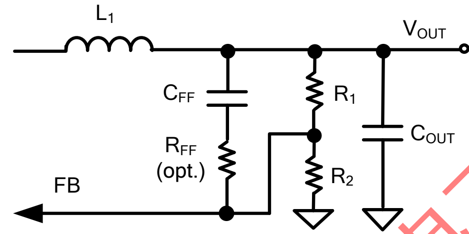
PG is an open-drain output pin. This pin will be pulled to ground if output voltage is lower than 90% or higher than 120% of regulation voltage. Otherwise this pin will go to a high impedance state.

## Light Load Operation Mode Selection

PFM or PWM light load operation is selected by the MODE pin. Pull the MODE pin low for PFM operation, and pull this pin high for PWM operation.

## Load Transient Considerations:

The SQV256 adopts the instant PWM architecture to achieve good stability and fast transient responses. In applications with high step load current, adding an RC network $R_{FF}$ and $C_{FF}$ parallel with $R_1$ may further speed up the load transient responses.




## Switching Frequency

The SQV256 uses constant-on-time (COT) control and there is no dedicated oscillator in the IC. When output voltage setting is low and input voltage is high, the switching on-time may be limited by the internal minimum on-time limit, and switching frequency will decrease. Table 1 shows the switching frequency vs. output voltage when $V_{IN}$=12V.

Table1: $f_{SW}$ vs. $V_{OUT}$

| $f_{SW}$(kHz) / $V_{OUT}$(V) | Min | Typ | Max |
|---|---|---|---|
| 5 | 510 | 600 | 690 |
| 3.3 | 510 | 600 | 690 |
| 2.5 | 510 | 600 | 690 |
| 1.8 | 510 | 600 | 690 |
| 1.5 | 503 | 592 | 681 |
| 1.2 | 452 | 565 | 678 |
| 1 | 428 | 535 | 642 |
| 0.9 | 408 | 510 | 612 |

## Layout Design:

The layout design of the SQV256 is relatively simple. For the best efficiency and minimum noise problem, the following components should be placed close to the IC: $C_{IN}$, $C_{VCC}$, L, $R_1$ and $R_2$.

1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) $C_{IN}$ must be close to the pins IN and GND. The loop area formed by $C_{IN}$ and GND must be minimized.

3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

4) The components $R_1$ and $R_2$, and the trace connected to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery. A 1MΩ pull-down resistor should be placed between the enable pin and the GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

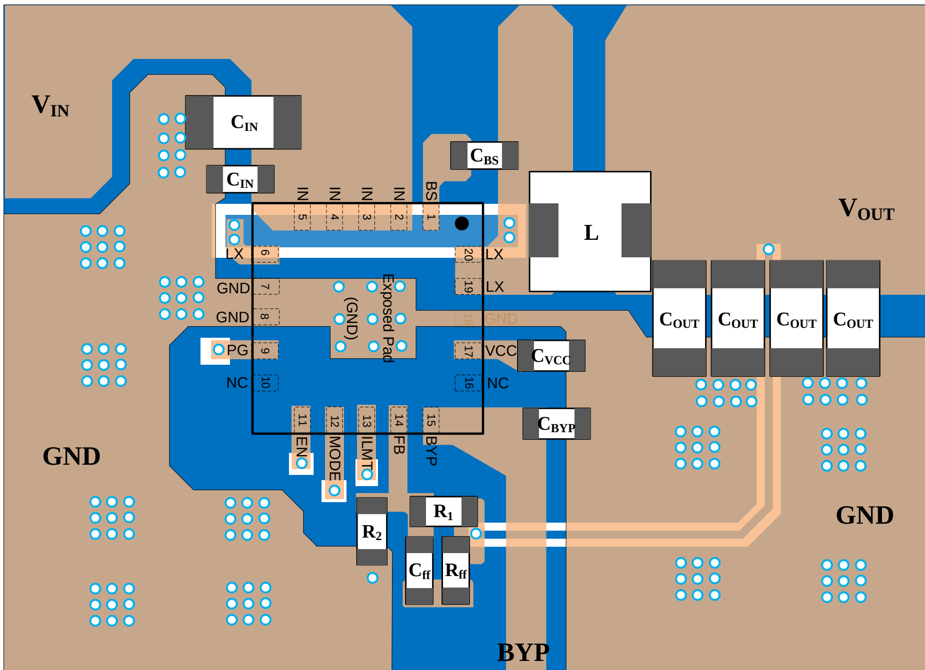
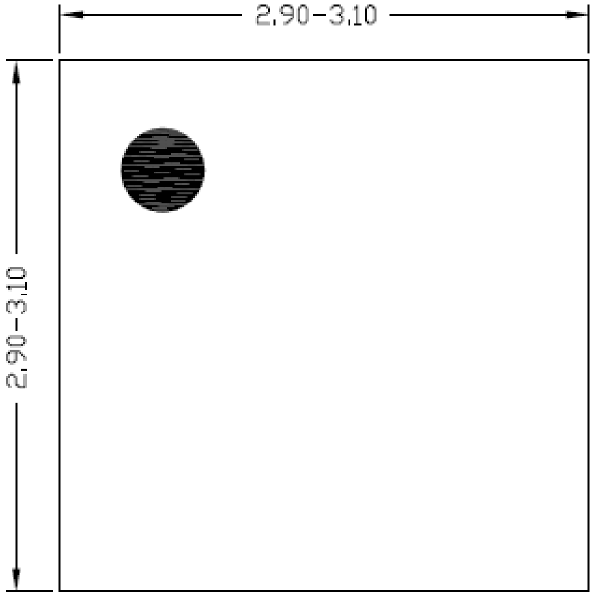
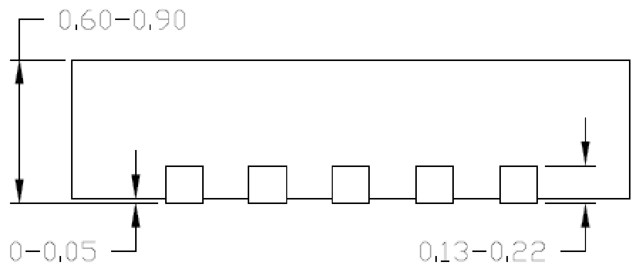



Figure4. PCB Layout Suggestion

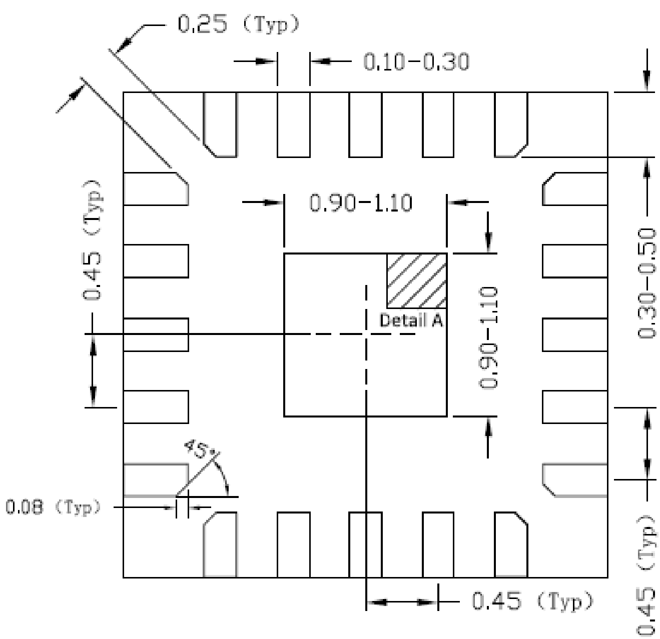
# QFN3×3-20 Package Outline



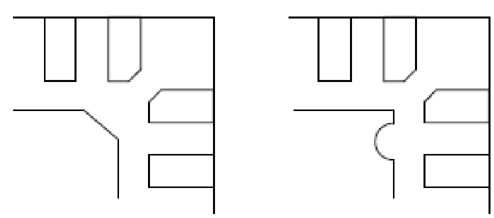

**Top view**



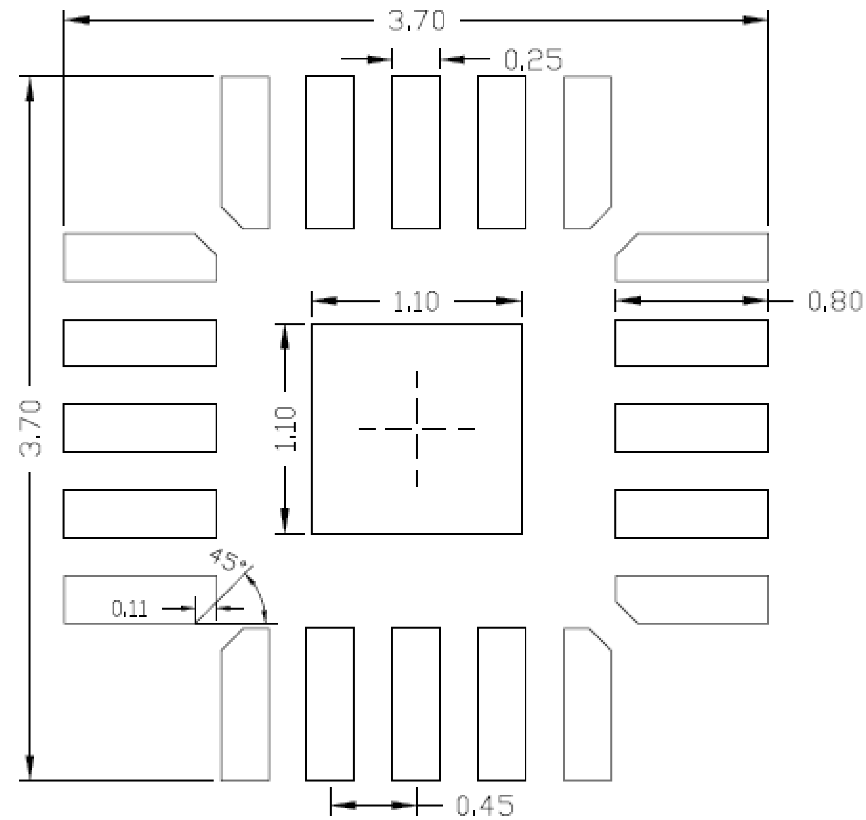

**Side view**




**Bottom view**



Detail A
Pin1 Identifier: two options

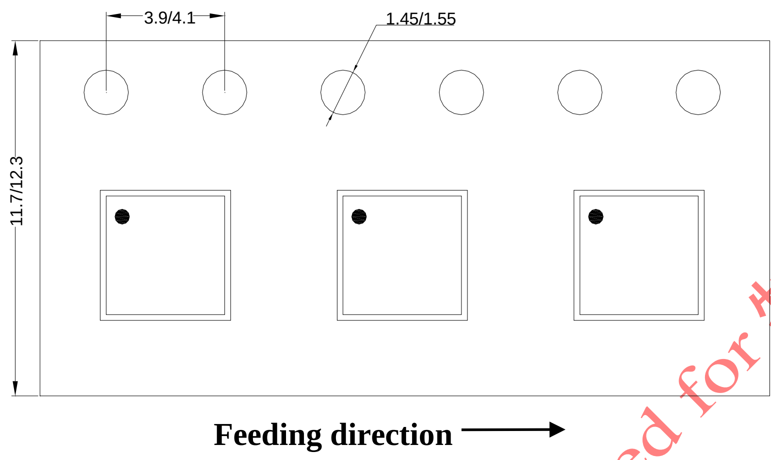



**Recommended PCB layout**
**(Reference only)**

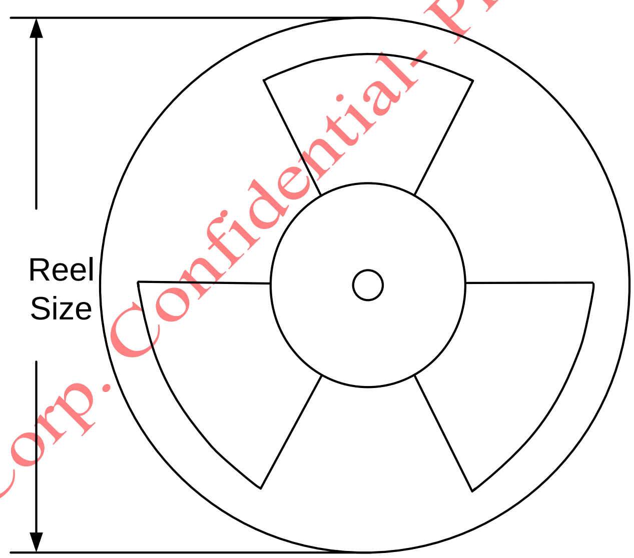
**Notes:** **All dimension in millimeter and exclude mold flash & metal burr.**

# Taping & Reel Specification

## 1. QFN3×3-20 taping orientation




## 2. Carrier Tape & Reel specification for packages




| Package type | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---|---|---|---|---|---|---|
| QFN3×3 | 12 | 8 | 13" | 400 | 400 | 5000 |

## 3. Others: NA

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