INA819 35 μV 失调电压、8 nV/√Hz 噪声、低功耗、精密仪表放大器

1 特性

- 低失调电压：10 μV（典型值），35 μV（最大值）
- 增益漂移：5 ppm/°C (G = 1)、35 ppm/°C (G > 1)（最大值）
- 噪声：8 nV/ √Hz
- 带宽：2 MHz (G = 1)、270 kHz (G = 100)
- 在 1 nF 容性负载下保持稳定
- 输入保护电压高达 ±60V
- 共模抑制：110 dB，G = 10（最小值）
- 电源抑制：110 dB，G = 1（最小值）
- 电源电流：385 μA（最大值）
- 电源电压范围：
  - 单电源：4.5V 至 36V
  - 双电源：±2.25V 至 ±18V
- 额定温度范围：–40°C 至 +125°C
- 封装：8 引脚 SOIC、VSSOP、WSON

2 应用

- 模拟输入模块
- 流量发送器
- 电池测试
- LCD 测试
- 心电图 (ECG)
- 外科手术设备
- 过程分析（pH、气体、浓度、力和湿度）

3 说明

INA819 是一款高精度仪表放大器，可提供低功耗并且可在极宽的单电源或双电源电压范围内工作。可通过单个外部电阻器在 1 到 10,000 范围内设置任意增益。由于采用超 β 输入晶体管（这些晶体管可提供极低的输入失调电压、失调电压漂移、输入偏置电流、输入电压和电流噪声），该器件可提供出色的精度。附加电路可以为输入提供高达 ±60V 的过压保护。

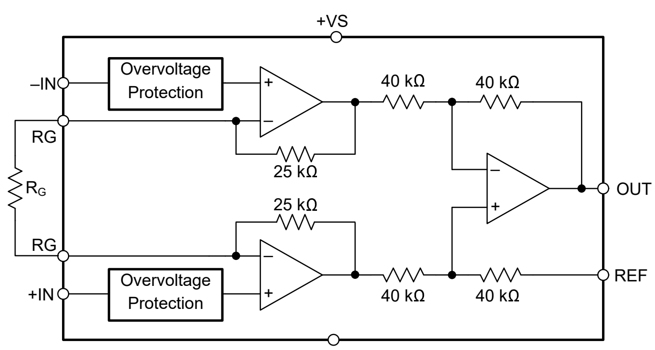
INA819 经过优化，可提供较高的共模抑制比。当 G = 1 时，整个输入共模范围内的共模抑制比超过 90 dB。根据设计，此器件在低电压下运行，由 4.5V 单电源和高达 ±18V 的双电源供电。

INA819 采用 8 引脚 SOIC、VSSOP 和 WSON 封装，并且额定工作温度范围为 –40°C 至 +125°C。

器件信息(1)

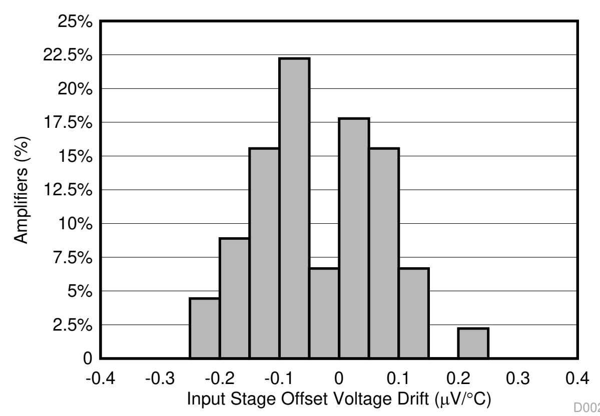
器件型号	封装	封装尺寸（标称值）
INA819	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)	3.00mm × 3.00mm
	WSON (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



$$G = 1 + \frac{50\text{ k}\Omega}{R_G} \qquad V_O = G(V_{+IN} - V_{-IN}) + V_{REF}$$

INA819 简化版内部原理图



输入阶段失调电压漂移的典型分布

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (June 2020) to Revision D (April 2022) — **Page**

- Changed input stage offset voltage specification for INA819DRG from 10 µV typical to 6 µV typical, and from 35 µV maximum to 30 µV maximum, in *Typical Characteristics* 6
- Changed maximum input stage offset voltage vs temperature specification for INA819DRG from 0.4 µV/°C to 0.35 µV/°C in *Typical Characteristics* 6
- Changed Figures 7-10 and 7-11 to correct units from nA to pA 8
- Changed input common-mode range calculator link from outdated Common-Mode Input Range Calculator for Instrumentation Amplifiers to Analog Engineers Calculator 22

Changes from Revision B (July 2019) to Revision C (June 2020) — **Page**

- 向数据表添加了 DRG (WSON) 封装和相关内容 1
- Added row for thermal pad to *Pin Functions* table 4
- Added bullet regarding exposed thermal pad to end of *Layout Guidelines* section 33

Changes from Revision A (May 2019) to Revision B (July 2019) — **Page**

- 将 DGK (VSSOP) 封装从预告信息（预发布）更改为量产数据（正在供货） 1

Changes from Revision * (December 2018) to Revision A (April 2019) — **Page**

- 向数据表添加了 8 引脚 DGK (VSSOP) 封装预告信息和相关内容 1
- 更改了*应用* 要点 1

5 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
INA819	35-µV Offset, 0.4-µV/°C V_{OS} Drift, 8-nV/$\sqrt{Hz}$ Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	2, 3
INA818	35-µV Offset, 0.4-µV/°C V_{OS} Drift, 8-nV/$\sqrt{Hz}$ Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	1, 8
INA821	35-µV Offset, 0.4-µV/°C V_{OS} Drift, 7-nV/$\sqrt{Hz}$ Noise, High-Bandwidth, Precision Instrumentation Amplifier	G = 1 + 49.4 kΩ / RG	2, 3
INA828	50-µV Offset, 0.5-µV/°C V_{OS} Drift, 7-nV/$\sqrt{Hz}$ Noise, Low-Power, Precision Instrumentation Amplifier	G = 1 + 50 kΩ / RG	1, 8
INA333	25-µV V_{OS}, 0.1-µV/°C V_{OS} Drift, 1.8-V to 5-V, RRO, 50-µA I_Q, Chopper-Stabilized INA	G = 1 + 100 kΩ / RG	1, 8
PGA280	20-mV to ±10-V Programmable Gain IA With 3-V or 5-V Differential Output; Analog Supply up to ±18 V	Digital programmable	N/A
INA159	G = 0.2 V Differential Amplifier for ±10-V to 3-V and 5-V Conversion	G = 0.2 V/V	N/A
PGA112	Precision Programmable Gain Op Amp With SPI	Digital programmable	N/A

6 Pin Configuration and Functions

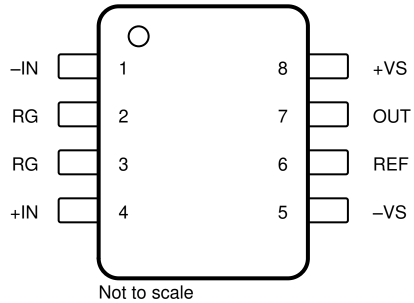


图 6-1. D (8-Pin SOIC) and DGK (8-Pin VSSOP) Packages, Top View

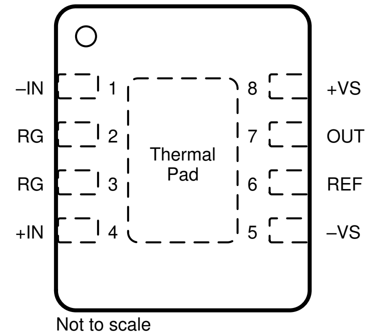


图 6-2. DRG Package, 8-Pin WSON, Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
– IN	1	Input	Negative (inverting) input
+IN	4	Input	Positive (noninverting) input
OUT	7	Output	Output
RG	2, 3	—	Gain setting pin. Place a gain resistor between pin 2 and pin 3.
REF	6	Input	Reference input. This pin must be driven by a low impedance source.
– VS	5	—	Negative supply
+VS	8	—	Positive supply
Thermal pad	—	—	Thermal pad internally connected to – VS. Connect externally to – VS or leave floating.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
Supply voltage dual supply, V_S = (V+) – (V –)		±20	V
Supply voltage single supply, V_S = (V+) – (V –)		40	V
Signal input pins	–60	60	V
VREF pin	–20	20	V
Signal output pins maximum voltage	(– V_s) – 0.5	(+V_s) + 0.5	V
Signal output pins maximum current	–50	50	mA
Output short-circuit[(2)]	Continuous		
Operating Temperature, T_A	–50	150	°C
Junction Temperature, T_J		175	°C
Storage Temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_S	Single-supply	4.5	36	V
	Dual-supply	±2.25	±18	
Specified temperature, T_A	Specified temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC[(1)]		INA819 D (SOIC) 8 PINS	INA819 DGK (VSSOP) 8 PINS	INA819 DRG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.6	215.4	55.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.3	66.3	57.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.9	97.8	28.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.5	10.5	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.4	96.1	28.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	12.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OSI}	Input stage offset voltage[1] [3]		INA819ID		10	35	µV
			INA819IDGK			40	µV
			INA819IDRG		6	30	µV
		T_A = –40°C to +125°C[2]	INA819ID, INA819DRG			75	µV
			INA819IDGK			80	µV
		vs temperature, T_A = –40°C to +125°C	INA819D, INA819DGK			0.4	µV/°C
			INA819DRG			0.35	µV/°C
V_{OSO}	Output stage offset voltage[1] [3]				50	300	µV
		T_A = –40°C to +125°C[2]				800	µV
		vs temperature, T_A = –40°C to +125°C				5	µV/°C
PSRR	Power-supply rejection ratio	G = 1, RTI		110	120		dB
		G = 10, RTI		114	130		dB
		G = 100, RTI		130	135		dB
		G = 1000, RTI		136	140		dB
z_{id}	Differential impedance				100 || 1		GΩ || pF
z_{ic}	Common-mode impedance				100 || 4		GΩ || pF
	RFI filter, –3-dB frequency				32		MHz
V_{CM}	Operating input range[4]			(V–) + 2		(V+) – 2	V
		V_S = ±2.25 V to ±18 V, T_A = –40°C to +125°C		See 图 7-51 through 图 7-54			V
	Input overvoltage range	T_A = –40°C to +125°C[2]				±60	V
CMRR	Common-mode rejection ratio	At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 1		90	105		dB
		At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 10		110	125		dB
		At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 100		130	145		dB
		At DC to 60 Hz, RTI, V_{CM} = (V–) + 2 V to (V+) – 2 V, G = 1000		140	150		dB
BIAS CURRENT							
I_B	Input bias current	V_{CM} = V_S / 2			0.15	0.5	nA
		T_A = –40°C to +125°C				2	nA
I_{OS}	Input offset current	V_{CM} = V_S / 2			0.15	0.5	nA
		T_A = –40°C to +125°C				2	nA
NOISE VOLTAGE							
e_{NI}	Input stage voltage noise[6]	f = 1 kHz, G = 100, R_S = 0 Ω			8		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100, R_S = 0 Ω			0.19		$µV_{PP}$
e_{NO}	Output stage voltage noise[6]	f = 1 kHz, R_S = 0 Ω			80		nV/√Hz
		f_B = 0.1 Hz to 10 Hz, R_S = 0 Ω			2.6		$µV_{PP}$
I_n	Noise current	f = 1 kHz			130		fA/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100			4.7		pA_{PP}

7.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GAIN						
	Gain equation			1 + (50 kΩ / R_G)		V/V
G	Gain		1		10000	V/V
GE	Gain error	G = 1, V_O = ±10 V		±0.005%	±0.025%	
		G = 10, V_O = ±10 V		±0.025%	±0.15%	
		G = 100, V_O = ±10 V		±0.025%	±0.15%	
		G = 1000, V_O = ±10 V		±0.05%		
	Gain vs temperature(5)	G = 1, T_A = –40°C to +125°C			±5	ppm/°C
		G > 1, T_A = –40°C to +125°C			±35	ppm/°C
	Gain nonlinearity	G = 1 to 10, V_O = –10 V to +10 V, R_L = 10 kΩ		1	10	ppm
		G = 100, V_O = –10 V to +10 V, R_L = 10 kΩ			15	ppm
		G = 1000, V_O = –10 V to +10 V, R_L = 10 kΩ		10		ppm
		G = 1 to 100, V_O = –10 V to +10 V, R_L = 2 kΩ		30		ppm
OUTPUT						
	Voltage swing		(V–) + 0.15		(V+) – 0.15	V
	Load capacitance stability			1000		pF
Z_O	Closed-loop output impedance	f = 10 kHz		5.0		Ω
I_{SC}	Short-circuit current	Continuous to V_S / 2		±20		mA
FREQUENCY RESPONSE						
BW	Bandwidth, –3 dB	G = 1		2.0		MHz
		G = 10		890		kHz
		G = 100		270		kHz
		G = 1000		30		kHz
SR	Slew rate	G = 1, V_O = ±10 V		0.9		V/µs
t_S	Settling time	0.01%, G = 1 to 100, V_{STEP} = 10 V		12		µs
		0.01%, G = 1000, V_{STEP} = 10 V		40		µs
		0.001%, G = 1 to 100, V_{STEP} = 10 V		16		µs
		0.001%, G = 1000, V_{STEP} = 10 V		60		µs
REFERENCE INPUT						
R_{IN}	Input impedance			40		kΩ
	Voltage range		(V–)		(V+)	V
	Gain to output			1		V/V
	Reference gain error			0.01%		
POWER SUPPLY						
I_Q	Quiescent current	V_{IN} = 0 V		350	385	µA
		vs temperature, T_A = –40°C to +125°C			520	µA

(1) Total offset, referred-to-input (RTI): $V_{OS} = (V_{OSI}) + (V_{OSO} / G)$.
(2) Specified by characterization.
(3) Offset drifts are uncorrelated. Input-referred offset drift is calculated using: $\Delta V_{OS(RTI)} = \sqrt{[\Delta V_{OSI}^2 + (\Delta V_{OSO} / G)^2]}$.
(4) Input voltage range of the Instrumentation Amplifier input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage.
(5) The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.
(6) Total RTI voltage noise is equal to: $e_{N(RTI)} = \sqrt{[e_{NI}^2 + (e_{NO} / G)^2]}$.

7.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

表 7-1. Table of Graphs

DESCRIPTION	FIGURE
Typical Distribution of Input Stage Offset Voltage	图 7-1
Typical Distribution of Input Stage Offset Voltage Drift	图 7-2
Typical Distribution of Output Stage Offset Voltage	图 7-3
Typical Distribution of Output Stage Offset Voltage Drift	图 7-4
Input Stage Offset Voltage vs Temperature	图 7-5
Output Stage Offset Voltage vs Temperature	图 7-6
Typical Distribution of Input Bias Current, T_A = 25°C	图 7-7
Typical Distribution of Input Bias Current, T_A = 90°C	图 7-8
Typical Distribution of Input Offset Current	图 7-9
Input Bias Current vs Temperature	图 7-10
Input Offset Current vs Temperature	图 7-11
Typical CMRR Distribution, G = 1	图 7-12
Typical CMRR Distribution, G = 10	图 7-13
CMRR vs Temperature, G = 1	图 7-14
CMRR vs Temperature, G = 10	图 7-15
Input Current vs Input Overvoltage	图 7-16
CMRR vs Frequency (RTI)	图 7-17
CMRR vs Frequency (RTI, 1-kΩ source imbalance)	图 7-18
Positive PSRR vs Frequency (RTI)	图 7-19
Negative PSRR vs Frequency (RTI)	图 7-20
Gain vs Frequency	图 7-21
Voltage Noise Spectral Density vs Frequency (RTI)	图 7-22
Current Noise Spectral Density vs Frequency (RTI)	图 7-23
0.1-Hz to 10-Hz RTI Voltage Noise, G = 1	图 7-24
0.1-Hz to 10-Hz RTI Voltage Noise, G = 1000	图 7-25
0.1-Hz to 10-Hz RTI Current Noise	图 7-26
Input Bias Current vs Common-Mode Voltage	图 7-27
Typical Distribution of Gain Error, G = 1	图 7-28
Typical Distribution of Gain Error, G = 10	图 7-29
Gain Error vs Temperature, G = 1	图 7-30
Gain Error vs Temperature, G = 10	图 7-31
Supply Current vs Temperature	图 7-32
Gain Nonlinearity, G = 1	图 7-33
Gain Nonlinearity, G = 10	图 7-34
Offset Voltage vs Negative Common-Mode Voltage	图 7-35
Offset Voltage vs Positive Common-Mode Voltage	图 7-36
Positive Output Voltage Swing vs Output Current	图 7-37
Negative Output Voltage Swing vs Output Current	图 7-38
Short Circuit Current vs Temperature	图 7-39
Large-Signal Frequency Response	图 7-40

7.6 Typical Characteristics

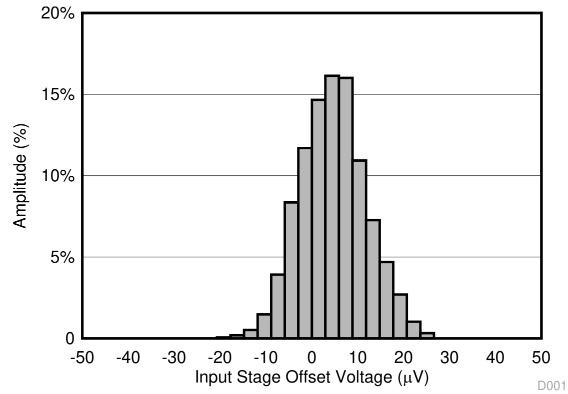
at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

表 7-1. Table of Graphs (continued)

DESCRIPTION	FIGURE
THD+N vs Frequency	图 7-41
Overshoot vs Capacitive Loads	图 7-42
Small-Signal Response, G = 1	图 7-43
Small-Signal Response, G = 10	图 7-44
Small-Signal Response, G = 100	图 7-45
Small-Signal Response, G = 1000	图 7-46
Large Signal Step Response	图 7-47
Closed-Loop Output Impedance	图 7-48
Differential-Mode EMI Rejection Ratio	图 7-49
Common-Mode EMI Rejection Ratio	图 7-50
Input Common-Mode Voltage vs Output Voltage, G = 1, V_S = 5 V	图 7-51
Input Common-Mode Voltage vs Output Voltage, G = 100, V_S = 5 V	图 7-52
Input Common-Mode Voltage vs Output Voltage, V_S =±5 V	图 7-53
Input Common-Mode Voltage vs Output Voltage, V_S =±15 V	图 7-54

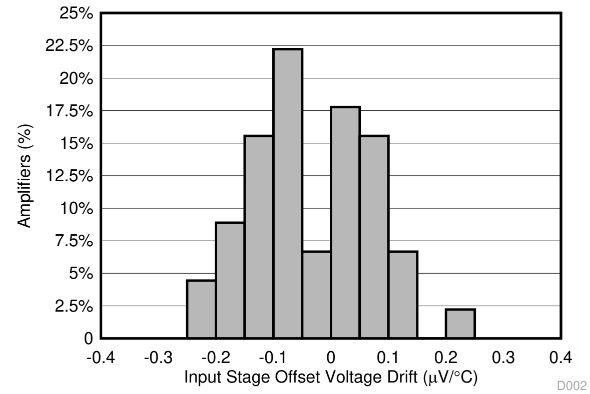
7.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



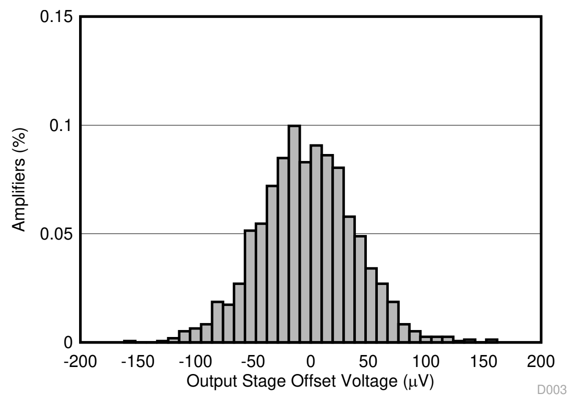
N = 1555 Mean = 4.71 µV Std. Dev. = 7.12 µV

图 7-1. Typical Distribution of Input Stage Offset Voltage



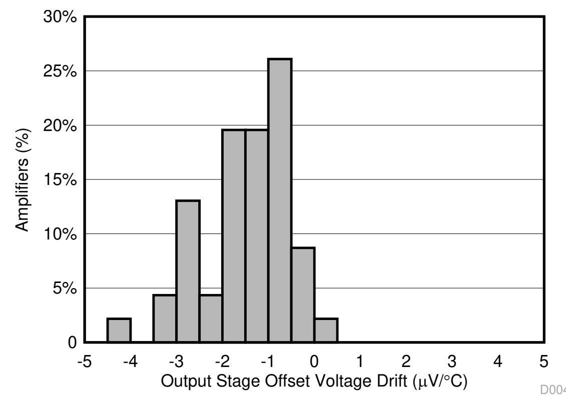
N = 45 Mean = 0.0357 µV/°C Std. Dev. = 0.099 µV/°C

图 7-2. Typical Distribution of Input Stage Offset Voltage Drift



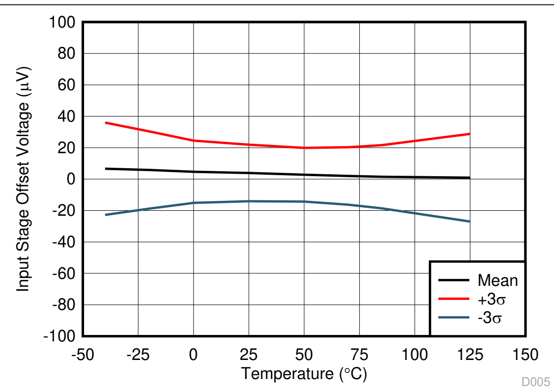
N = 1555 Mean = –3.18 µV Std. Dev. = 41.26 µV

图 7-3. Typical Distribution of Output Stage Offset Voltage



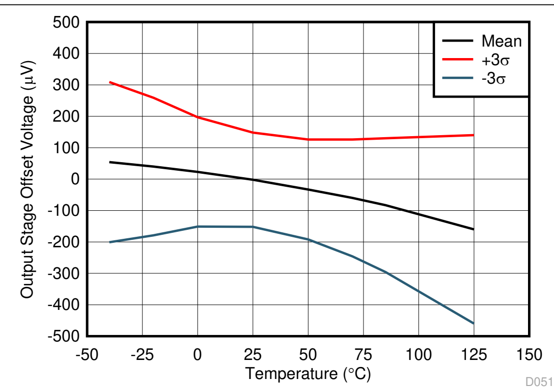
N = 45 Mean = –1.49 µV/°C Std. Dev. = 0.89 µV/°C

图 7-4. Typical Distribution of Output Stage Offset Voltage Drift



45 units, 1 wafer lot

图 7-5. Input Stage Offset Voltage vs Temperature

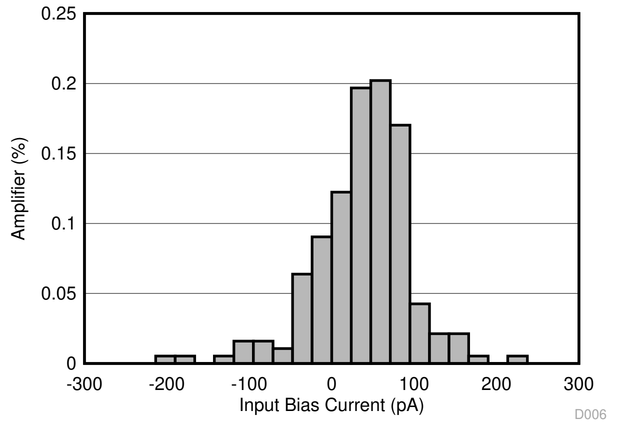


45 units, 1 wafer lots

图 7-6. Output Stage Offset Voltage vs Temperature

7.6 Typical Characteristics (continued)

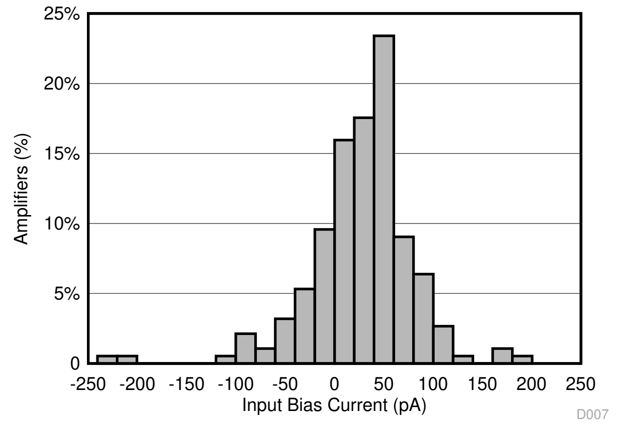
at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



N = 94 Mean = 37.13 pA Std. Dev. = 57.65 pA

T_A = 25°C

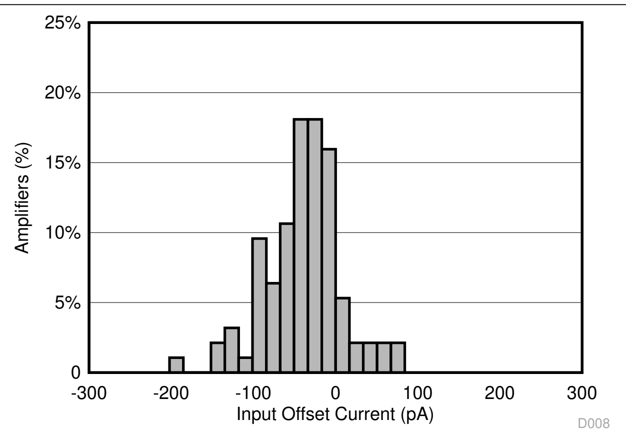
图 7-7. Typical Distribution of Input Bias Current



N = 94 Mean = – 27.65 pA Std. Dev. = 52.58 pA

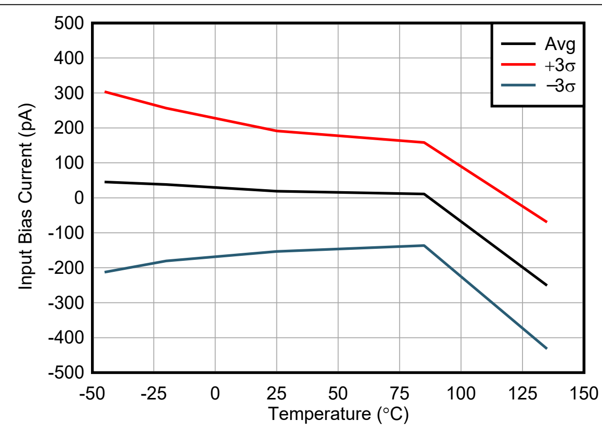
T_A = 90°C

图 7-8. Typical Distribution of Input Bias Current



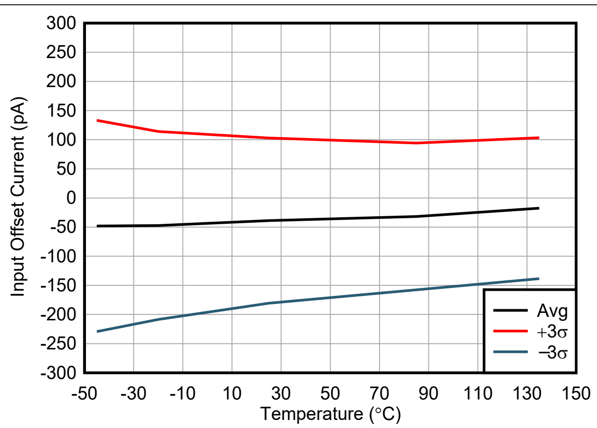
N = 94 Mean = – 38.82 pA Std. Dev. = 47.24 pA

图 7-9. Typical Distribution of Input Offset Current



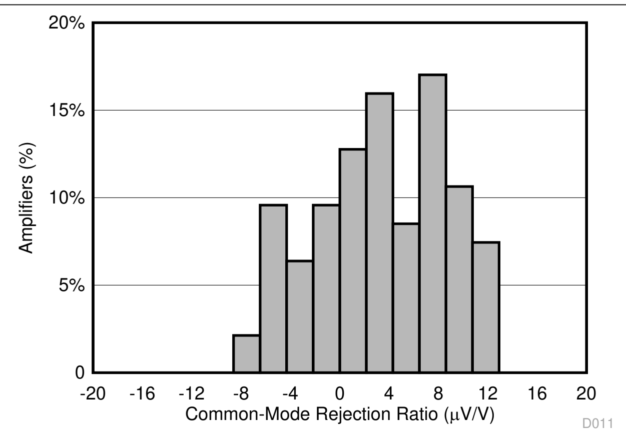
N = 94 G = 1

图 7-10. Input Bias Current vs Temperature



N = 94 G = 1

图 7-11. Input Offset Current vs Temperature



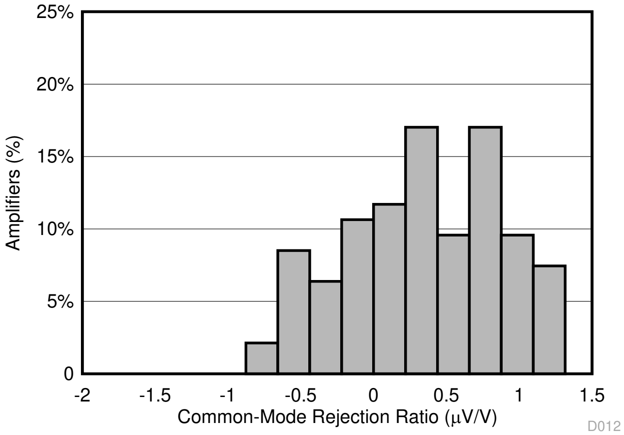
N = 94 Mean = 3.23 μV/V Std. Dev. = 5.38 μV/V

G = 1

图 7-12. Typical CMRR Distribution

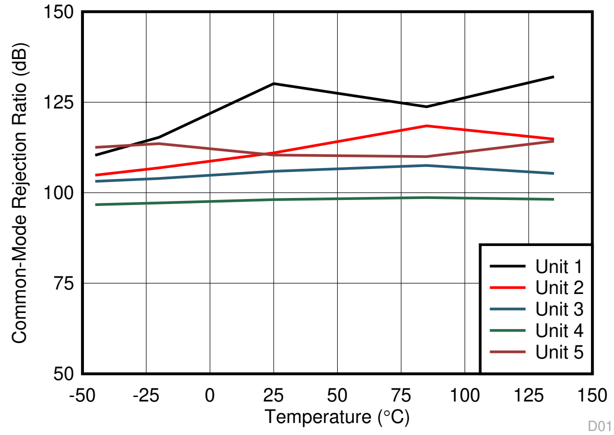
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



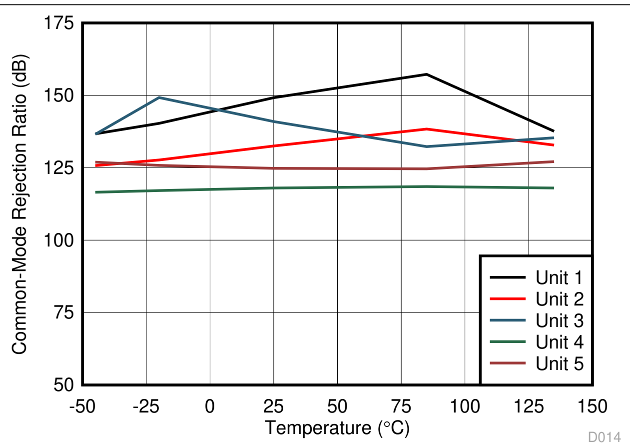
N = 94 Mean = 0.34 µV/V Std. Dev. = 0.54 µV/V
G = 10

图 7-13. Typical CMRR Distribution



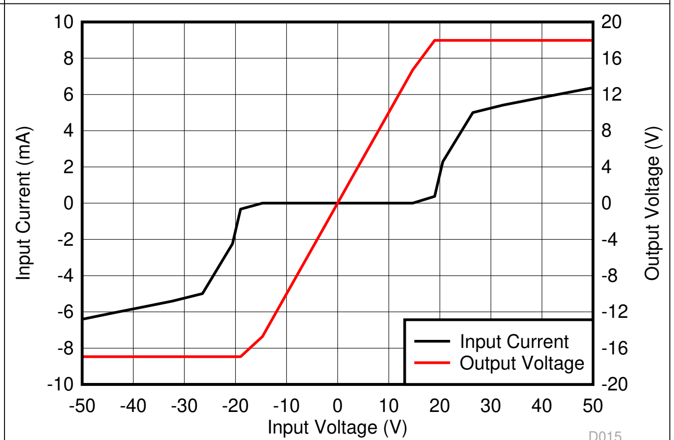
5 typical units G = 1

图 7-14. CMRR vs Temperature



5 typical units G = 10

图 7-15. CMRR vs Temperature



V_S = 36 V

图 7-16. Input Current vs Input Overvoltage

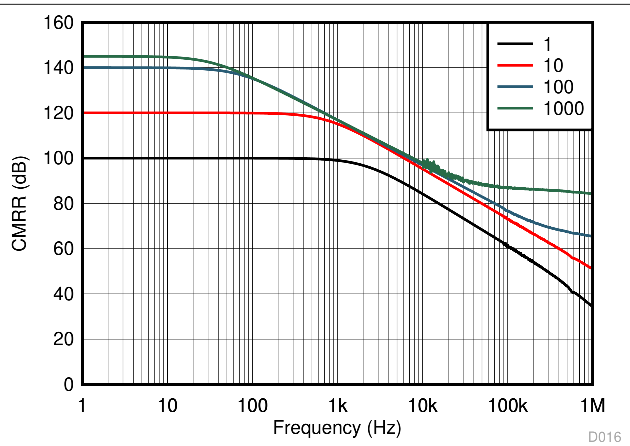
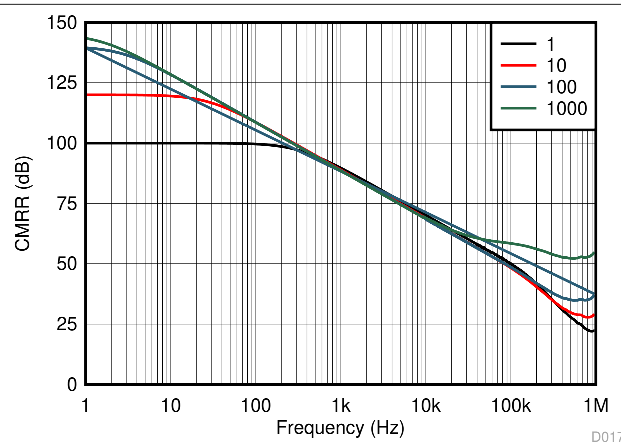


图 7-17. CMRR vs Frequency (RTI)



1-kΩ source imbalance

图 7-18. CMRR vs Frequency (RTI)

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

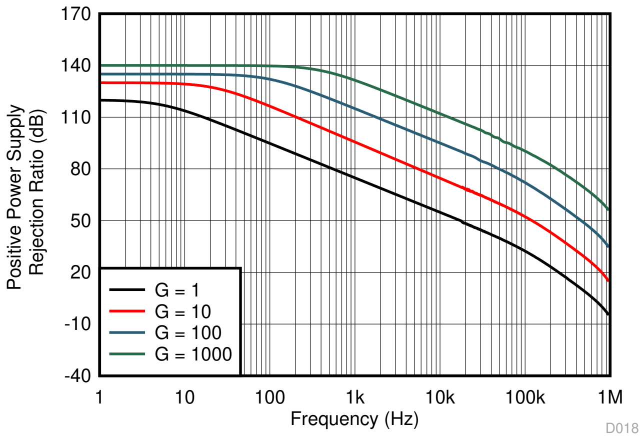


图 7-19. Positive PSRR vs Frequency (RTI)

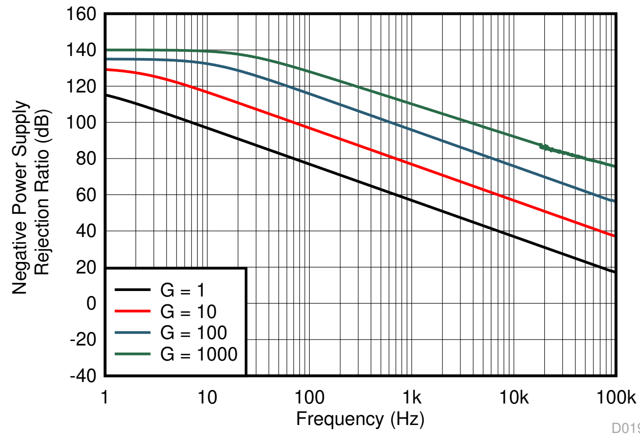


图 7-20. Negative PSRR vs Frequency (RTI)

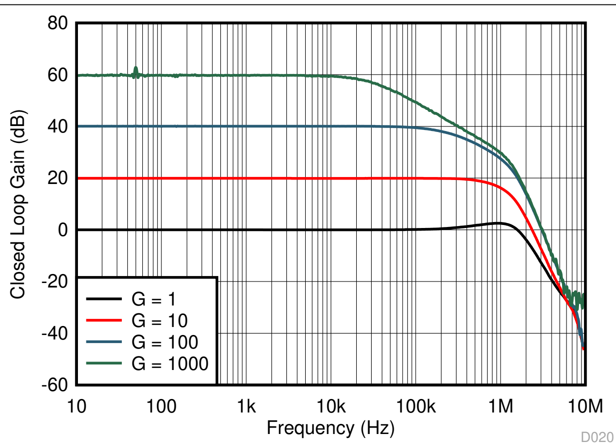


图 7-21. Gain vs Frequency

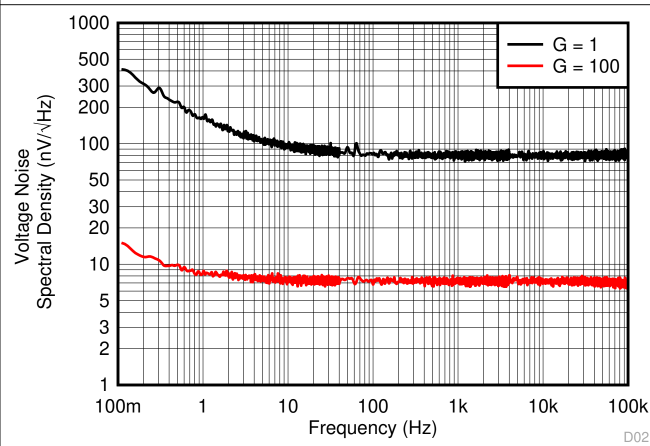


图 7-22. Voltage Noise Spectral Density vs Frequency (RTI)

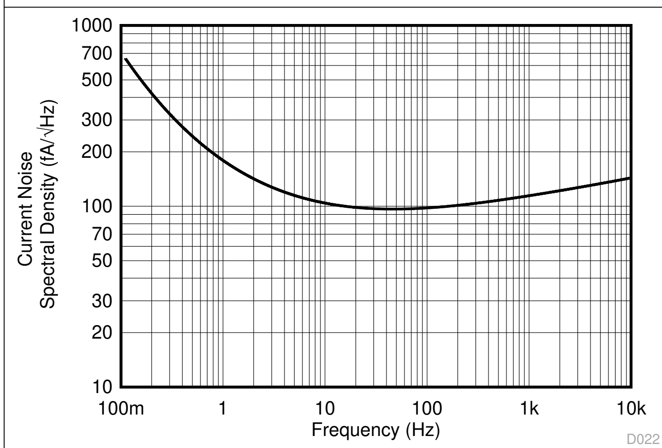
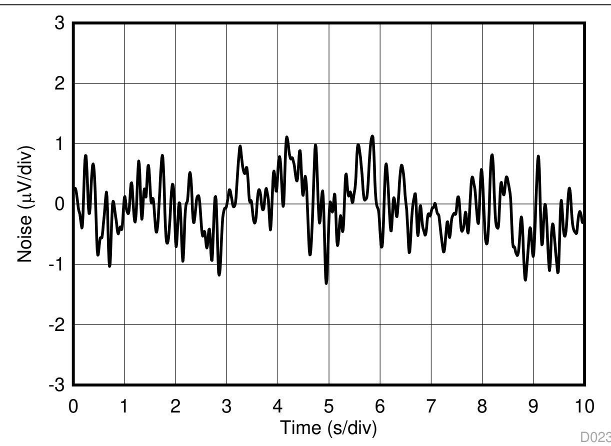


图 7-23. Current Noise Spectral Density vs Frequency (RTI)

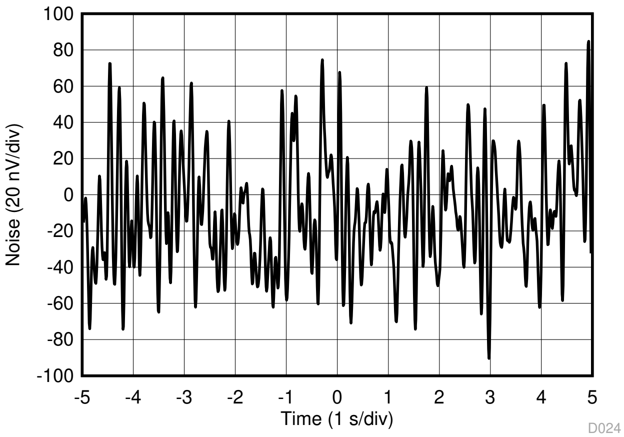


G = 1

图 7-24. 0.1-Hz to 10-Hz RTI Voltage Noise

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



G = 1000

图 7-25. 0.1-Hz to 10-Hz RTI Voltage Noise

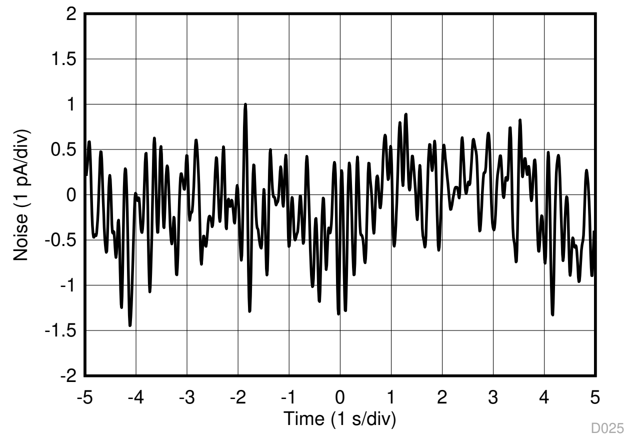
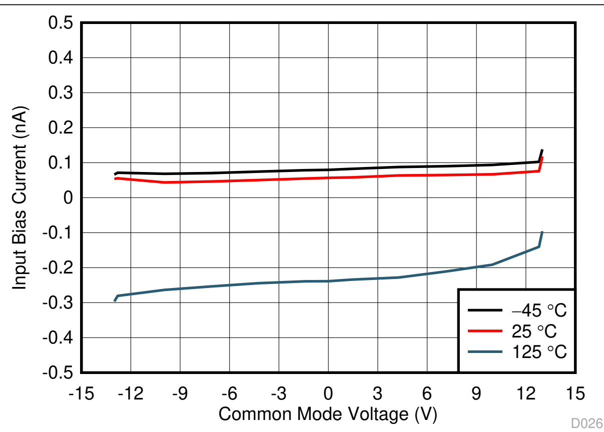
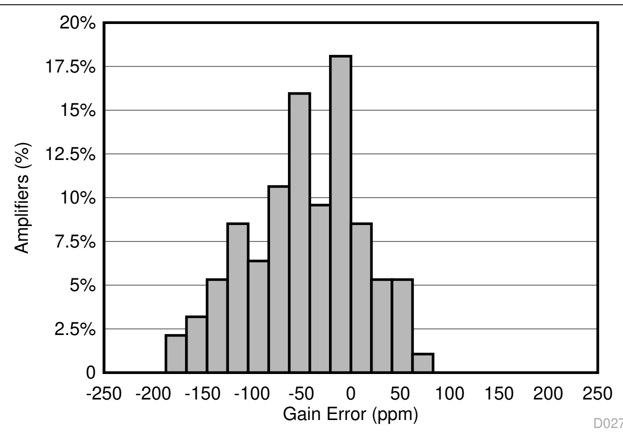


图 7-26. 0.1-Hz to 10-Hz RTI Current Noise



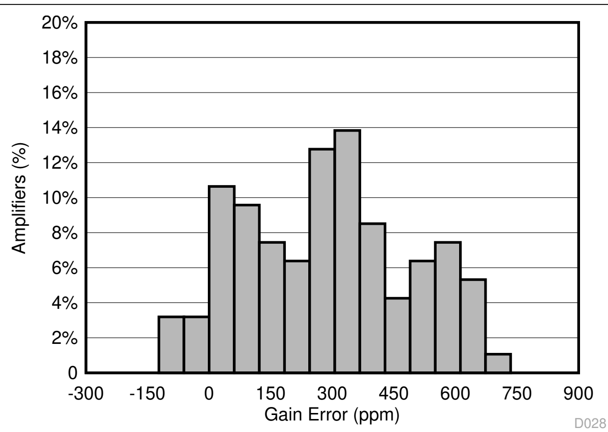
V_S = ±15 V

图 7-27. Input Bias Current vs Common-Mode Voltage



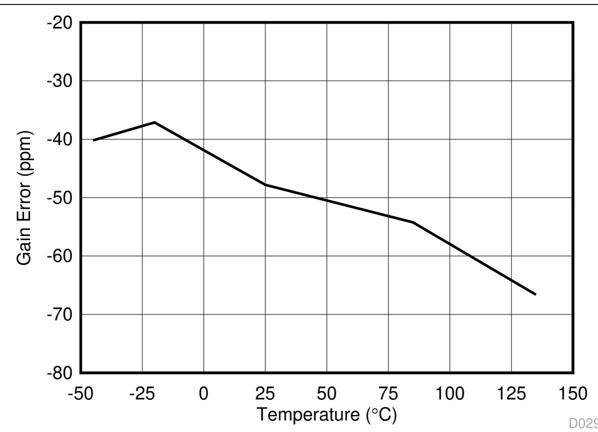
N = 94 Mean = –48 ppm Std. Dev. = 58 ppm
G = 1

图 7-28. Typical Distribution of Gain Error, G = 1



N = 94 Mean = 286 ppm Std. Dev. = 204 ppm
G = 10

图 7-29. Typical Distribution of Gain Error, G = 10

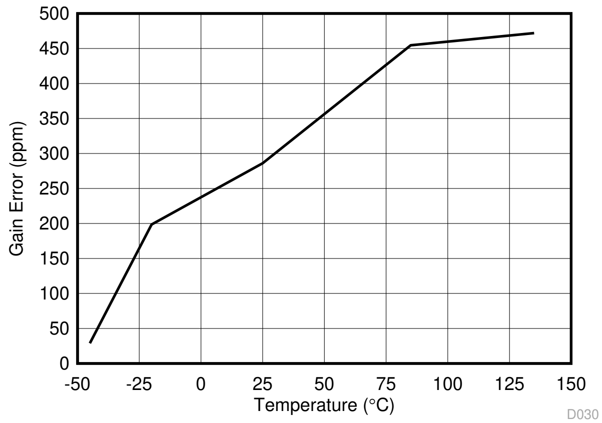


G = 1

图 7-30. Gain Error vs Temperature

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



G = 10

图 7-31. Gain Error vs Temperature

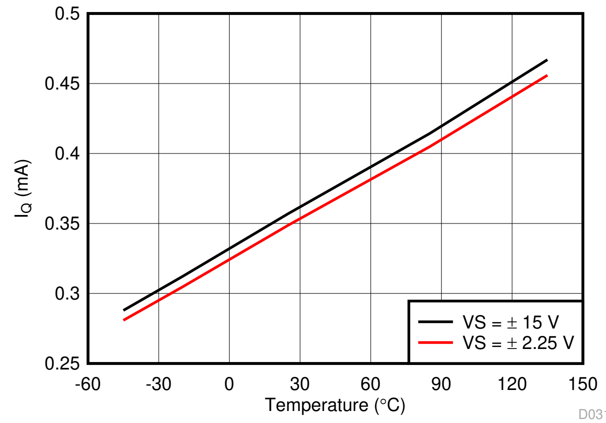
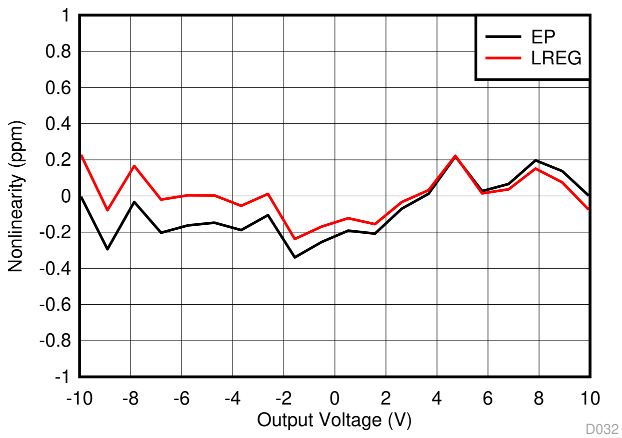
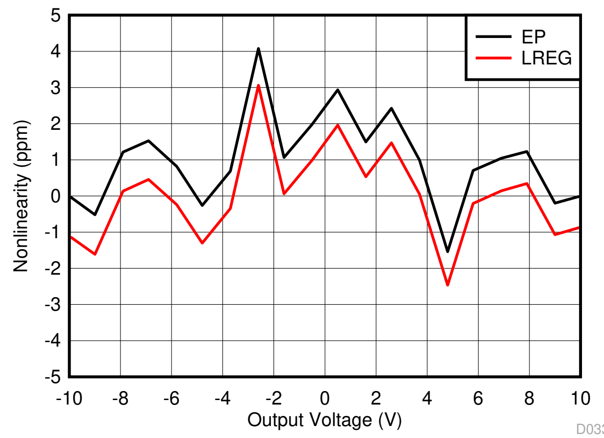


图 7-32. Supply Current vs Temperature



G = 1

图 7-33. Gain Nonlinearity



G = 10

图 7-34. Gain Nonlinearity

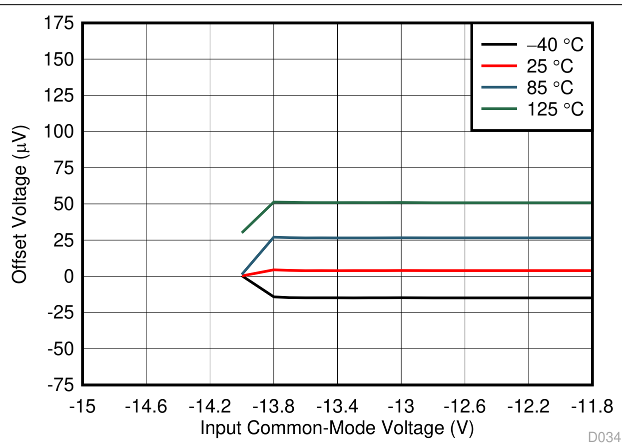


图 7-35. Offset Voltage vs Negative Common-Mode Voltage

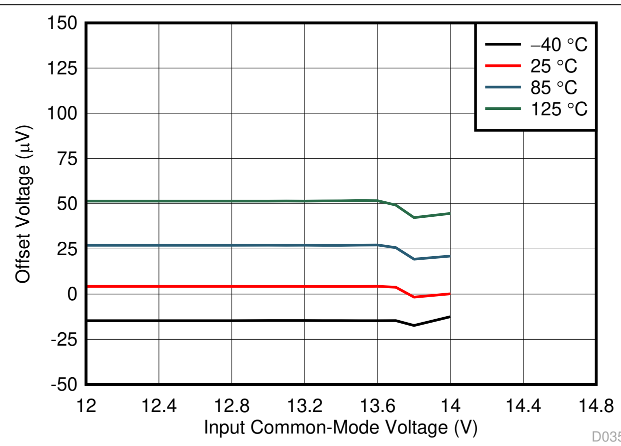


图 7-36. Offset Voltage vs Positive Common-Mode Voltage

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

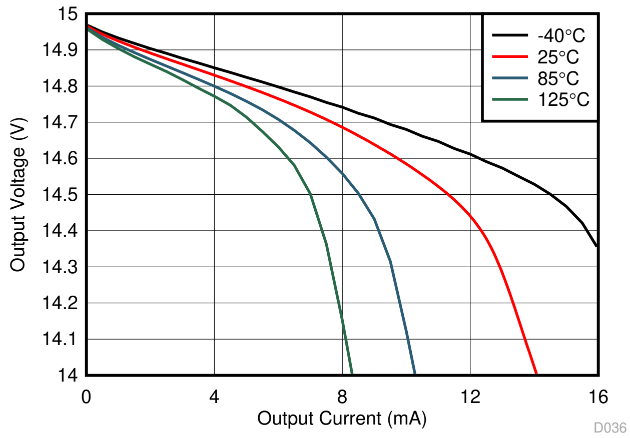


图 7-37. Positive Output Voltage Swing vs Output Current

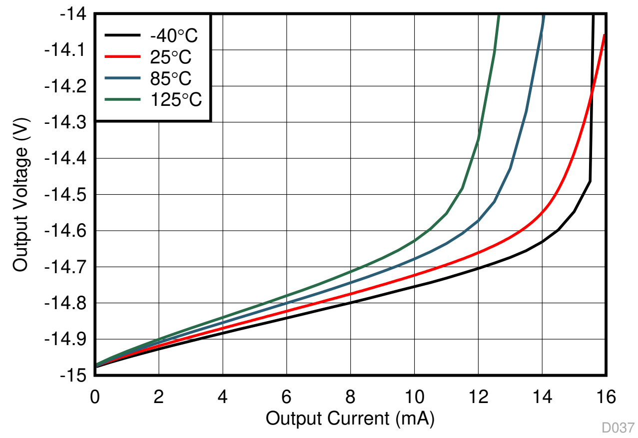


图 7-38. Negative Output Voltage Swing vs Output Current

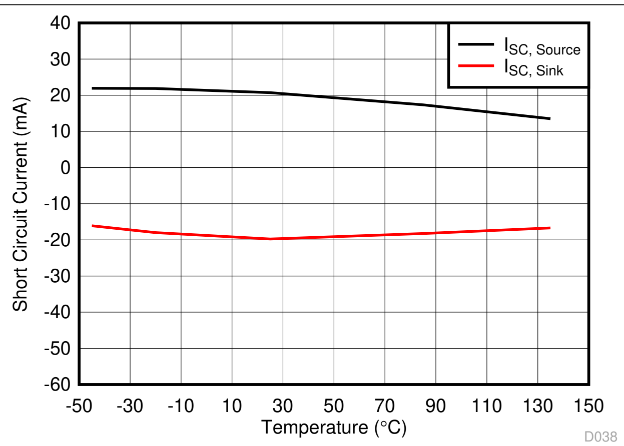


图 7-39. Short Circuit Current vs Temperature

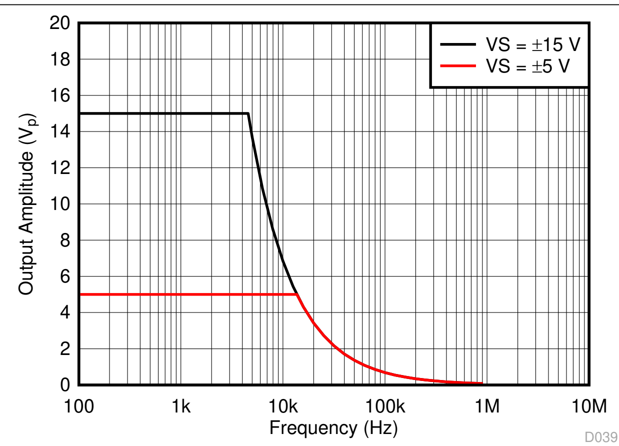
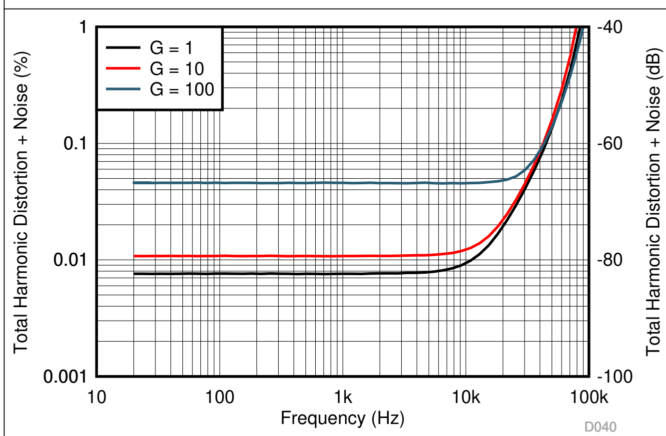


图 7-40. Large-Signal Frequency Response



500-kHz measurement bandwidth

1-V_{RMS} output voltage 100-kΩ load

图 7-41. THD+N vs Frequency

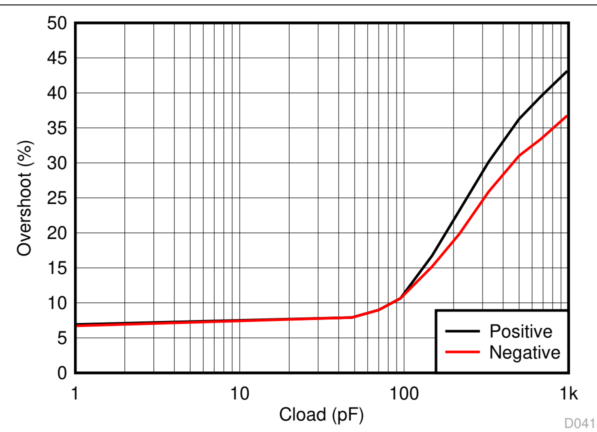
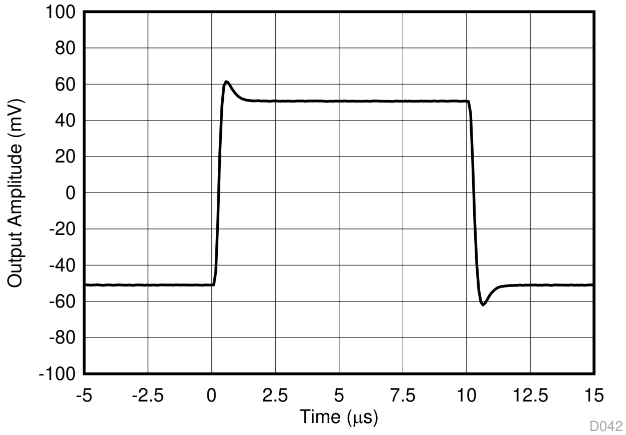


图 7-42. Overshoot vs Capacitive Loads

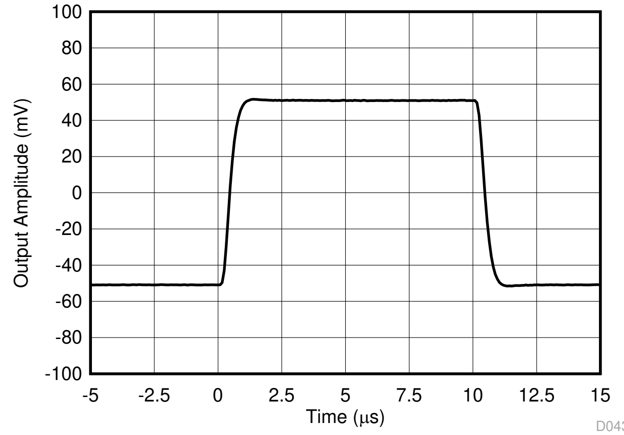
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



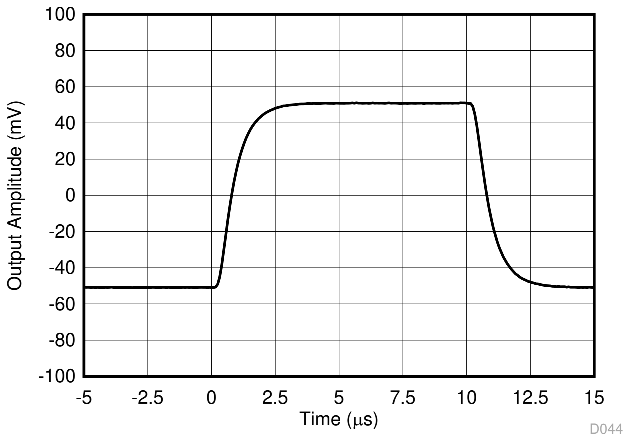
G = 1 R_L = 10 kΩ C_L = 100 pF

图 7-43. Small-Signal Response



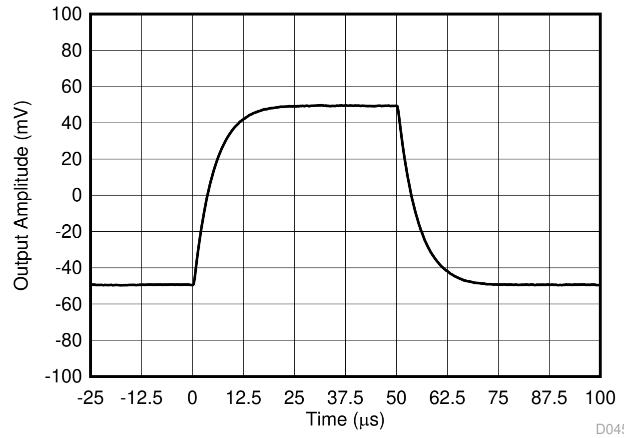
G = 10 R_L = 10 kΩ C_L = 100 pF

图 7-44. Small-Signal Response



G = 100 R_L = 10 kΩ C_L = 100 pF

图 7-45. Small-Signal Response



G = 1000 R_L = 10 kΩ C_L = 100 pF

图 7-46. Small-Signal Response

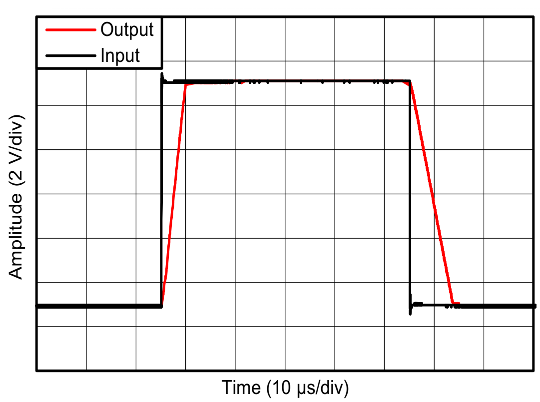


图 7-47. Large Signal Step Response

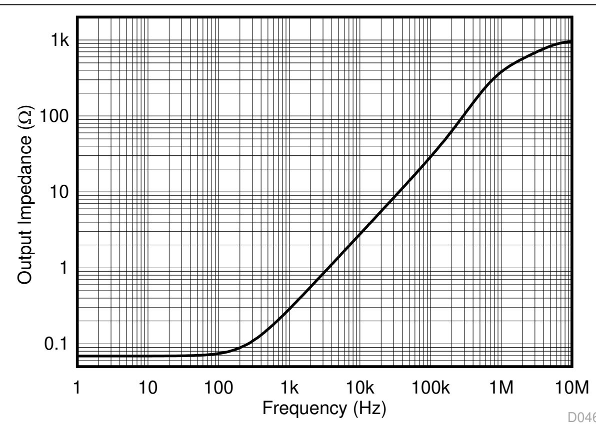


图 7-48. Closed-Loop Output Impedance

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

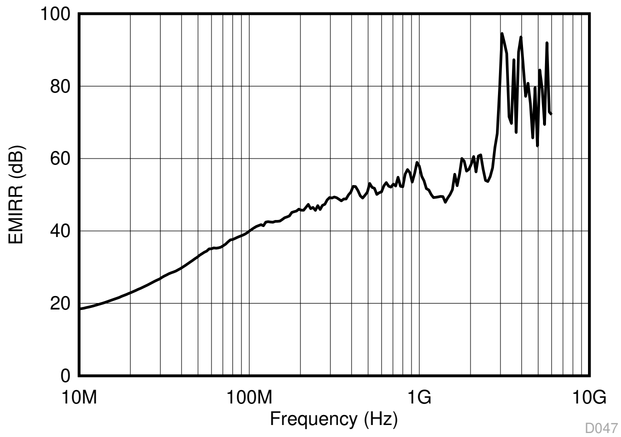


图 7-49. Differential-Mode EMI Rejection Ratio

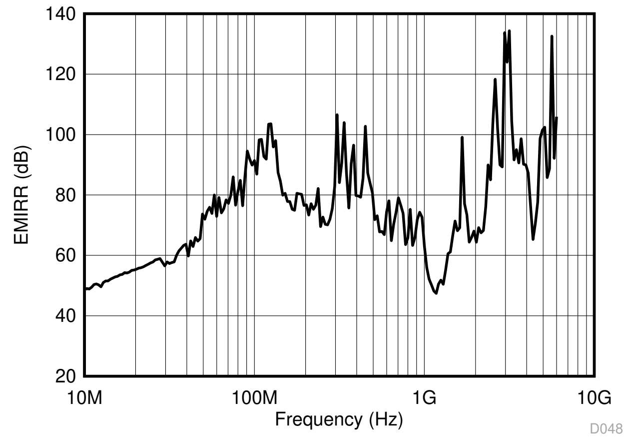
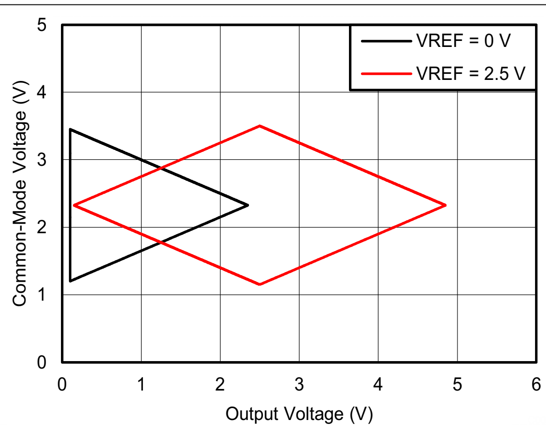
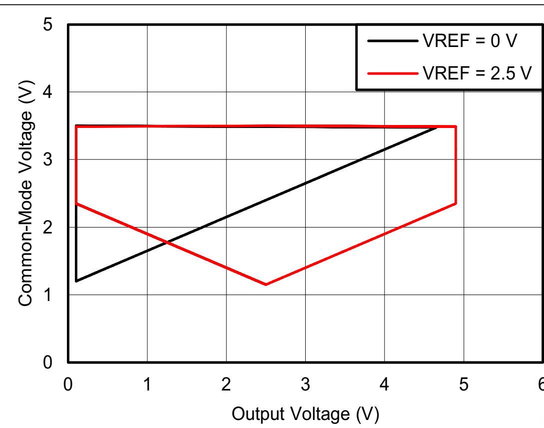


图 7-50. Common-Mode EMI Rejection Ratio



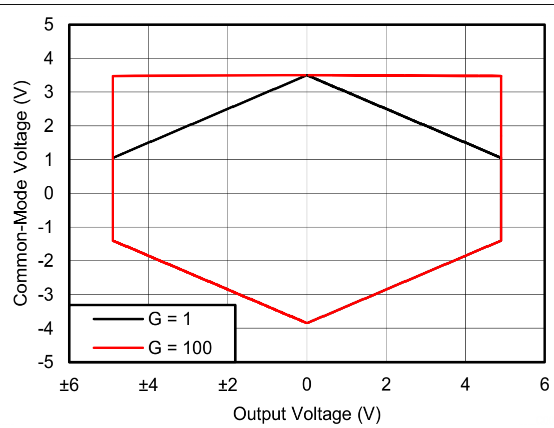
V_S = 5 V G = 1

图 7-51. Input Common-Mode Voltage vs Output Voltage



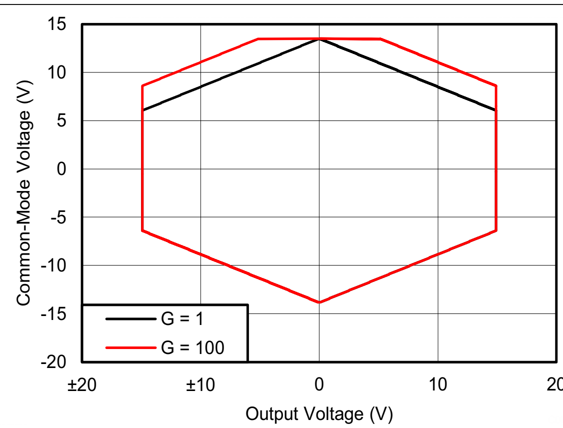
V_S = 5 V G = 100

图 7-52. Input Common-Mode Voltage vs Output Voltage



V_S = ±5 V V_{REF} = 0 V

图 7-53. Input Common-Mode Voltage vs Output Voltage



V_S = ±15 V V_{REF} = 0 V

图 7-54. Input Common-Mode Voltage vs Output Voltage

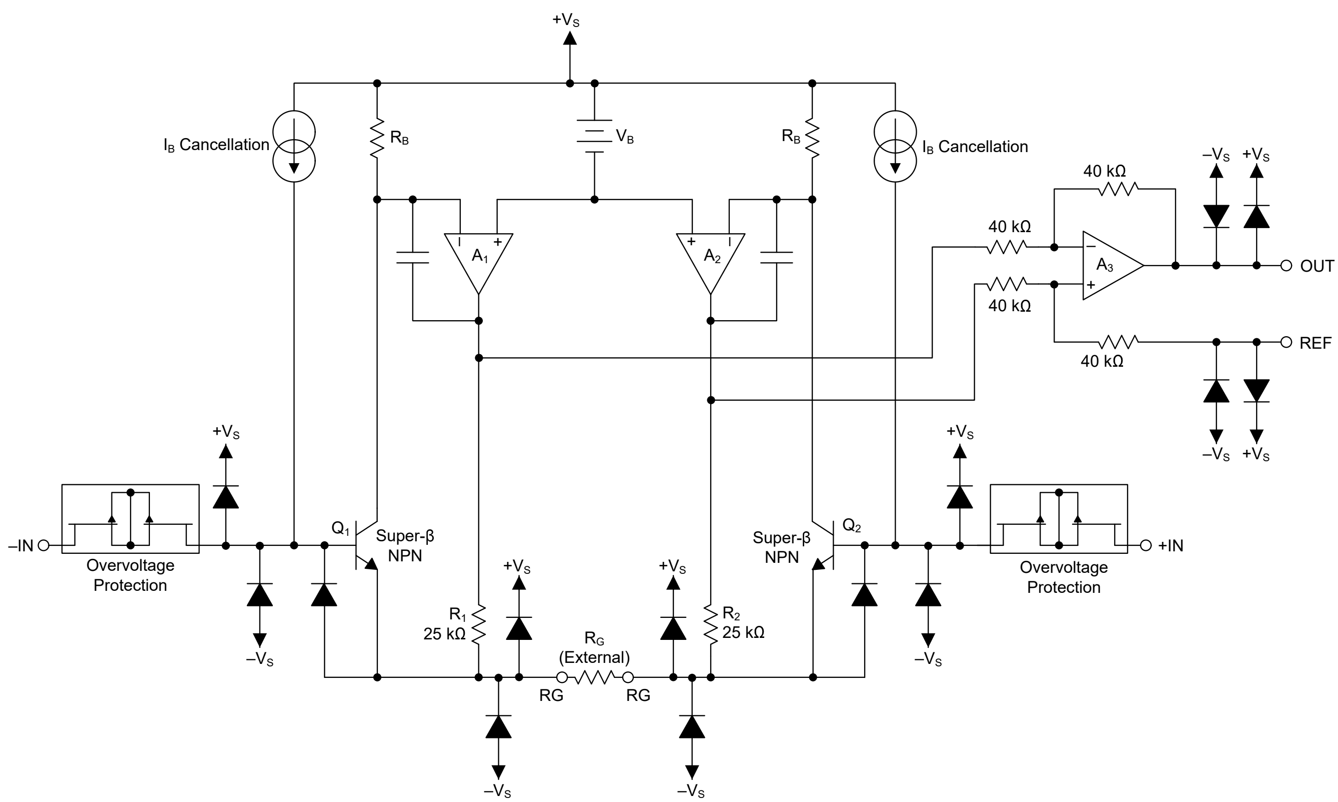
8 Detailed Description

8.1 Overview

The INA819 is a monolithic precision instrumentation amplifier that incorporates a current-feedback input stage and a four-resistor difference amplifier output stage. The functional block diagram in the next section shows how the differential input voltage is buffered by Q_1 and Q_2 and is forced across R_G, which causes a signal current to flow through R_G, R_1, and R_2. The output difference amplifier, A_3, removes the common-mode component of the input signal and refers the output signal to the REF pin. The V_{BE} and voltage drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 0.8 V lower than the input voltages.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8 mA.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Setting the Gain

图 8-1 shows that the gain of the INA819 is set by a single external resistor (R_G) connected between the RG pins (pins 1 and 8).

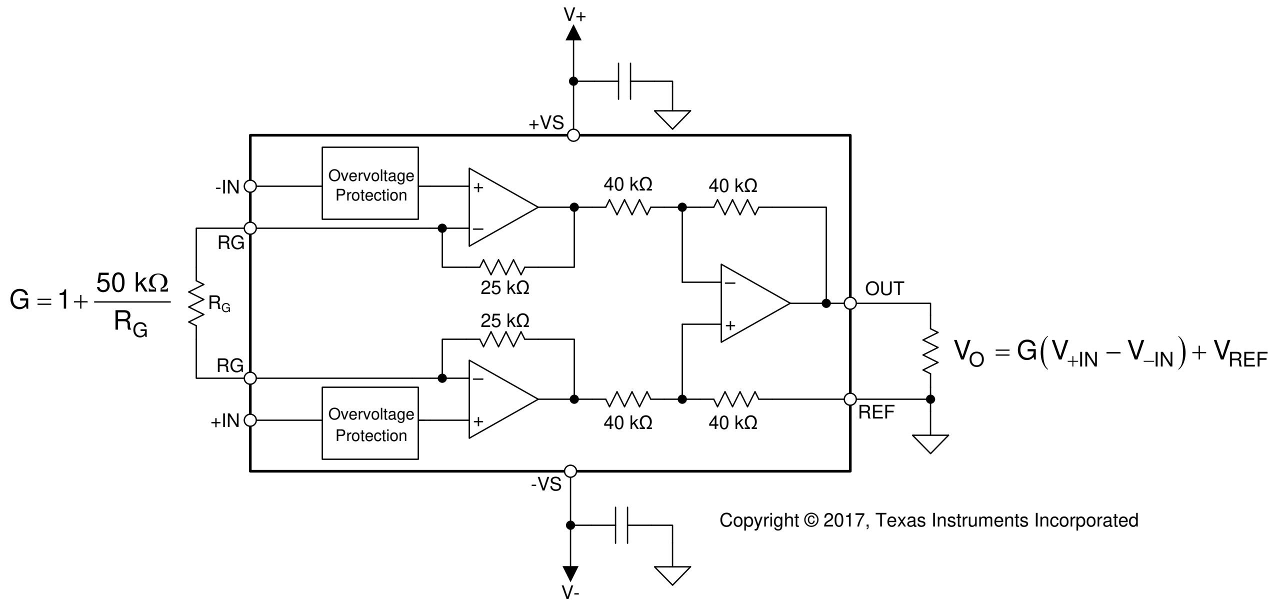


图 8-1. Simplified Diagram of the INA819 With Gain and Output Equations

The value of R_G is selected according to 方程式 1:

$$G = 1 + \frac{50\ k\Omega}{R_G} \tag{1}$$

表 8-1 lists several commonly used gains and resistor values. The 50-kΩ term in 方程式 1 is a result of the sum of the two internal 25-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA819. As shown in 图 8-1 and explained in more details in 节 11, make sure to connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground that are placed as close to the device as possible.

表 8-1. Commonly Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50 k	49.9 k
5	12.5 k	12.4 k
10	5.556 k	5.49 k
20	2.632 k	2.61 k
50	1.02 k	1.02 k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9

8.3.1.1 Gain Drift

The stability and temperature drift of the external gain setting resistor (R_G) also affects gain. The contribution of R_G to gain accuracy and drift is determined from 方程式 1.

The best gain drift of 5 ppm/℃ (maximum) is achieved when the INA819 uses G = 1 without R_G connected. In this case, gain drift is limited by the mismatch of the temperature coefficient of the integrated 40-kΩ resistors in the differential amplifier (A_3). At gains greater than 1, gain drift increases as a result of the individual drift of the 25-kΩ resistors in the feedback of A_1 and A_2, relative to the drift of the external gain resistor (R_G.) The low temperature coefficient of the internal feedback resistors improves the overall temperature stability of applications using gains greater than 1 V/V over alternate solutions.

Low resistor values required for high gain make wiring resistance an important consideration. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To maintain stability, avoid parasitic capacitance of more than a few picofarads at R_G connections. Careful matching of any parasitics on the R_G pins maintains optimal CMRR over frequency; see 图 7-17.

8.3.2 EMI Rejection

Texas Instruments developed a method to accurately measure the immunity of an amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. This method uses an EMI rejection ratio (EMIRR) to quantify the ability of the INA819 to reject EMI. The offset resulting from an input EMI signal is calculated using Equation 2:

$$\Delta V_{OS} = \left(\frac{V_{RF\_PEAK}{}^2}{100\ mV_P} \right) \cdot 10^{-\left(\frac{EMIRR\ (dB)}{20} \right)} \tag{2}$$

where

- V_{RF_PEAK} is the peak amplitude of the input EMI signal.

图 8-2 and 图 8-3 show the INA819 EMIRR graph for differential and common-mode EMI rejection across this frequency range. 表 8-2 lists the EMIRR values for the INA819 at frequencies commonly encountered in real-world applications. Applications listed in 表 8-2 are centered on or operated near the frequency shown. Depending on the end-system requirements, additional EMI filters may be required near the signal inputs of the system. Incorporating known good practices such as using short traces, low-pass filters, and damping resistors combined with parallel and shielded signal routing may be required.

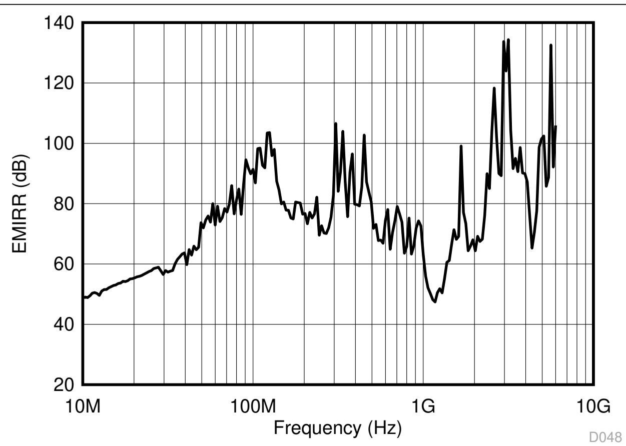


图 8-2. Common-Mode EMIRR Testing

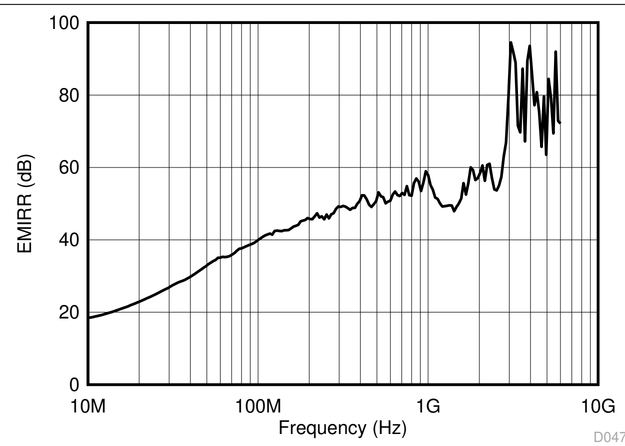


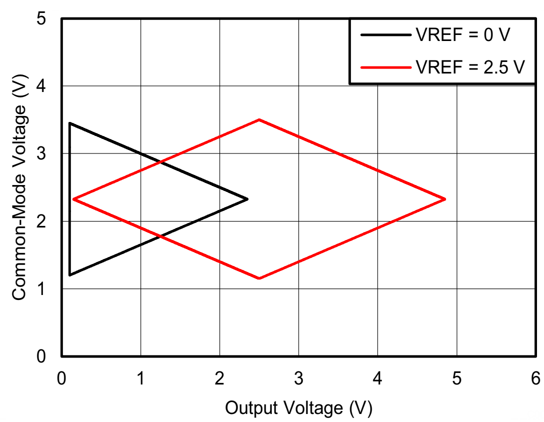
图 8-3. Differential Mode EMIRR Testing

表 8-2. INA819 EMIRR for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	DIFFERENTIAL EMIRR	COMMON-MODE EMIRR
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh-frequency (UHF) applications	52 dB	80 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (up to 1.6 GHz), GSM, aeronautical mobile, UHF applications	55 dB	71 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	58 dB	73 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	59 dB	95 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	78 dB	96 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	70 dB	100 dB

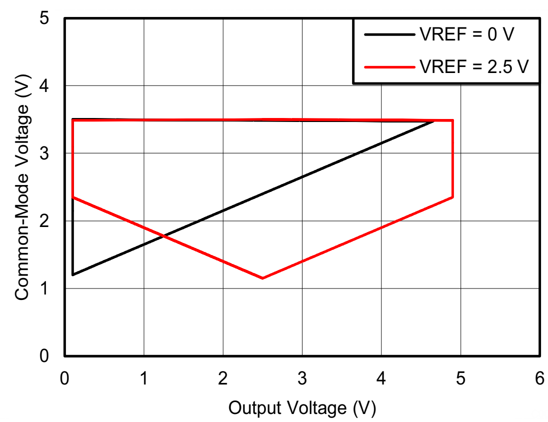
8.3.3 Input Common-Mode Range

The linear input voltage range of the INA819 input circuitry extends within 1.5 volts (typical) of both power supplies and maintains excellent common-mode rejection throughout this range. The common-mode range for the most common operating conditions are shown in 图 8-4 to 图 8-7. The common-mode range for other operating conditions is best calculated using the *Analog Engineers Calculator*.



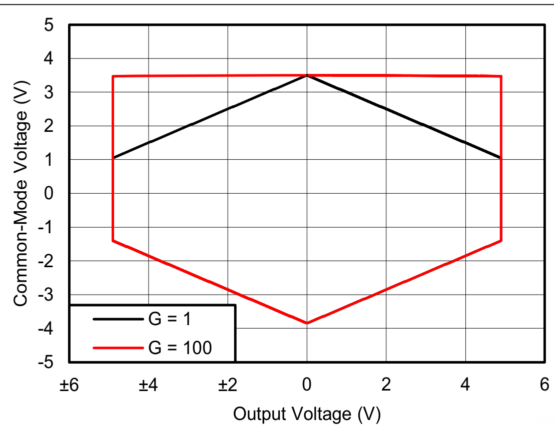
V_S = 5 V G = 1

图 8-4. Input Common-Mode Voltage vs Output Voltage



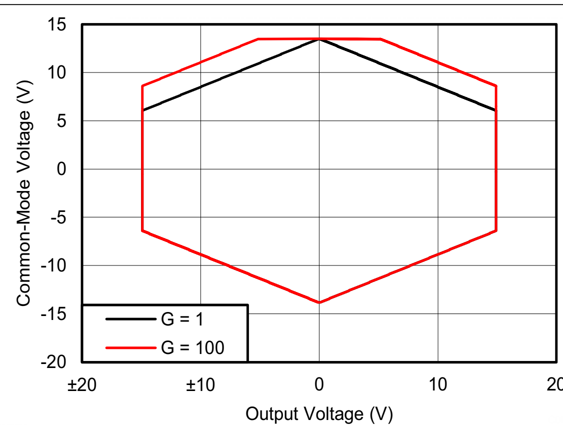
V_S = 5 V G = 100

图 8-5. Input Common-Mode Voltage vs Output Voltage



V_S = ±5 V V_{REF} = 0 V

图 8-6. Input Common-Mode Voltage vs Output Voltage



V_S = ±15 V V_{REF} = 0 V

图 8-7. Input Common-Mode Voltage vs Output Voltage

8.3.4 Input Protection

The inputs of the INA819 device are individually protected for voltages up to ±60 V. For example, a condition of –60 V on one input and +60 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately 8 mA.

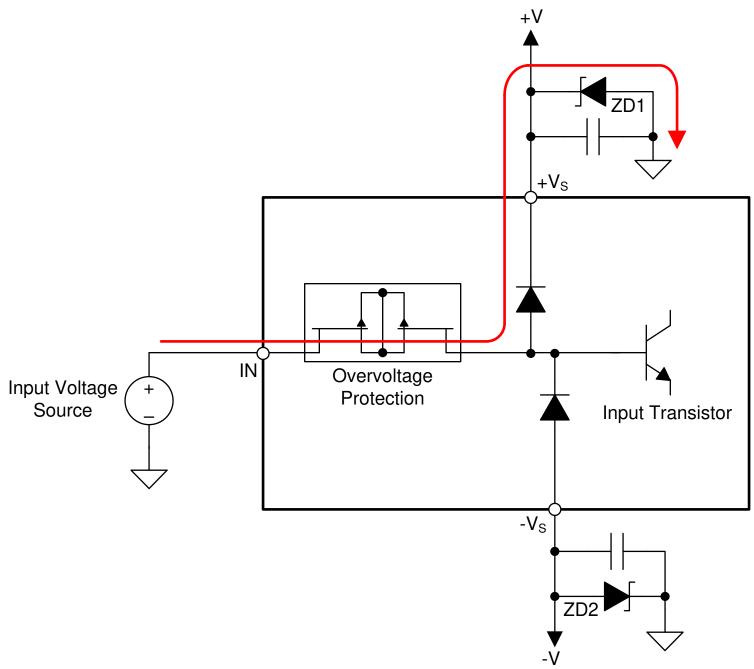


图 8-8. Input Current Path During an Overvoltage Condition

During an input overvoltage condition, current flows through the input protection diodes into the power supplies; see 图 8-8. If the power supplies are unable to sink current, then Zener diode clamps (ZD1 and ZD2 in 图 8-8) must be placed on the power supplies to provide a current pathway to ground. 图 8-9 shows the input current for input voltages from –50 V to 50 V when the INA819 is powered by ±15-V supplies.

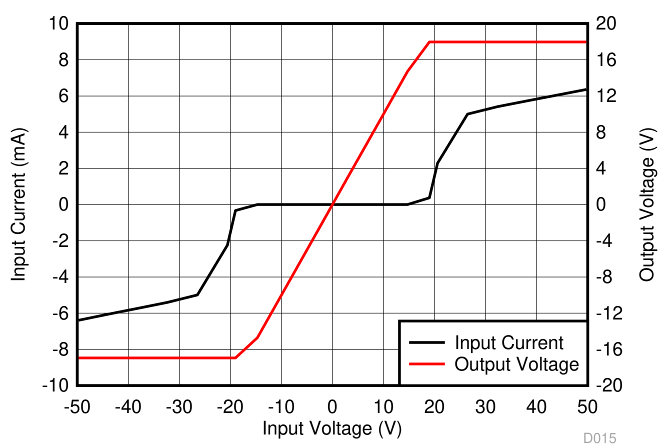


图 8-9. Input Current vs Input Overvoltage

8.3.5 Operating Voltage

The INA819 operates over a power-supply range of 4.5 V to 36 V (±2.25 V to ±18 V).

CAUTION

Supply voltages higher than 40 V (±20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in 节 7.6 .

8.3.6 Error Sources

Most modern signal-conditioning systems calibrate errors at room temperature. However, calibration of errors that result from a change in temperature is normally difficult and costly. Therefore, minimize these errors by choosing high-precision components, such as the INA819, that have improved specifications in critical areas that impact the precision of the overall system. 图 8-10 shows an example application.

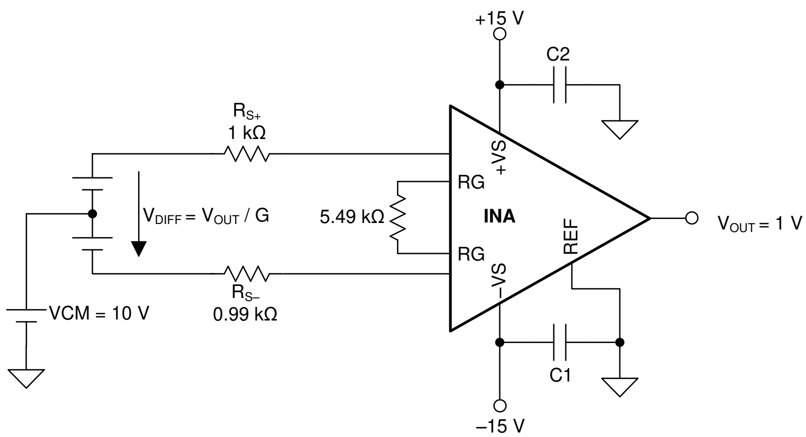


图 8-10. Example Application with G = 10 V/V and 1-V Output Voltage

Resistor-adjustable devices (such as the INA819) show the lowest gain error in G = 1 because of the inherently well-matched drift of the internal resistors of the differential amplifier. At gains greater than 1 (for instance, G = 10 V/V or G = 100 V/V), the gain error becomes a significant error source because of the contribution of the resistor drift of the 25-kΩ feedback resistors in conjunction with the external gain resistor. Except for very high gain applications, the gain drift is by far the largest error contributor compared to other drift errors, such as offset drift.

The INA819 offers excellent gain error over temperature for both G > 1 and G = 1 (no external gain resistor). 表 8-4 summarizes the major error sources in common INA applications and compares the three cases of G = 1 (no external resistor) and G = 10 (5.49-kΩ external resistor) and G = 100 (511-Ω external resistor). All calculations are assuming an output voltage of V_{OUT} = 1 V. Thus, the input signal V_{DIFF} (given by $V_{DIFF} = V_{OUT}/G$) exhibits smaller and smaller amplitudes with increasing gain G. In this example, V_{DIFF} = 1 mV at G = 1000. All calculations refer the error to the input for easy comparison and system evaluation. As 表 8-4 shows, errors generated by the input stage (such as input offset voltage) are more dominant at higher gain, while the effects of output stage are suppressed because they are divided by the gain when referring them back to the input. The gain error and gain drift error are much more significant for gains greater than 1 because of the contribution of the resistor drift of the 25-kΩ feedback resistors in conjunction with the external gain resistor. In most applications, static errors (absolute accuracy errors) can readily be removed during calibration in production, while the drift errors are the key factors limiting overall system performance.

表 8-3. System Specifications for Error Calculation

QUANTITY	VALUE	UNIT
V_{OUT}	1	V
VCM	10	V
VS	1	V
R_{S+}	1000	Ω
R_{S-}	999	Ω
RG tolerance	0.01	%
RG drift	10	ppm/°C
Temperature range upper limit	105	°C

表 8-4. Error Calculation

ERROR SOURCE	ERROR CALCULATION	INA819 VALUES				
		SPECIFICATION	UNIT	G = 1 ERROR (ppm)	G = 100 ERROR (ppm)	G = 1000 ERROR (ppm)
ABSOLUTE ACCURACY AT 25°C						
Input offset voltage	V_{OSI} / V_{DIFF}	35	µV	35	350	3500
Output offset voltage	$V_{OSO} / (G \times V_{DIFF})$	300	µV	300	300	300
Input offset current	$I_{OS} \times$ maximum $(R_{S+}, R_{S-}) / V_{DIFF}$	0.5	nA	1	5	50
CMRR (min)	$V_{CM} / (10^{CMRR/20} \times V_{DIFF})$	90 (G = 1), 110 (G = 10), 130 (G = 100)	dB	316	316	316
PSRR (min)	$(V_{CC} - V_S) / (10^{PSRR/20} \times V_{DIFF})$	110 (G = 1), 114 (G = 10), 130 (G = 100)	dB	3	20	32
Gain error from INA (max)	$GE(\%) \times 10^4$	0.02 (G = 1), 0.15 (G = 10, 100)	%	200	1500	1500
Gain error from external resistor RG (max)	$GE(\%) \times 10^4$	0.01	%	100	100	100
Total absolute accuracy error (ppm) at 25°C, worst case	sum of all errors	—	—	955	2591	5798
Total absolute accuracy error (ppm) at 25°C, average	rms sum of all errors	—	—	491	1604	3835
DRIFT TO 105°C						
Gain drift from INA (max)	$GTC \times (T_A - 25)$	5 (G = 1), 35 (G = 10, 100)	ppm/°C	400	2800	2800
Gain drift from external resistor RG (max)	$GTC \times (T_A - 25)$	10	ppm/°C	800	800	800
Input offset voltage drift (max)	$(V_{OSI\_TC} / V_{DIFF}) \times (T_A - 25)$	0.4	µV/°C	32	320	3200
Output offset voltage drift	$[V_{OSO\_TC} / (G \times V_{DIFF})] \times (T_A - 25)$	5	µV/°C	400	400	400
Offset current drift	$I_{OS\_TC} \times$ maximum $(R_{S+}, R_{S-}) \times (T_A - 25) / V_{DIFF}$	20	pA/°C	2	16	160
Total drift error to 105°C (ppm), worst case	sum of all errors	—	—	1634	4336	7360
Total drift error to 105°C (ppm), typical	rms sum of all errors	—	—	980	2957	4348
RESOLUTION						
Gain nonlinearity		10 (G = 1, 10), 15 (G = 100)	ppm of FS	10	10	15
Voltage noise (at 1 kHz)	$\sqrt{BW} \times \sqrt{(e_{NI}^2 + \left[\frac{e_{NO}}{G}\right]^2} \times \frac{6}{V_{DIFF}}$	e_{NI} = 8, e_{NO} = 90	$µV_{PP}$	1204	1070	3941
Current noise (at 1kHz)	$I_N \times$ maximum $(R_{S+}, R_{S-}) \times \sqrt{BW} / V_{DIFF}$	0.13	pA/ √ Hz	0.3	2	11
Total resolution error (ppm), worst case	sum of all errors	—	—	1214	1080	3956
Total resolution error (ppm), typical	rms sum of all errors	—	—	1204	1070	3941
TOTAL ERROR						
Total error (ppm), worst case	sum of all errors	—	—	3802	8007	17113

表 8-4. Error Calculation (continued)

ERROR SOURCE	ERROR CALCULATION	INA819 VALUES				
		SPECIFICATION	UNIT	G = 1 ERROR (ppm)	G = 100 ERROR (ppm)	G = 1000 ERROR (ppm)
Total error (ppm), typical	rms sum of all errors	—	—	1628	3530	7010

8.4 Device Functional Modes

The INA819 has a single functional mode and operates when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power-supply voltage for the INA819 is 36 V (±18 V.)

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

9.1.1 Reference Pin

The output voltage of the INA819 is developed with respect to the voltage on the reference pin (REF.) Often, in dual-supply operation, REF (pin 6) is connected to the low-impedance system ground. In single-supply operation, offsetting the output signal to a precise midsupply level is useful (for example, 2.5 V in a 5-V supply environment). To accomplish this level shift, a voltage source must be connected to the REF pin to level-shift the output so that the INA819 drives a single-supply analog-to-digital converter (ADC).

The voltage source applied to the reference pin must have a low output impedance. As shown in 图 9-1, any resistance at the reference pin (shown as R_{REF} in 图 9-1) is in series with an internal 40-kΩ resistor.

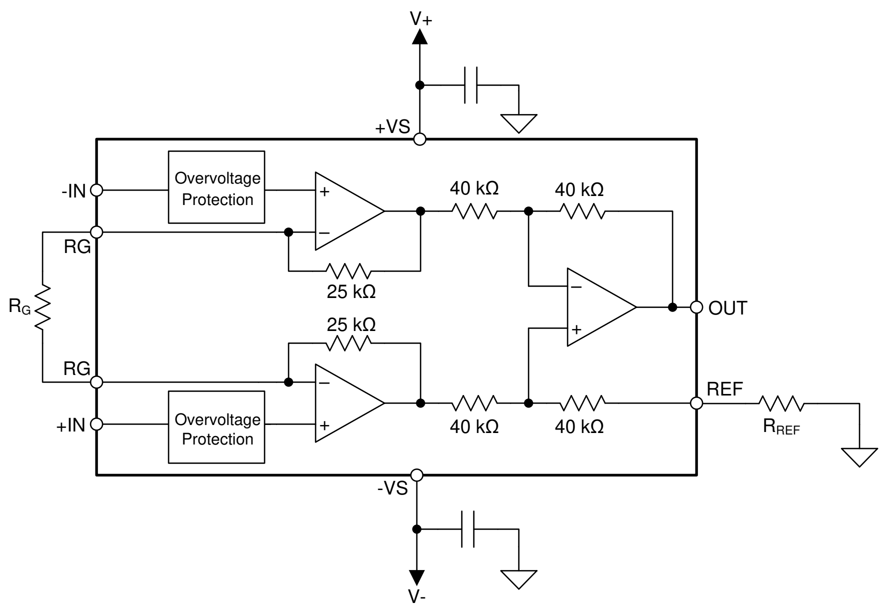


图 9-1. Parasitic Resistance Shown at the Reference Pin

The parasitic resistance at the reference pin (R_{REF}) creates an imbalance in the four resistors of the internal difference amplifier that results in a degraded common-mode rejection ratio (CMRR). 图 9-2 shows the degradation in CMRR of the INA819 as a result of increased resistance at the reference pin. For the best performance, keep the source impedance to the REF pin (R_{REF}) less than 5 Ω.

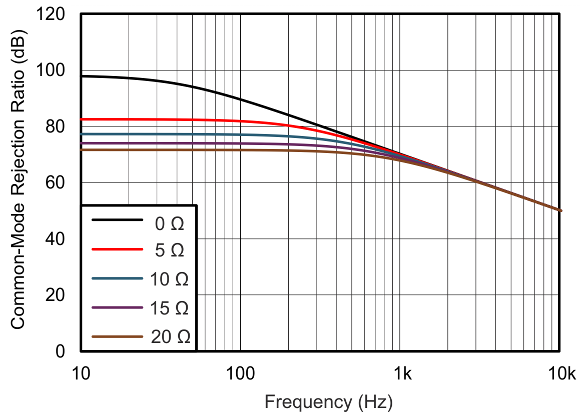


图 9-2. The Effect of Increasing Resistance at the Reference Pin

Voltage reference devices are an excellent option for providing a low-impedance voltage source for the reference pin. However, if a resistor voltage divider generates a reference voltage, the divider must be buffered by an op amp, as 图 9-3 shows, to avoid CMRR degradation.

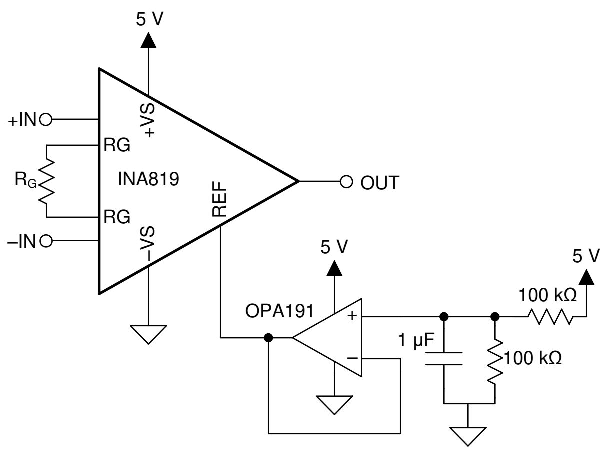


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图 9-3. Using an Op Amp to Buffer Reference Voltages

9.1.2 Input Bias Current Return Path

The input impedance of the INA819 is extremely high—approximately 100 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically 150 pA. High input impedance means that this input bias current changes very little with varying input voltage.

For proper operation, input circuitry must provide a path for input bias current. 图 9-4 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA819, and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can connect to one input (as shown in the thermocouple example in 图 9-4). With a higher source impedance, using two equal resistors provides a balanced input with possible advantages of a lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

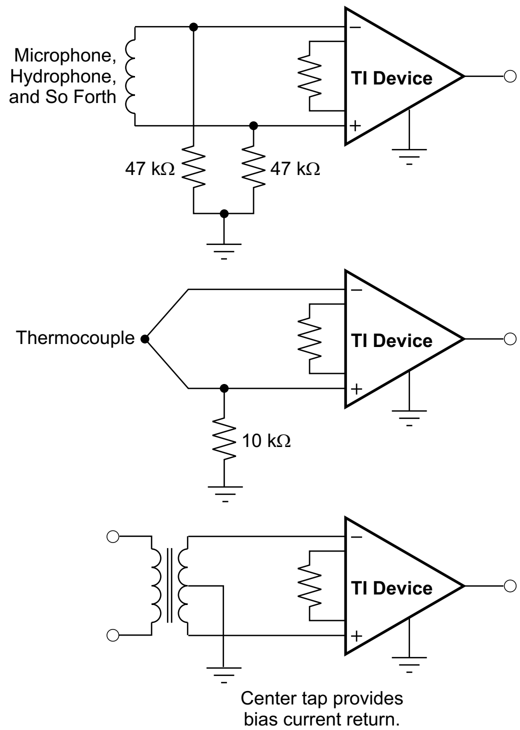

图 9-4. Providing an Input Common-Mode Current Path

9.2 Typical Applications

9.2.1 Three-Pin Programmable Logic Controller (PLC)

图 9-5 shows a three-pin programmable-logic controller (PLC) design for the INA819. This PLC reference design accepts inputs of ±10 V or ±20 mA. The output is a single-ended voltage of 2.5 V ±2.3 V (or 200 mV to 4.8 V). Many PLCs typically have these input and output ranges.

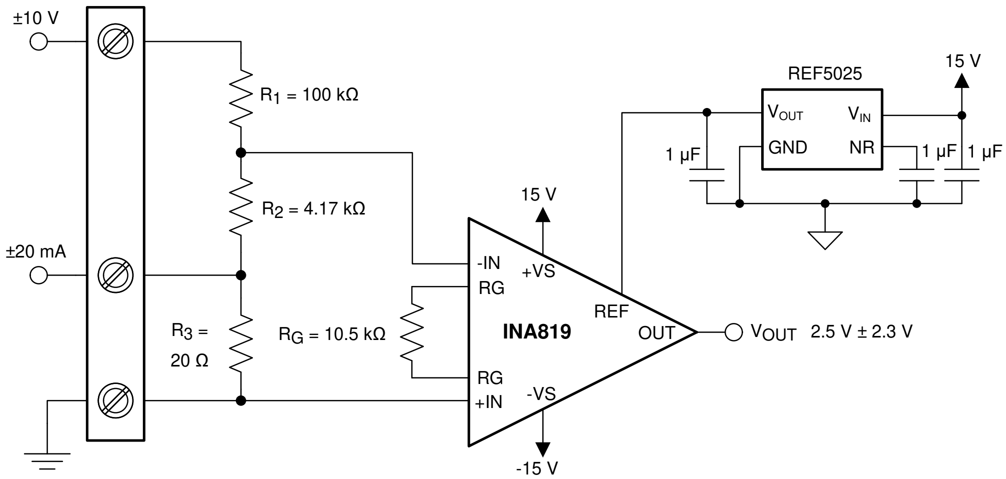

图 9-5. PLC Input (±10 V, 4 mA to 20 mA)

9.2.1.1 Design Requirements

For this application, the design requirements are as follows:

- 4-mA to 20-mA input with less than 20-Ω burden
- ±20-mA input with less than 20-Ω burden
- ±10-V input with impedance of approximately 100 kΩ
- Maximum 4-mA to 20-mA or ±20-mA burden voltage equal to ±0.4 V
- Output range within 0 V to 5 V

9.2.1.2 Detailed Design Procedure

There are two modes of operation for the circuit shown in 图 9-5: current input and voltage input. This design requires $R_1 >> R_2 >> R_3$. Given this relationship, Equation 3 calculates the current input mode transfer function.

$$V_{OUT-I} = V_D \times G + V_{REF} = -(I_{IN} \times R_3) \times G + V_{REF} \tag{3}$$

where

- G represents the gain of the instrumentation amplifier.
- V_D represents the differential voltage at the INA819 inputs.
- V_{REF} is the voltage at the INA819 REF pin.
- I_{IN} is the input current.

Equation 4 shows the transfer function for the voltage input mode.

$$V_{OUT-V} = V_D \times G + V_{REF} = -\left(V_{IN} \times \frac{R_2}{R_1 + R_2}\right) \times G + V_{REF} \tag{4}$$

where

- V_{IN} is the input voltage.

R_1 sets the input impedance of the voltage input mode. The minimum typical input impedance is 100 kΩ. The R_1 value is 100 kΩ because increasing the R_1 value also increases noise. The value of R_3 must be extremely small compared to R_1 and R_2. 20 Ω for R_3 is selected because that resistance value is much smaller than R_1 and yields an input voltage of ±400 mV when operated in current mode (±20 mA).

Use Equation 5 to calculate R_2 given V_D = ±400 mV, V_{IN} = ±10 V, and R_1 = 100 kΩ.

$$V_D = V_{IN} \times \frac{R_2}{R_1 + R_2} \rightarrow R_2 = \frac{R_1 \times V_D}{V_{IN} - V_D} = 4.167\ k\Omega \tag{5}$$

The value obtained from Equation 5 is not a standard 0.1% value, so 4.17 kΩ is selected. R_1 and R_2 also use 0.1% tolerance resistors to minimize error.

Use Equation 6 to calculate the ideal gain of the instrumentation amplifier.

$$G = \frac{V_{OUT} - V_{REF}}{V_D} = \frac{4.8\ V - 2.5\ V}{400\ mV} = 5.75\ \frac{V}{V} \tag{6}$$

Equation 7 calculates the gain-setting resistor value using the INA819 gain equation (方程式 1).

$$R_G = \frac{50\ k\Omega}{G - 1} = \frac{50\ k\Omega}{5.75 - 1} = 10.5\ k\Omega \tag{7}$$

Use a standard 0.1% resistor value of 10.5 kΩ for this design.

9.2.1.3 Application Curves

图 9-6 and 图 9-7 show typical characteristic curves for the circuit in 图 9-5.

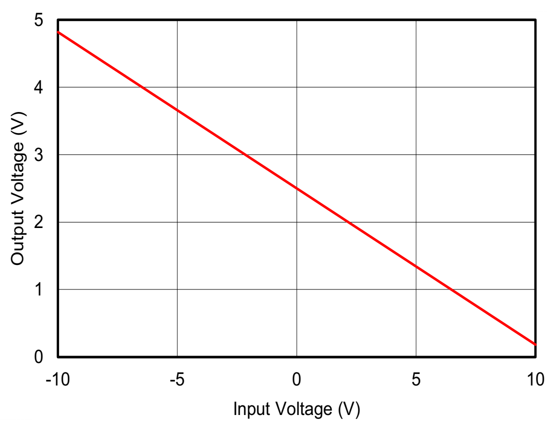

图 9-6. PLC Output Voltage vs Input Voltage

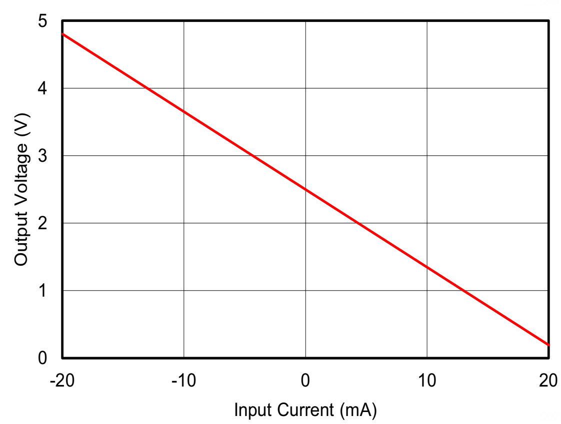

图 9-7. PLC Output Voltage vs Input Current

9.2.2 Resistance Temperature Detector Interface

图 9-8 illustrates a 3-wire interface circuit for resistance temperature detectors (RTDs). The circuit incorporates analog linearization and has an output voltage range from 0 V to 5 V. The linearization technique employed is described in *Analog linearization of resistance temperature detectors* analog application journal. Series and parallel combinations of standard 1% resistor values are used to achieve less than 0.02°C of error over a 200°C temperature span.

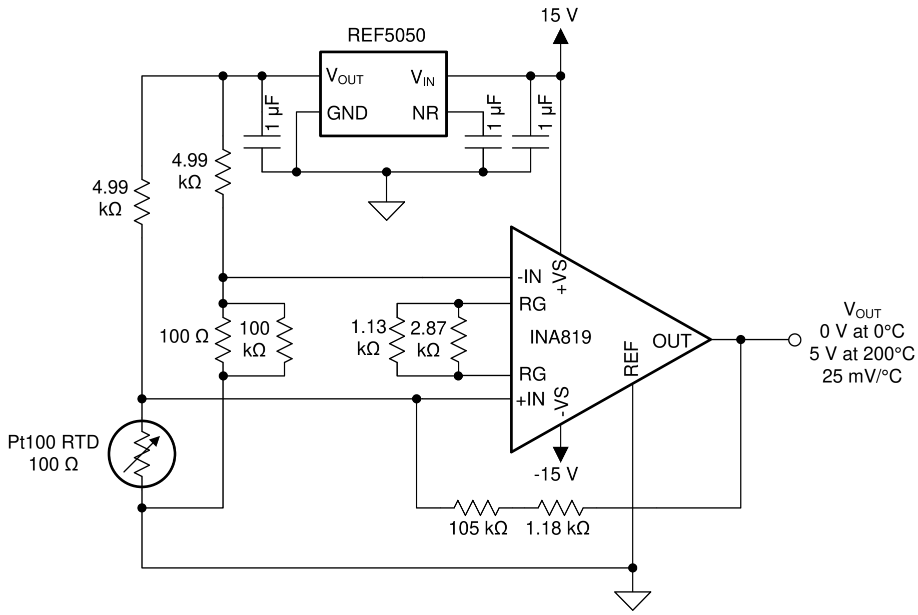

图 9-8. A 3-Wire Interface for RTDs With Analog Linearization

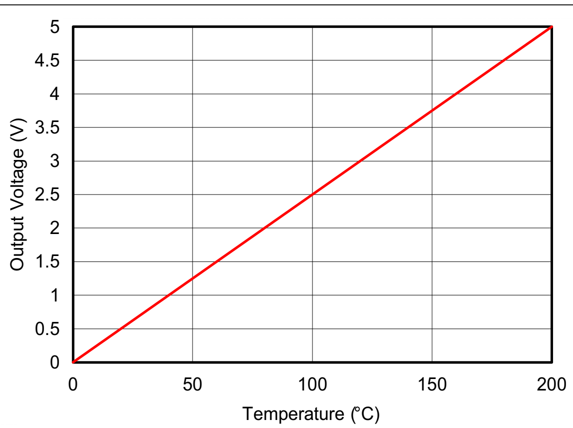

图 9-9. Transfer Function of a 3-Wire RTD Interface

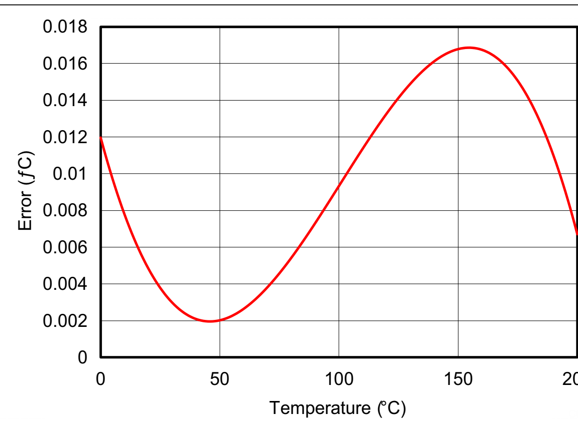

图 9-10. Temperature Error Over the Full Temperature Range

10 Power Supply Recommendations

The nominal performance of the INA819 is specified with a supply voltage of ±15 V and midsupply reference voltage. The device also operates using power supplies from ±2.25 V (4.5 V) to ±18 V (36 V) and non-midsupply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are shown in the *节 7.6* section.

11 Layout

11.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Take care to make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. Even slight mismatch in parasitic capacitance at the gain setting pins can degrade CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G, select the component so that the switch capacitance is as small as possible and most importantly so that capacitance mismatch between the RG pins is minimized.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 图 11-1, keep R_G close to the pins to minimize parasitic capacitance.
- Keep the traces as short as possible.
- Connect exposed thermal pad to negative supply –V.

11.2 Layout Example

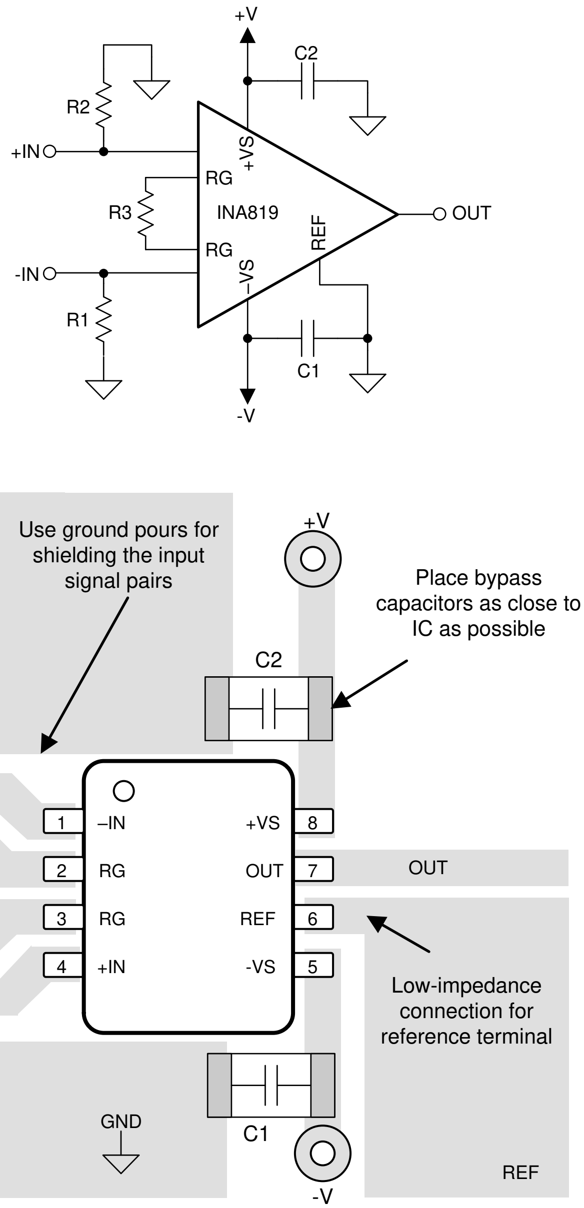

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图 11-1. Example Schematic and Associated PCB Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

12.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

备注

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *Comprehensive Error Calculation for Instrumentation Amplifiers* application note

12.3 接收文档更新通知

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA819ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA819
INA819ID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA819
INA819IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1X3Q
INA819IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1X3Q
INA819IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1X3Q
INA819IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1X3Q
INA819IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA819
INA819IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA819
INA819IDRGR	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	INA819
INA819IDRGR.B	Active	Production	SON (DRG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	INA819
INA819IDRGT	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	INA819
INA819IDRGT.B	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	INA819
INA819IDRGTG4	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	INA819
INA819IDRGTG4.B	Active	Production	SON (DRG) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	INA819

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

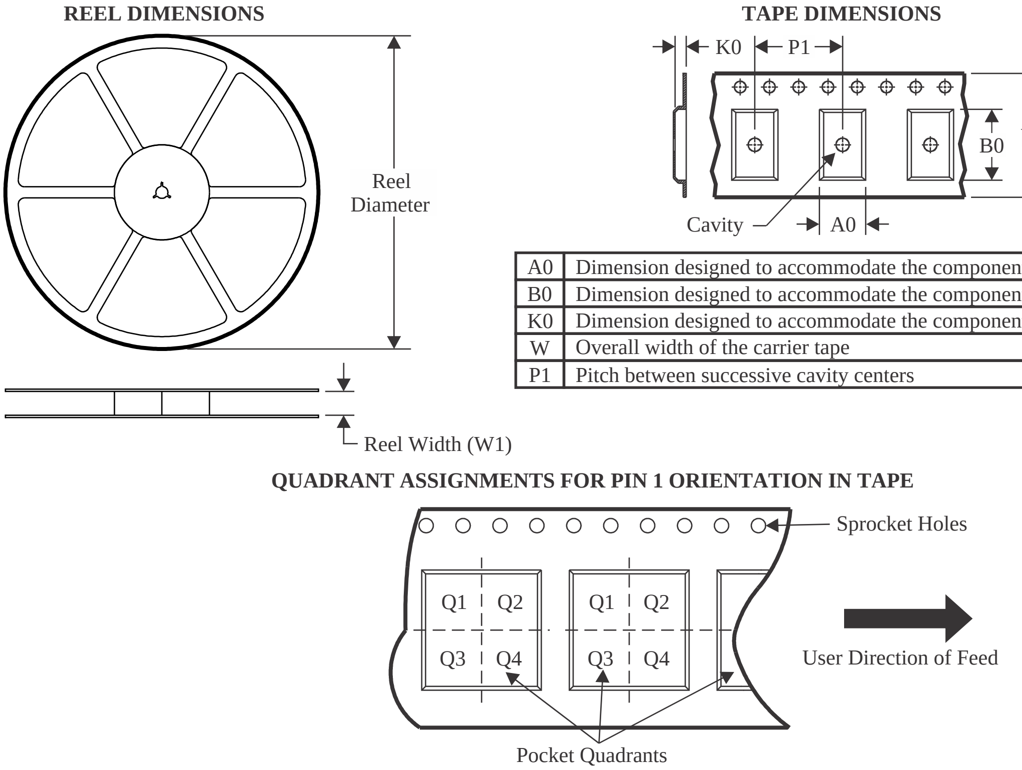
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

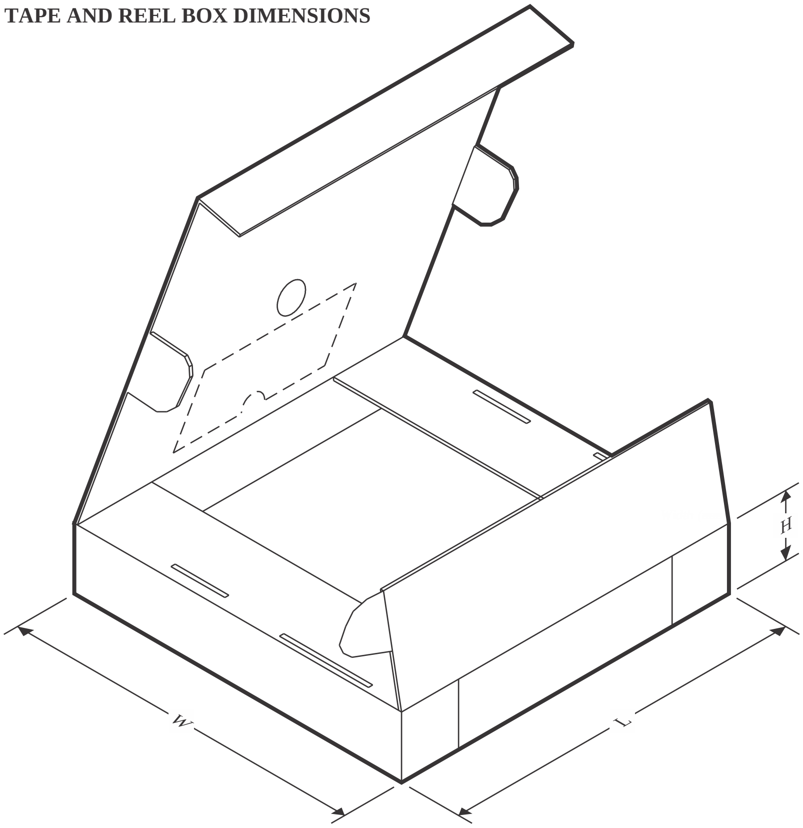


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA819IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA819IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
INA819IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA819IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA819IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA819IDRGTG4	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

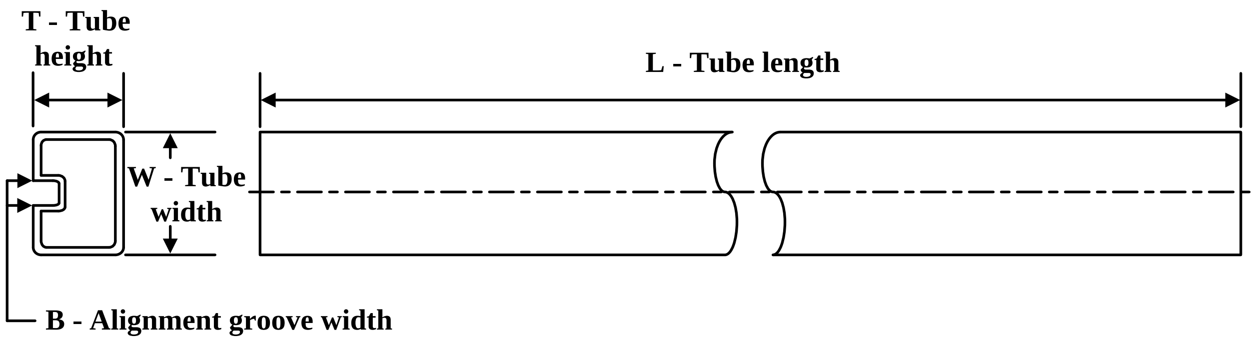
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

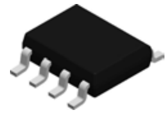
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA819IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA819IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
INA819IDR	SOIC	D	8	2500	353.0	353.0	32.0
INA819IDRGR	SON	DRG	8	3000	367.0	367.0	35.0
INA819IDRGT	SON	DRG	8	250	210.0	185.0	35.0
INA819IDRGTG4	SON	DRG	8	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA819ID	D	SOIC	8	75	506.6	8	3940	4.32
INA819ID.B	D	SOIC	8	75	506.6	8	3940	4.32

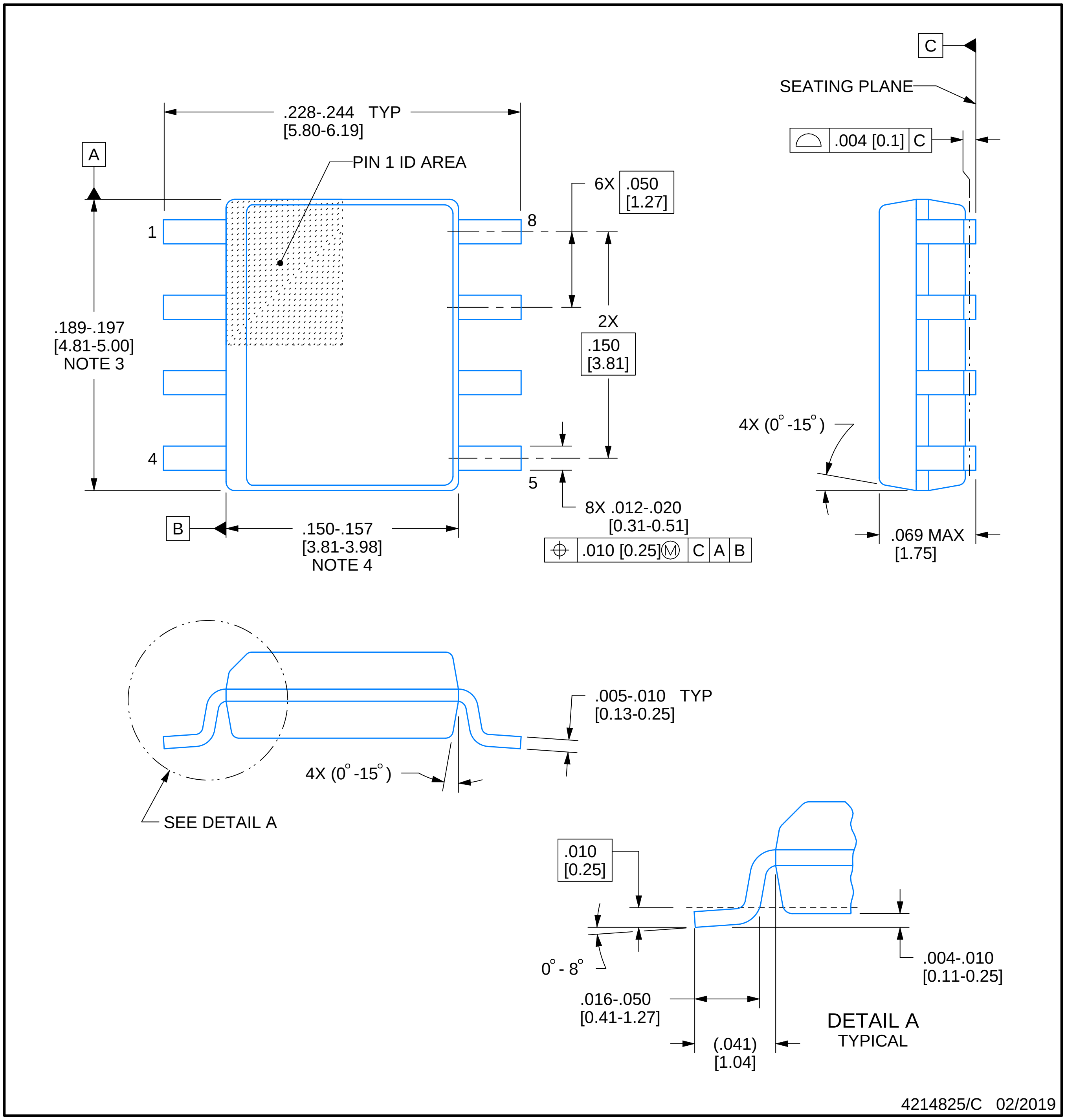


PACKAGE OUTLINE

D0008A

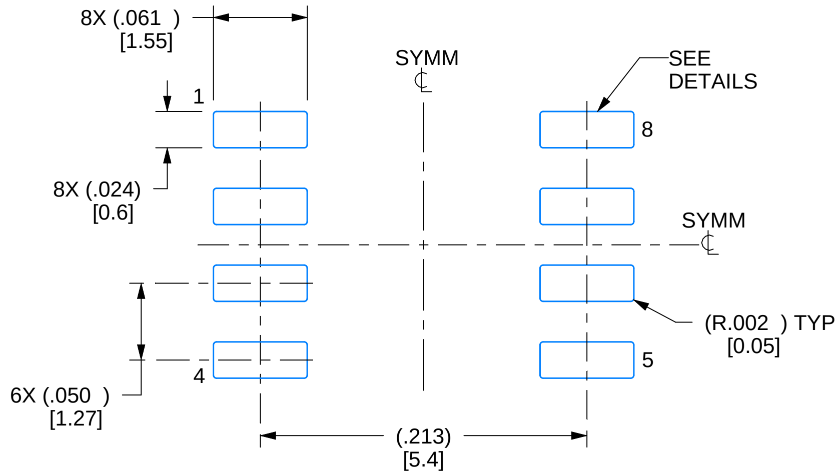
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

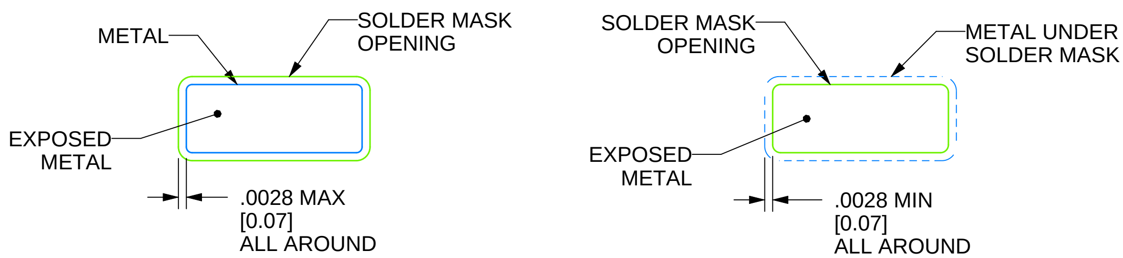


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

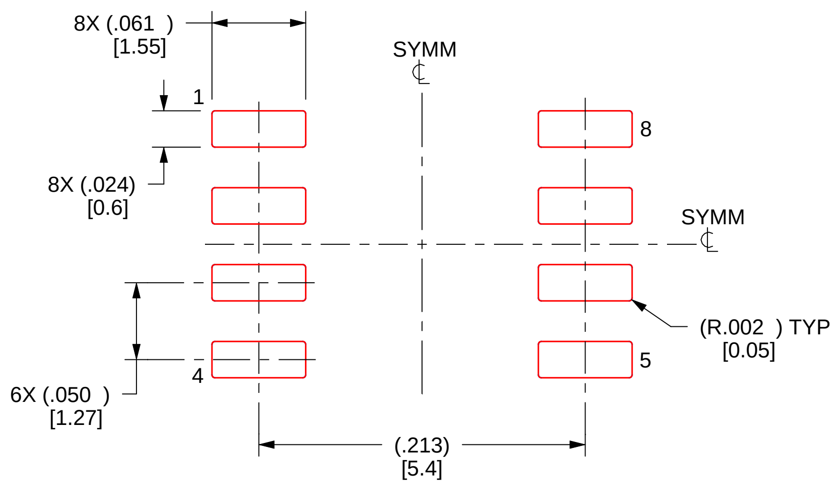
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

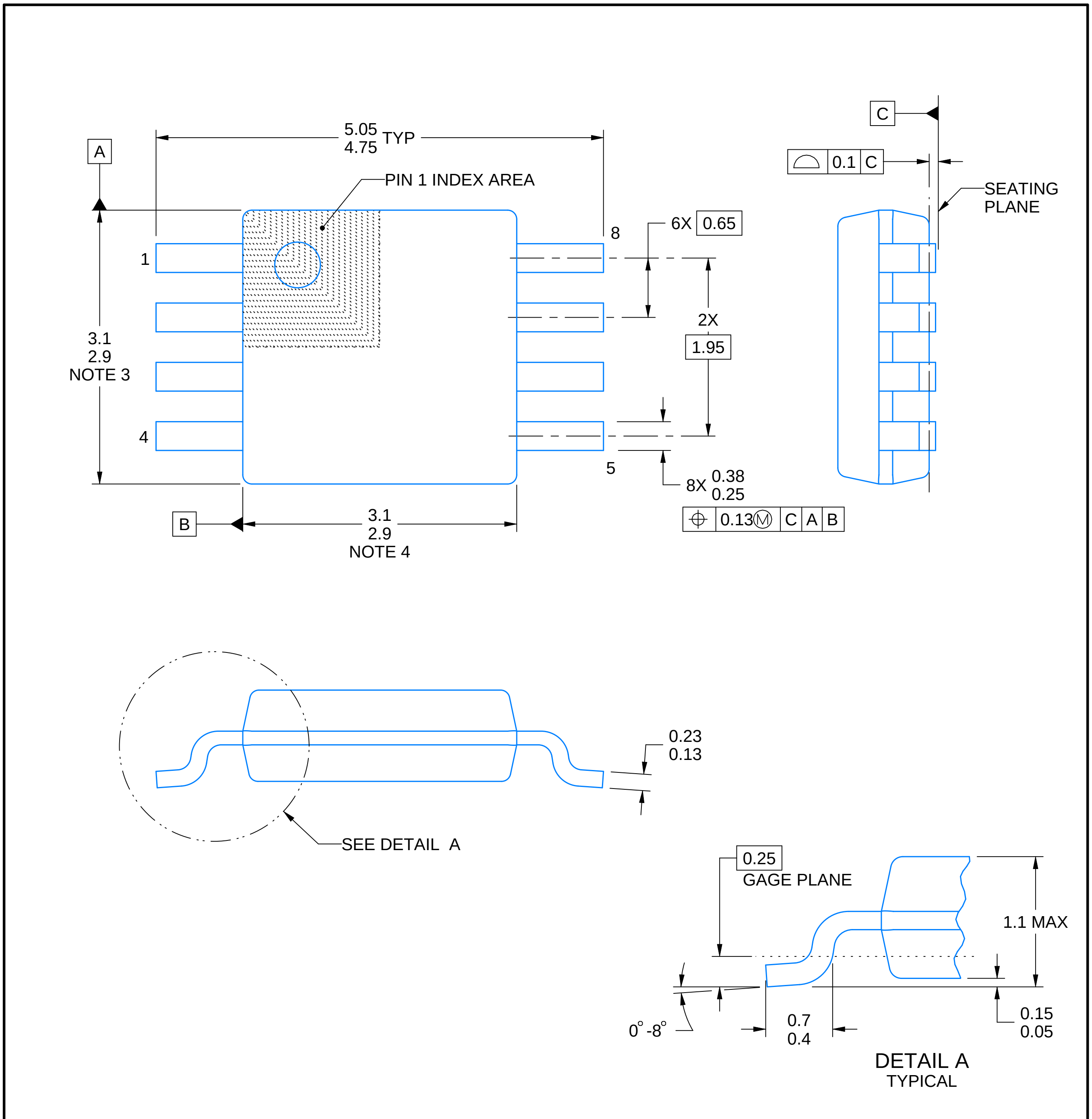


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

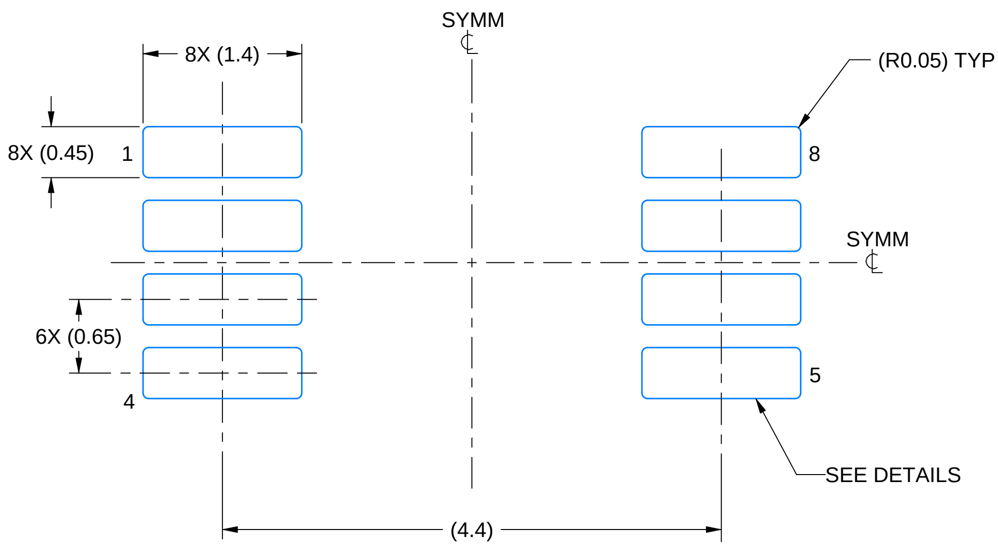
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



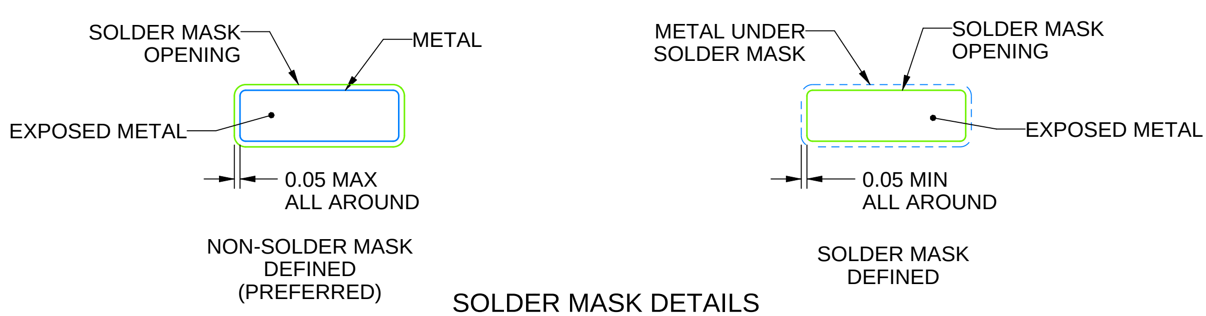
4214862/A 04/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

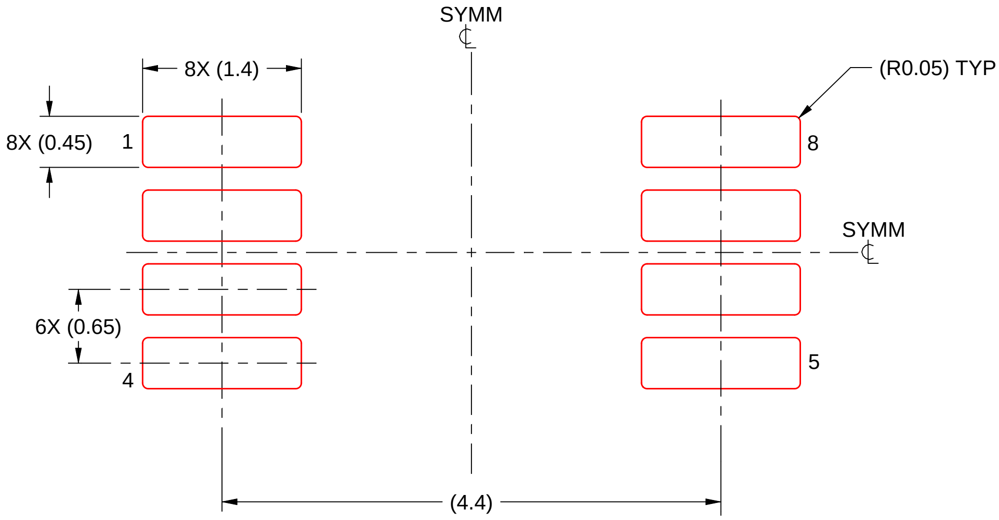


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

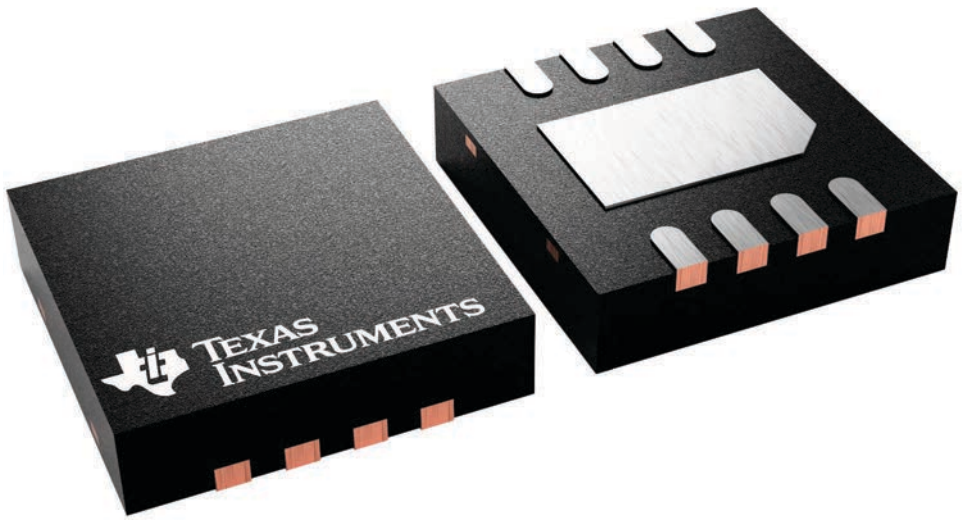
DRG 8

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

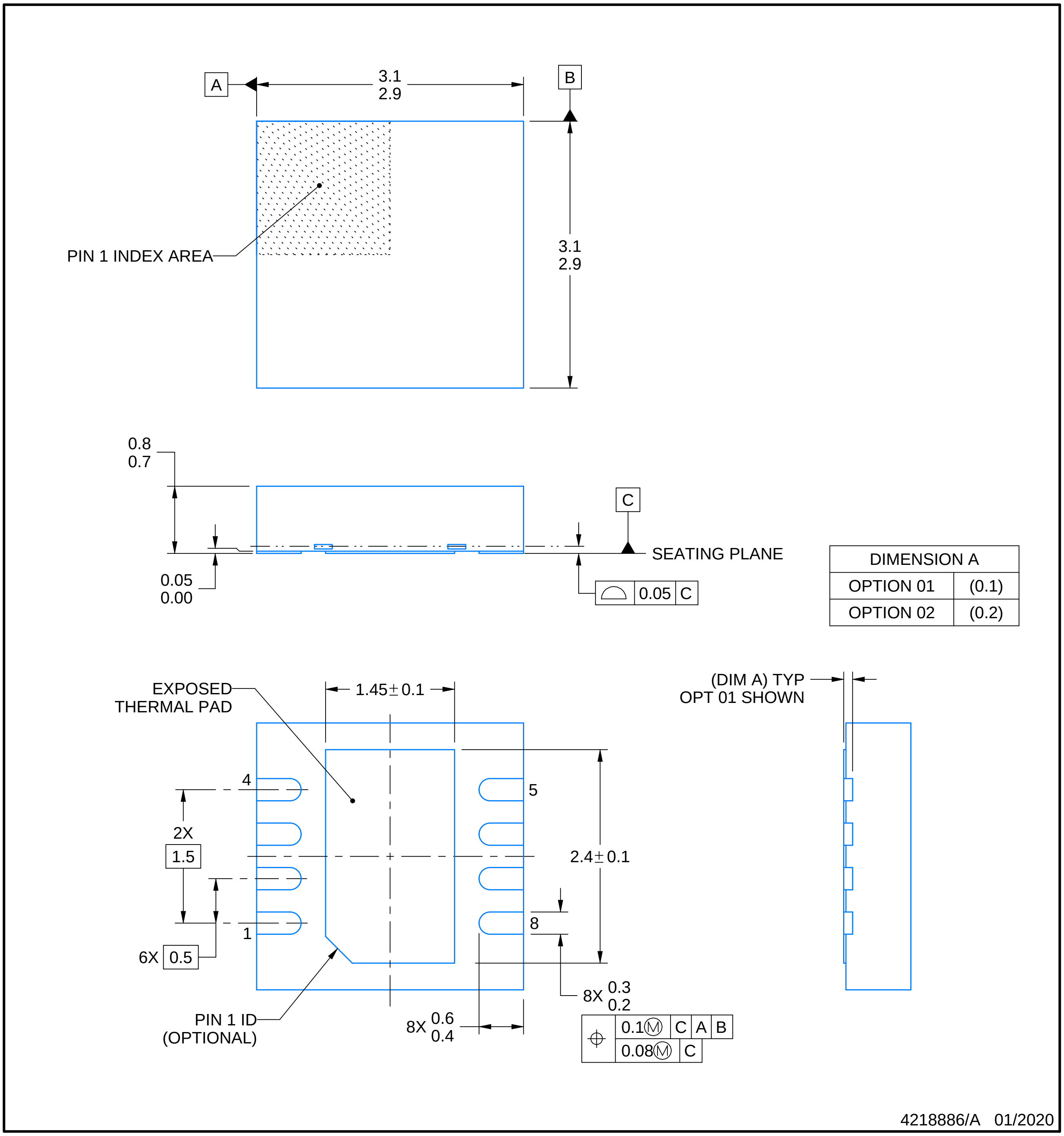


4225794/A

PACKAGE OUTLINE

WSON - 0.8 mm max height

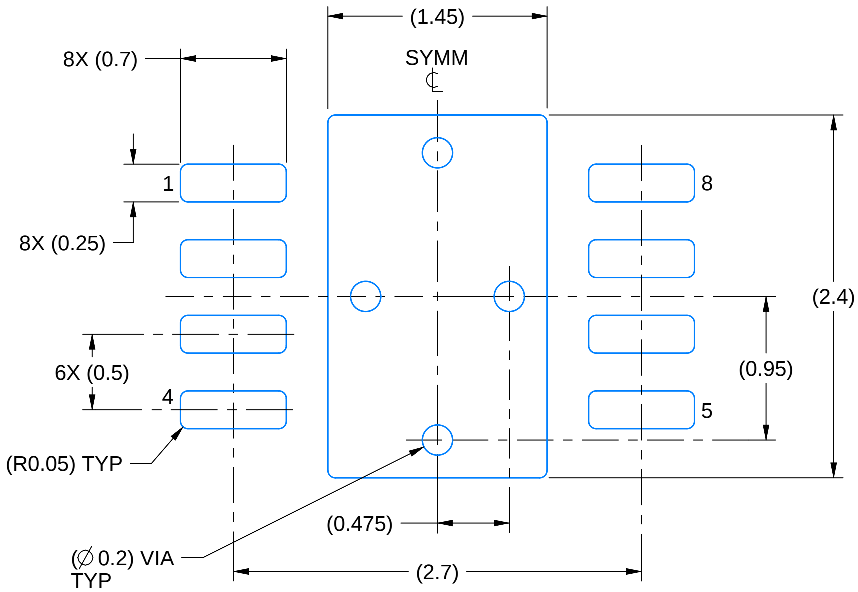
PLASTIC SMALL OUTLINE - NO LEAD



DIMENSION A	
OPTION 01	(0.1)
OPTION 02	(0.2)

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

NON SOLDER MASK
DEFINED
(PREFERRED)

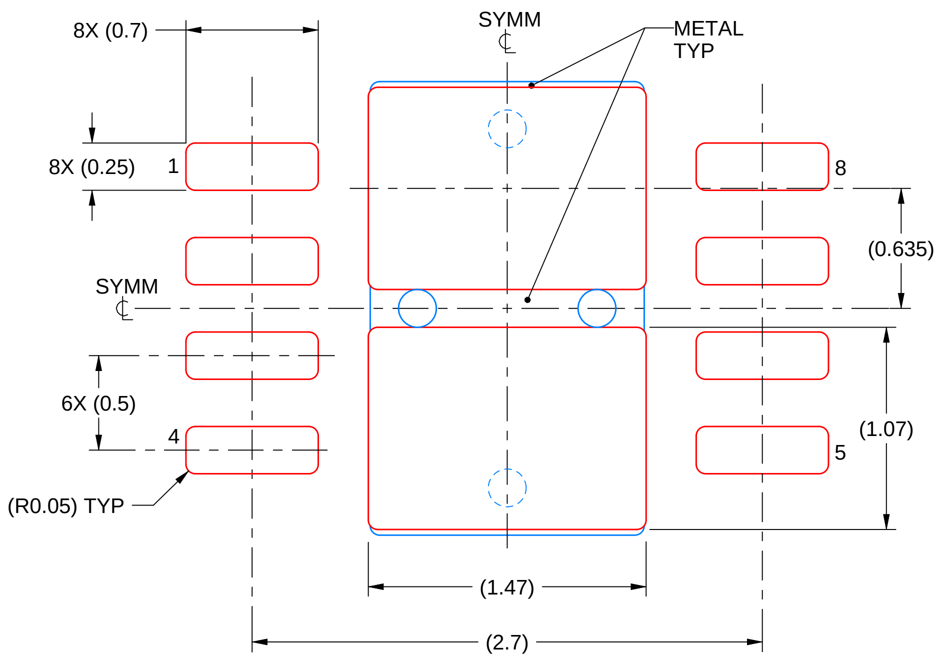
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218886/A 01/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218886/A 01/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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