High Voltage Level Shifter for TFT-LCD Panel

General Description

The RT8982B is a 19-Channel high-voltage level-shifter application such as TVs. The device converts logic level signals generated by the Timing Controller (T-con) to high level signals used by the display panel. With being available in a VQFN-48L 6x6 package, this device is suitable for GIP TFT-LCD/POLED panel.

Level shifter is designed for generating a high voltage signal to drive the TFT LCD panel. It provides 19 outputs (CLK1 to CLK12, STV1 to STV2, LC1 to LC2, DSCG1 to DSCG2, and RESET) which are switching from VGL to VGH and VSS1 to VGH and VSS2 to VGH with capacitive loads. It also integrates reset function.

Ordering Information

RT8982B □□

- Package Type
  QV : VQFN-48L 6x6 (V-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

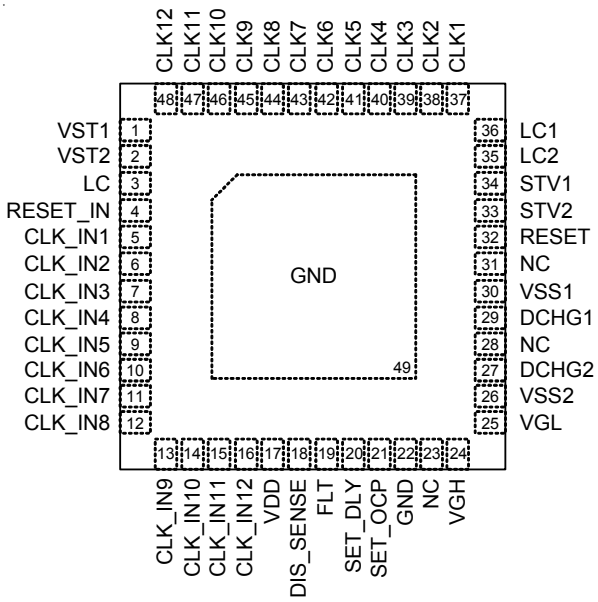
- **High-Voltage**
  - **–20V to 40V Output Voltage Range**
  - **Slew Rate to Drive up to 4.7nF Load**
- **DCHG1 and DCHG2 Discharge Function**
- **Short-Circuit Protection**
- **Over-Temperature Protection**
- **Wide 48-Lead VQFN Package**

Applications

- GIP TFT-LCD Panel

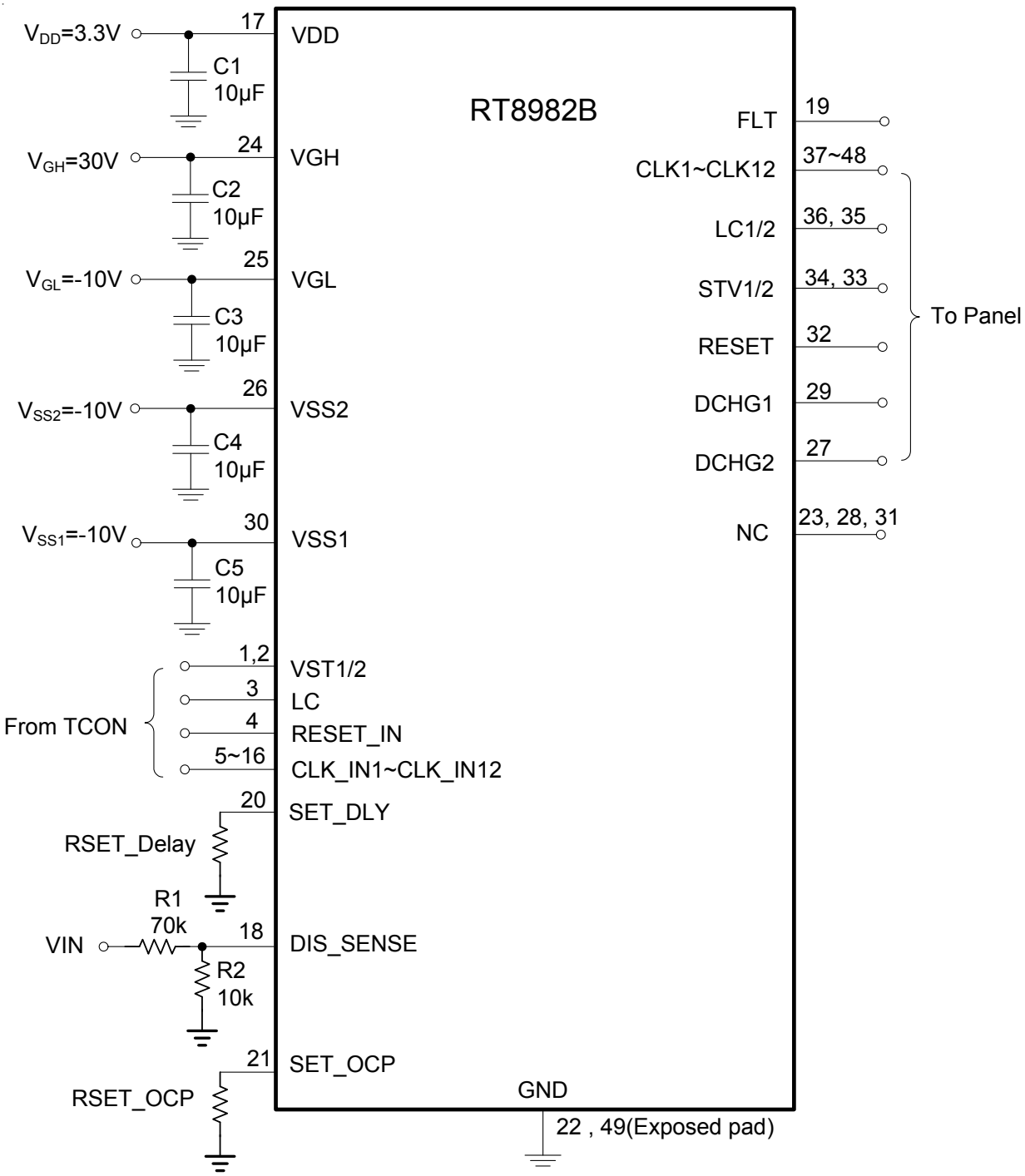
Pin Configuration

(TOP VIEW)

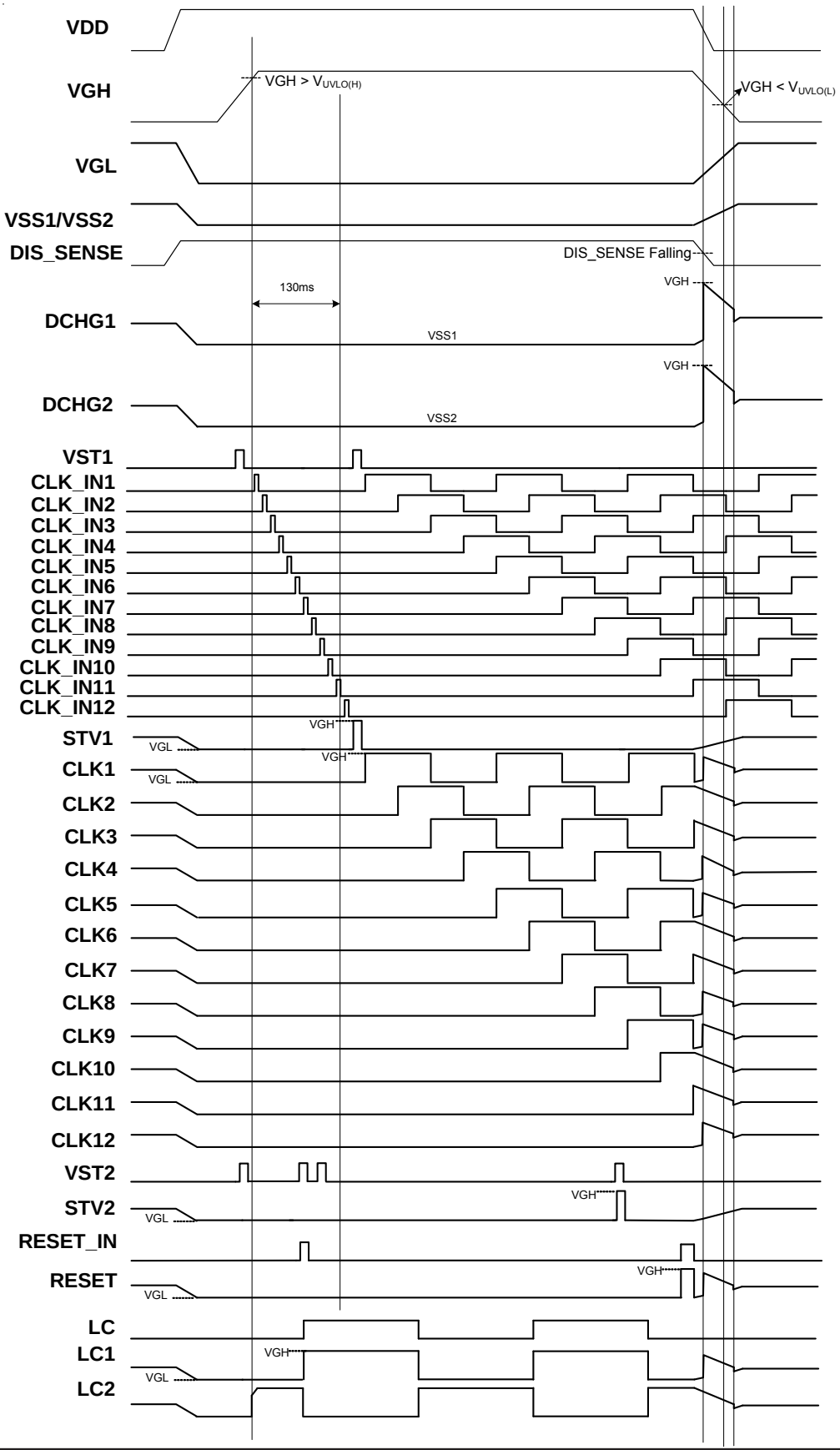


VQFN-48L 6x6

Typical Application Circuit



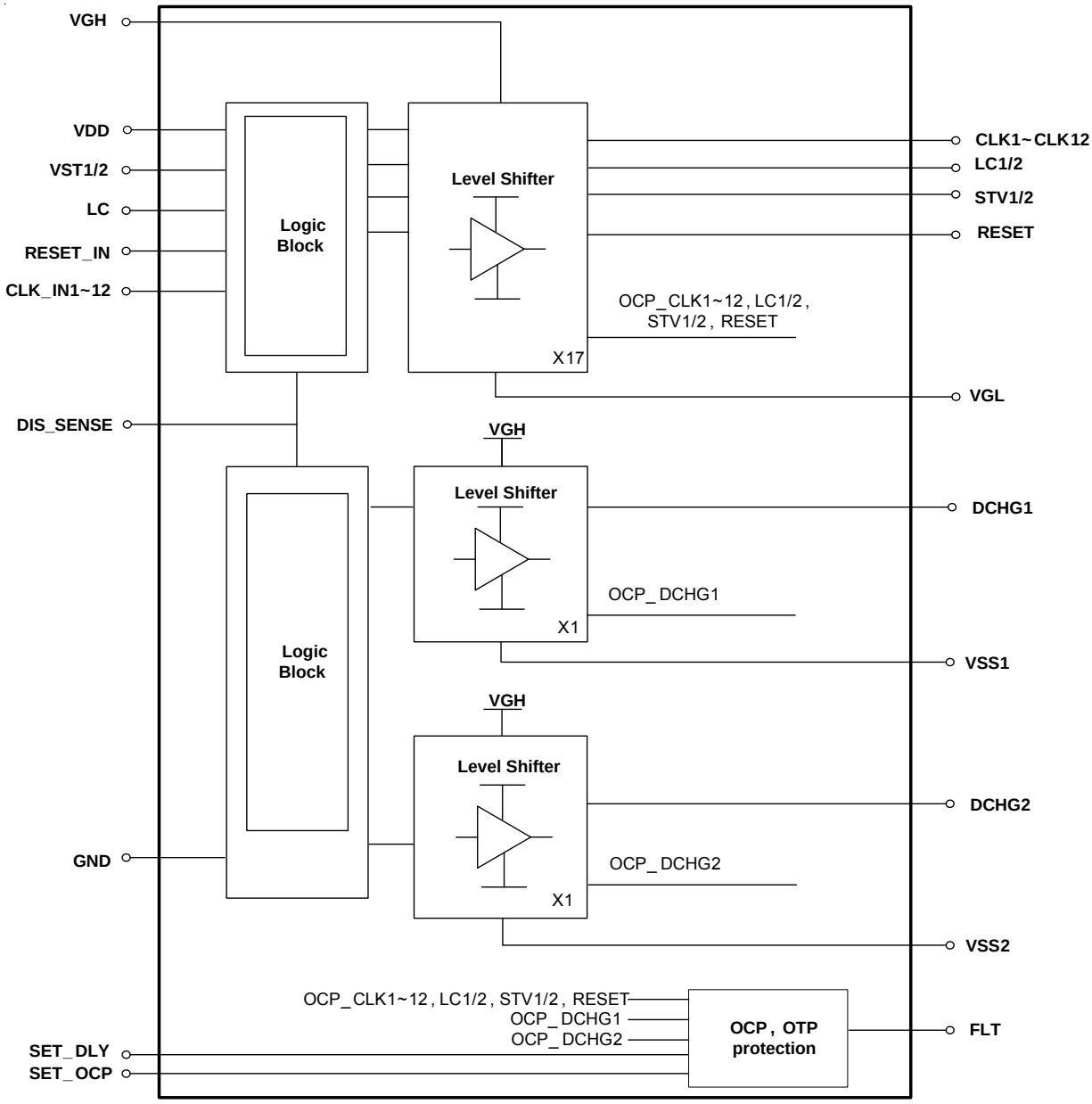
Timing Diagram



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VST1	Level shifter input for STV1.
2	VST2	Level shifter input for STV2.
3	LC	Level shifter input for LC1 and LC2.
4	RESET_IN	Level shifter input for RESET.
5 to 16	CLK_IN1 to CLK_IN12	Level shifter input for CLK1 to CLK12.
17	VDD	Supply voltage input.
18	DIS_SENSE	Voltage sense input for level shifter discharge function.
19	FLT	Fault output pin, logic low at normal operation. When OCP or OTP happen, this pin is pulled to VDD.
20	SET_DLY	OCP delay time programming pin. Connect a resistor to GND for OCP delay setting.
21	SET_OCP	OCP level programming pin. Connect a resistor to GND for OCP level setting.
22	GND	Ground.
23, 28, 31	NC	No use pin.
24	VGH	Positive power supply pin for all level shifter output.
25	VGL	Negative power supply pin for CLK1 to CLK12, LC1/2, STV1/2, RESET output.
26	VSS2	Negative power supply pin for DCHG2 output.
27	DCHG2	Level shifter output for discharge function.
29	DCHG1	Level shifter output for discharge function
30	VSS1	Negative power supply pin for DCHG1 output.
32	RESET	Level shifter output signal.
33	STV2	Level shifter output signal.
34	STV1	Level shifter output signal.
35	LC2	Level shifter output signal (Low frequency clock) out-of-phase with LC.
36	LC1	Level shifter output signal (Low frequency clock) in-phase with LC.
37 to 48	CLK1 to CLK12	Level shifter output signal.
48 (Exposed Pad)	GND	Ground. The Exposed Pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.

Functional Block Diagram



Operation

The RT8982B is a 19-Channel high-voltage level-shifter application such as TVs.

The device converts logic level signals generated by the Timing Controller (T-con) to high level signals used for the display panel.

When DIS_SENSE should be larger than 1.35V, where DIS_SENSE is the voltage divided from VIN or VDD, the outputs of level shifter STV1, STV2, CLK1 to CLK12, RESET, LC1 and LC2 will follow VGL, DCHG1 will follow VSS1, DCHG2 will follow VSS2.

The DIS_SENSE allows designer to implement panel discharging during power off.

Once DIS_SENSE falls below 1.25V, the outputs of level shifter CLK1 to CLK12, RESET, LC1 and LC2 will pull to VGH, then STV1 and STV2 will keep their initial state.

Absolute Maximum Ratings (Note 1)

- (CLK_IN1 to CLK_IN12), VST1, VST2, LC, RESET_IN, FLT, SET_DLY, SET_OCP, VDD, DIS_SENSE to GND ---------- –0.3 to 6V
- VGH to GND ---------- –0.3 to 45V
- VGH to VGL, VSS1, VSS2 ---------- –0.3 to 65V
- VGL, VSS1, VSS2 to GND ---------- –3 to –22V
- VGL to VSS1, VSS2 ---------- –0.3V
- (CLK1 to CLK12), STV1, STV2, LC1, LC2, RESET, DCHG1, DCHG2 to GND ---------- (–0.3 + VGL) to VGH
- Power Dissipation, P_D @ T_A = 25°C
  VQFN-48L 6x6 ---------- 2.94W
- Package Thermal Resistance (Note 2)
  VQFN-48L 6x6, θ_{JA} ---------- 34°C/W
  VQFN-48L 6x6, θ_{JC} ---------- 5.8°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{GH} = 30V, V_{DD} = 3.3V, VGL, VSS1, VSS2 = –10V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Voltage Level Shift						
VGH Input Voltage Range	V_{GH}		8	--	40	V
VGL, VSS1, VSS2 Input Voltage Range	V_{GL}		–20	--	–2	V
VGH to VGL Voltage Range	V_{GH_VGL}		--	--	60	V
VDD Supply Voltage			2.6	--	5.5	V
VDD UVLO	VDD_{UVLOR}	VDD rising	2	2.2	2.4	V
	VDD_{UVLOF}	VDD falling	1.8	2	2.2	V
VGH Under-Voltage Lockout Threshold	VGH_{UVLOR}	VGH rising	6.3	7	7.7	V
VGH Under-Voltage Lockout Hysteresis	VGH_{UVLOHY}		--	200	--	mV
Maximum Operating Frequency on Input Signal			--	--	200	kHz
Input Minimum Pulse Width	t_{INPUT}		100	--	--	ns
Maximum Output Frequency			--	--	200	kHz

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	Logic-Low	V_{IL}		--	--	0.6	V
	Logic-High	V_{IH}		1.4	--	--	V
Input pull low resistance		I_{IL}		250	400	550	kΩ
VGH Quiescent Current		I_{VGH}	No load, all channels pull to VGL	0.5	2.75	5	mA
VGL Quiescent Current		I_{VGL}	No load, all channels pull to VGL	50	250	350	μA
VSS1 Quiescent Current		I_{VSS1}	No load, DCHG1 pull to VSS1	5	55	90	μA
VSS2 Quiescent Current		I_{VSS2}	No load, DCHG2 pull to VSS2	5	55	90	μA
Thermal Shutdown Temperature		TH(SD)	Hys.= 20°C	--	150	--	°C
FLT Internal Pull Low Resistor		R_{FLT}		50	200	400	kΩ
FLT_MOS ON Resistor		R_{FLT_ON}		10	50	90	Ω
Discharge Threshold Voltage			DIS_SENSE falling	1.15	1.25	1.55	V
Discharge Threshold Voltage Hysteresis			DIS_SENSE rising	--	0.1	--	V
CLK1 to 12, STV1, STV2, LC1, LC2, RESET, DCHG1, DCHG2 On-Resistance (P-MOSFET)		$R_{DS(ON)\_P}$	I_{LOAD} = 10mA	--	12	30	Ω
CLK1 to 12, STV1, STV2, LC1, LC2, RESET, DCHG1, DCHG2 On-Resistance (N-MOSFET)		$R_{DS(ON)\_N}$	I_{LOAD} = 10mA	--	8	30	Ω
Propagation Rising Delay (CLK1 to 12, STV1, STV2, LC1, LC2, RESET, DCHG1, DCHG2)		t_{DR1}	R_{LOAD_SERIES} = 51Ω, C_{LOAD} = 4.7nF	--	100	200	ns
Propagation Falling Delay (CLK1 to 12, STV1, STV2, LC1, LC2, RESET, DCHG1, DCHG2)		t_{DF1}	R_{LOAD_SERIES} = 51Ω, C_{LOAD} = 4.7nF	--	100	200	ns
Rising Time (CLK1 to 12, STV1, STV2, LC1, LC2, RESET, DCHG1, DCHG2)		t_{R1}	C_{LOAD} = 3.3nF, 20% to 80%	--	--	700	ns
Falling Time (CLK1 to 12, STV1, STV2, LC1, LC2, RESET, DCHG1, DCHG2)		t_{F1}	C_{LOAD} = 3.3nF, 20% to 80%	--	--	700	ns
CLK1 to 12, STV1, STV2, LC1, LC2, RESET, DCHG1, DCHG2 OCP Level error (P-MOSFET)		I_{OCP_P}	OCP setting = 20mA to 100mA	−10	--	10	mA
			OCP setting = 100mA to 150mA	−10	--	10	%
			OCP setting = 150mA to 200mA	−15	--	15	%
CLK1 to 12, STV1, STV2, LC1, LC2, RESET, DCHG1, DCHG2 OCP Level error (N-MOSFET)		I_{OCP_N}	OCP setting = 20mA to 100mA	−10	--	10	mA
			OCP setting = 100mA to 150mA	−10	--	10	%
			OCP setting = 150mA to 200mA	−15	--	15	%

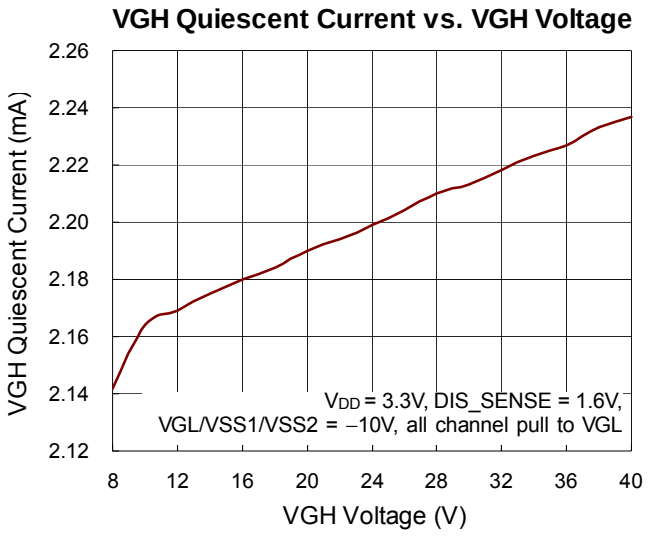
Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

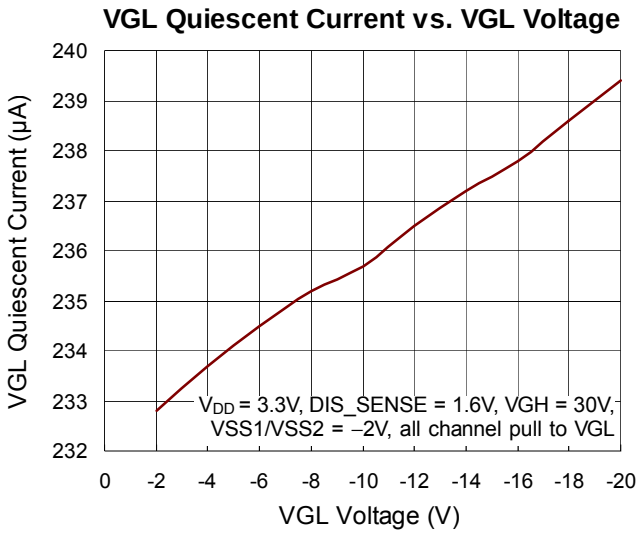
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

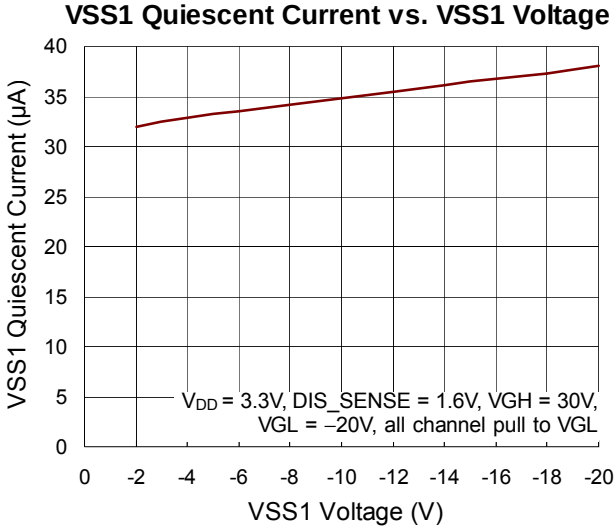
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

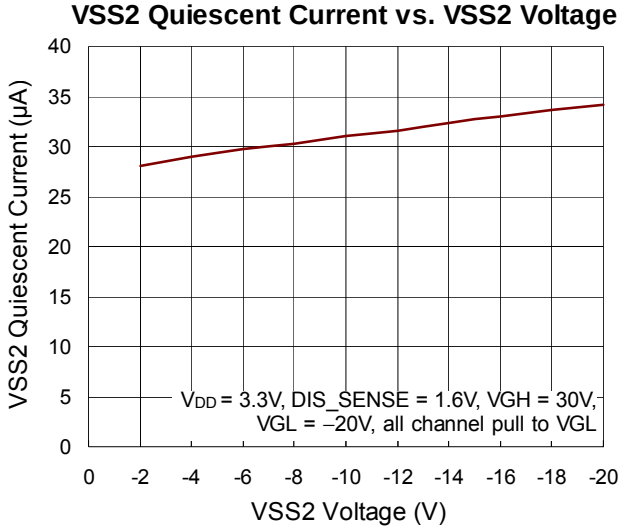
Note 4. The device is not guaranteed to function outside its operating conditions.

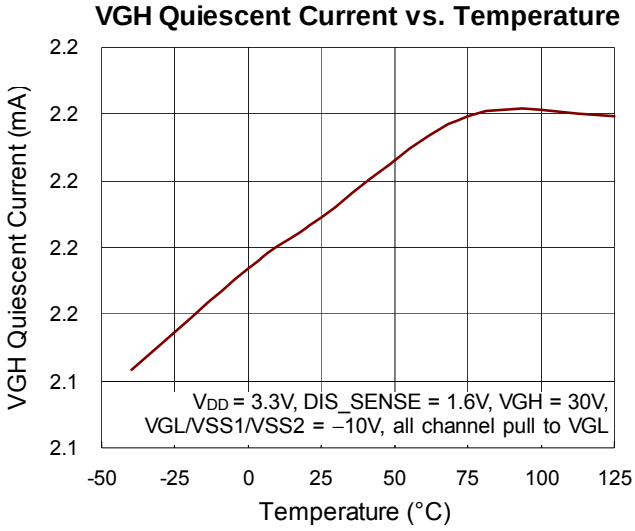
Typical Operating Characteristics

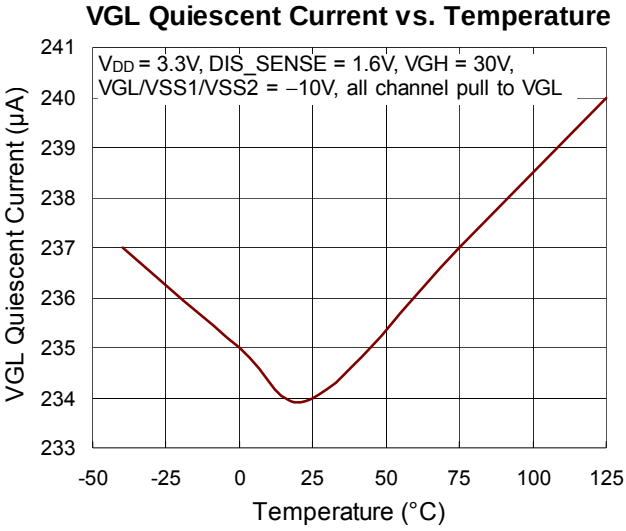




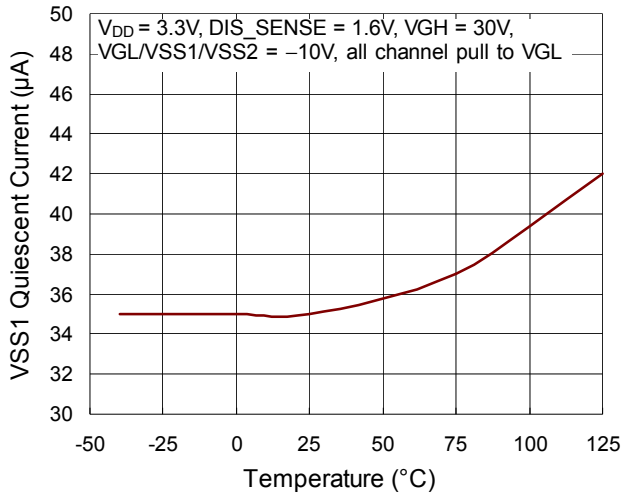




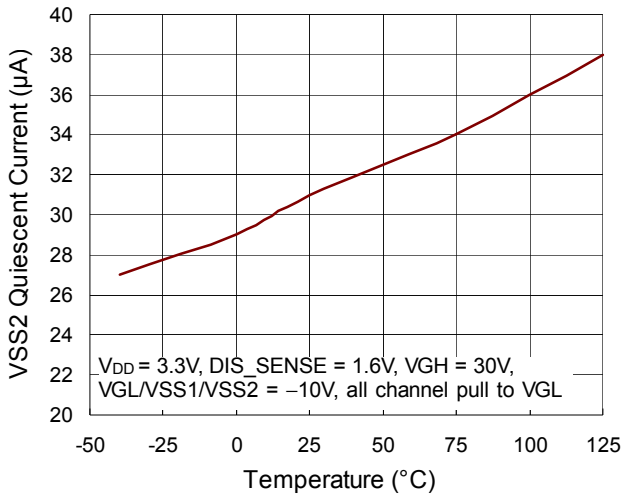




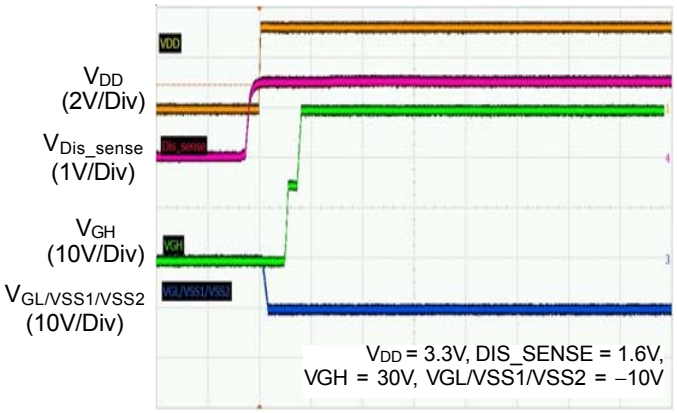
VSS1 Quiescent Current vs. Temperature



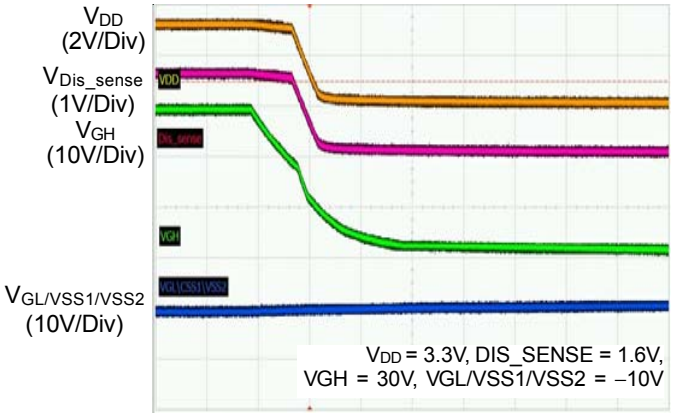
VSS2 Quiescent Current vs. Temperature



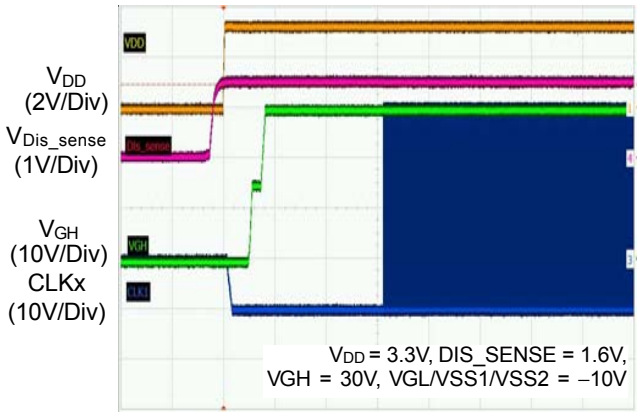
Power On



Power Off



Power On



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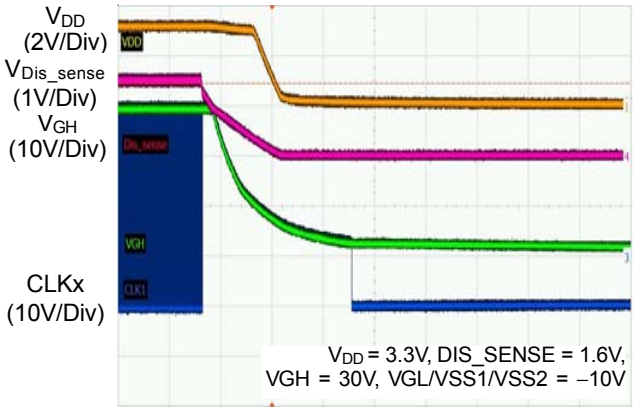
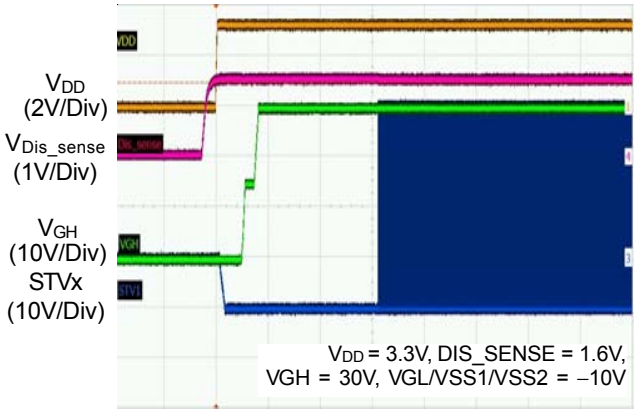


Power On



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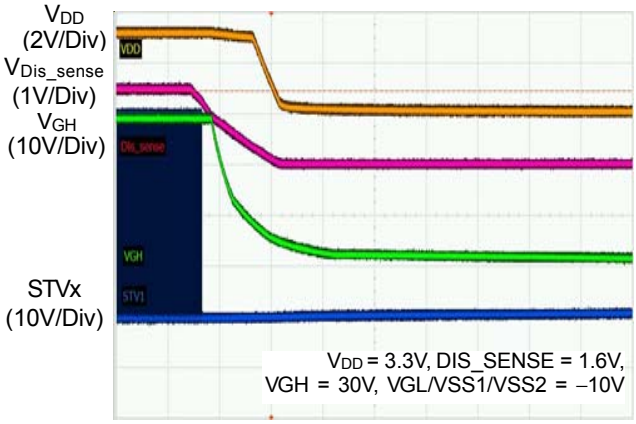

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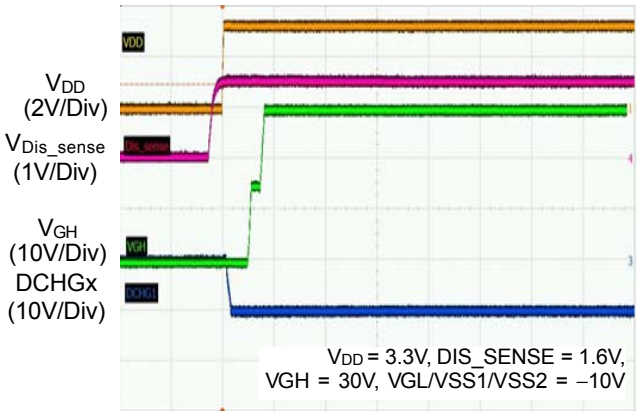

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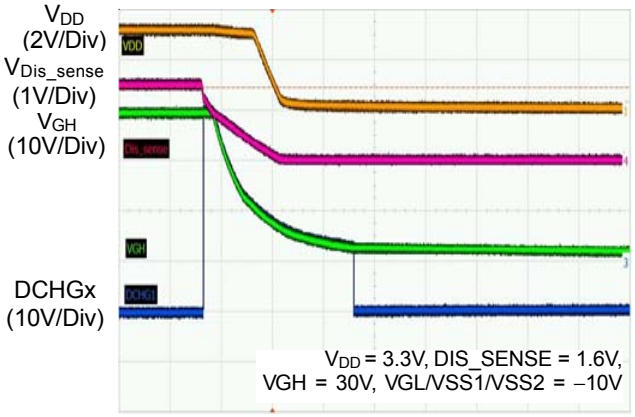
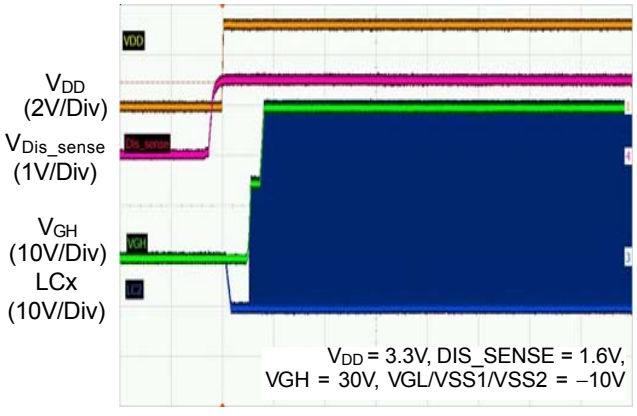
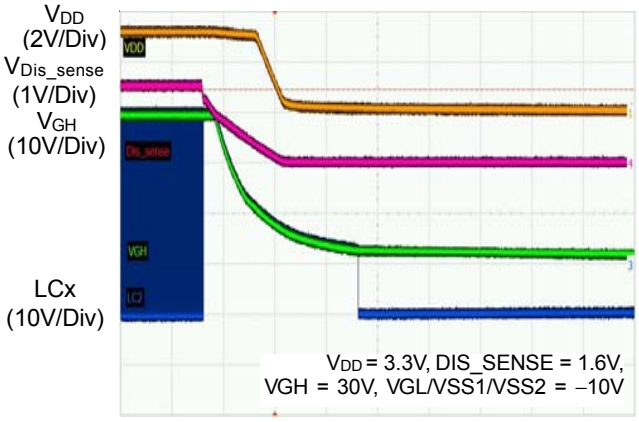


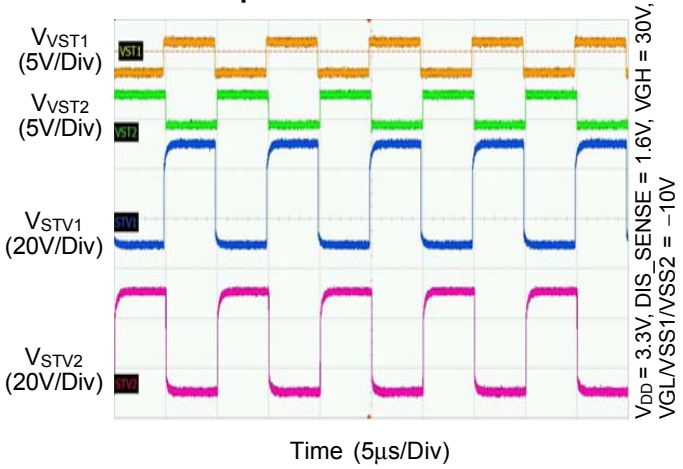
Power On



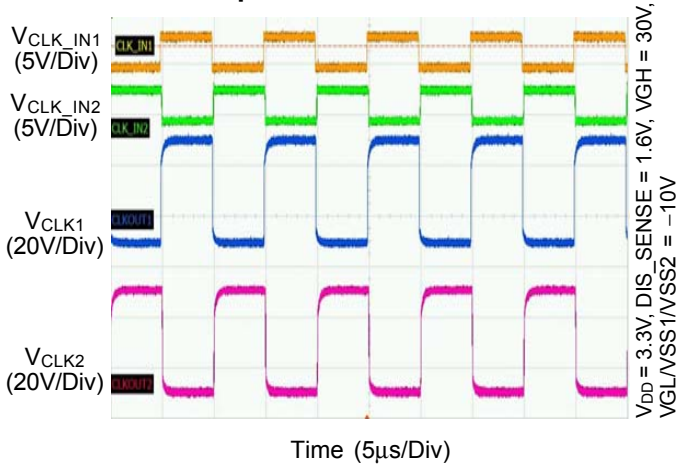
Power Off



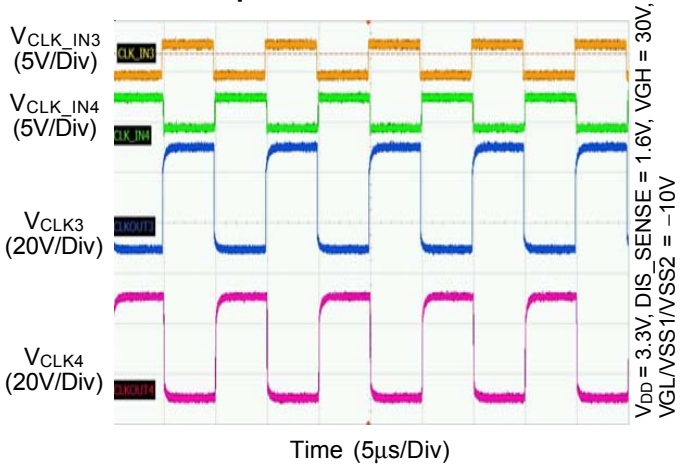
LS Operation-STV1 and STV2



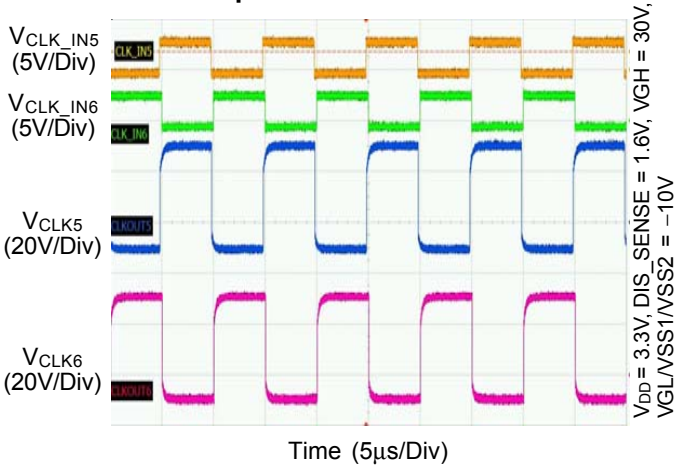
LS Operation-CLK1 and CLK2



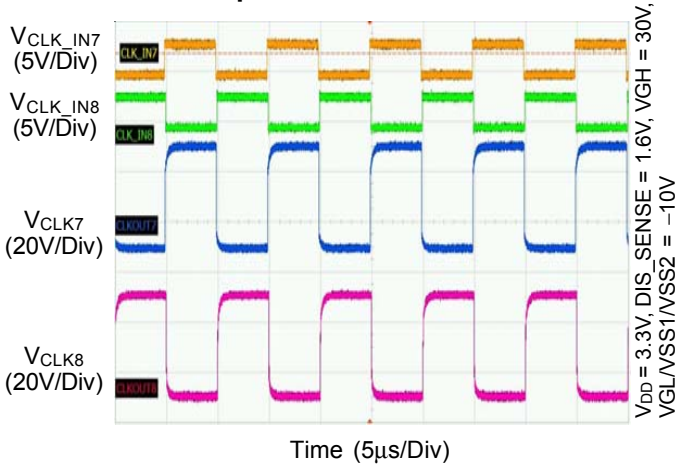
LS Operation-CLK3 and CLK4



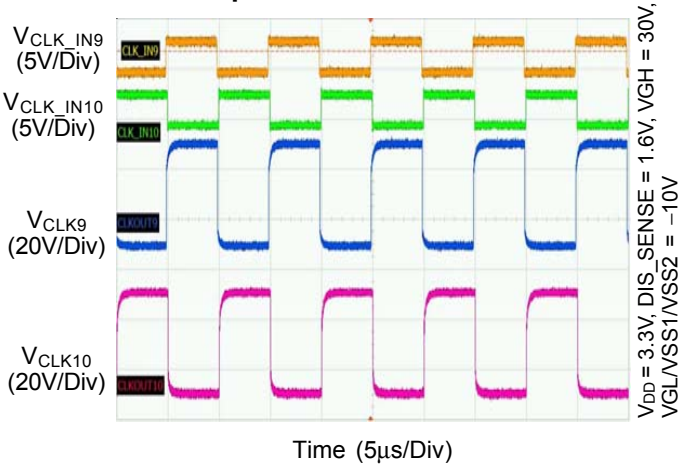
LS Operation-CLK5 and CLK6



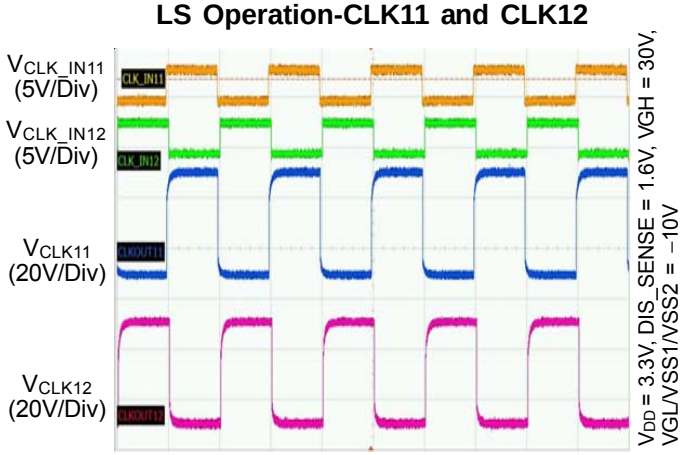
LS Operation-CLK7 and CLK8



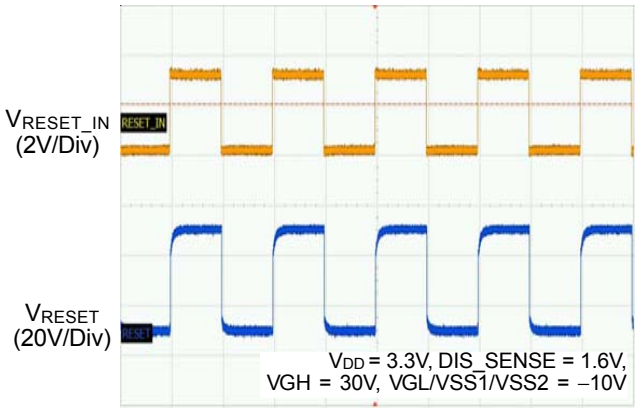
LS Operation-CLK9 and CLK10



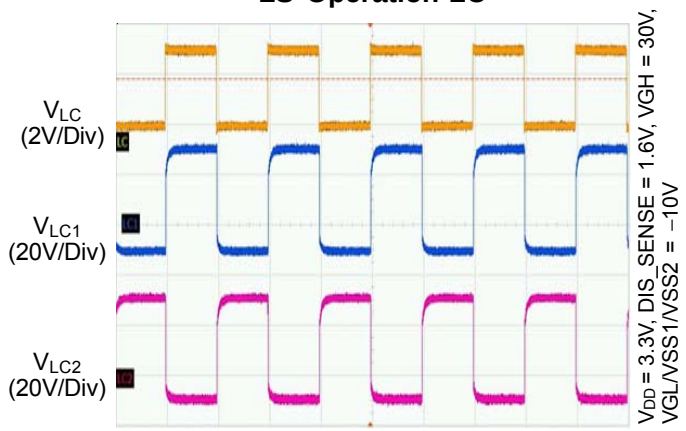
LS Operation-CLK11 and CLK12



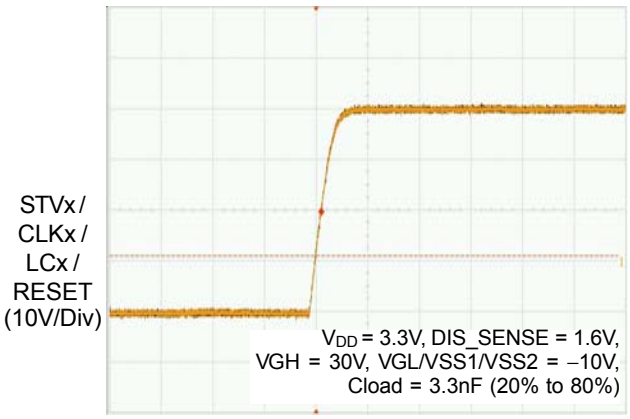
LS Operation-RESET



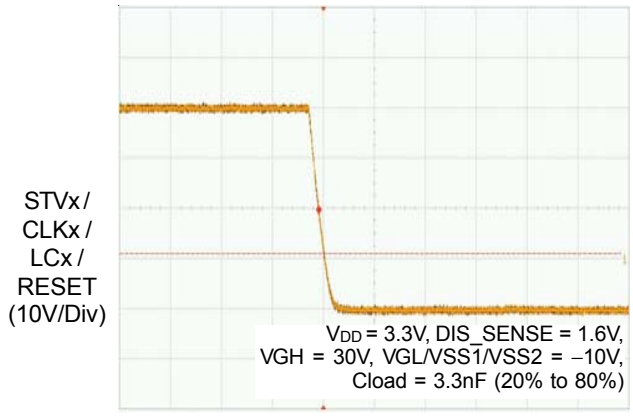
LS Operation-LC



STVx/CLKx/LCx/RESET/DCHGx Rising Time



STVx/CLKx/LCx /RESET/DCHGx Falling Time



Application Information

The RT8982B is a 19-channel high-voltage level-shifter application such as TVs.

The device converts logic level signals generated by the Timing Controller (T-con) to high level signals used for the display panel.

Power ON

When VDD, VGH and DIS_SENSE voltages are higher than UVLO, LC will be work, and then IC will start counting blanking time 130ms.

After 130ms, STV1, STV2, RESET and CLK1 to CLK12 will wait for receiving the first VST1 rising edge.

Before first VST1 rising edge, STV1, STV2, RESET and CLK1 to CLK12 will keep initial state.

Power OFF

Once DIS_SENSE falls below 1.25V, the outputs of level shifter CLK1 to CLK12, RESET, LC1 and LC2 will pull to VGH.

After VGH voltage falls below around 3V, the outputs return to their initial state.

Panel Discharge Detection

The panel discharge detection is for detecting the input voltage of primary power manager. It usually uses the resistor divider, then connect the voltage of resistor divider to the DIS_SENSE pin. The panel discharge detection threshold (DIS_SENSE) is 1.25V (typ.) if the DIS_SENSE is lower than 1.25V (typ.), the outputs of level shifter CLK1 to CLK12, RESET, LC1 and LC2 will pull to VGH, then STV1 and STV2 will keep their initial state.

Once the DIS_SENSE is higher than 1.35V (typ.), all output signals will resume operation.

Over-Temperature Protection (OTP)

Over-Temperature Protection prevents the RT8982B from overheating due to excessive power dissipation. When the junction temperature exceeds 150°C, the OTP will be triggered to shut down all outputs.

Power On Table

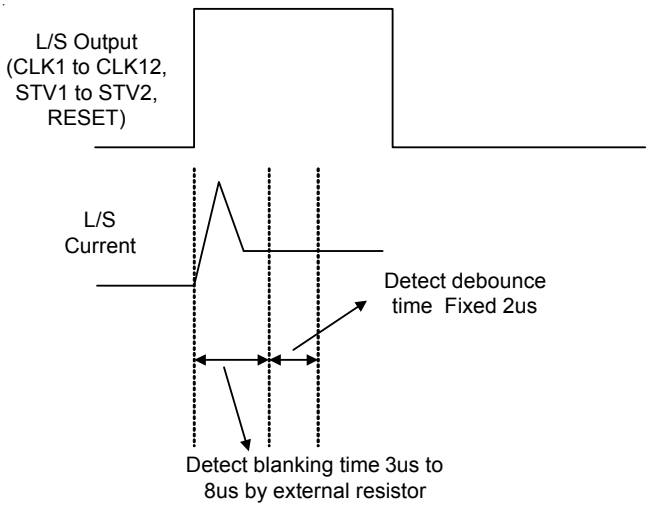
Case	Analog Input Power/Condition					Level Shifter Input					Level Shifter Output							
	VDD	DIS_SENSE	VGH	Blanking 130ms	1st VST1 rising edge after 130ms blanking	VST1	VST2	CLK_INx	RESET_IN	LC	STV1	STV2	CLKx	RESET	LC1	LC2	DCHG1	DCHG2
1	<UVLO	<UVLO	<UVLO	0	0	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	VGL	VGL	VGL	VGL	VGL	VGL	VSS1	VSS2
2	>UVLO	<UVLO	<UVLO	0	0	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	VGL	VGL	VGL	VGL	VGL	VGL	VSS1	VSS2
3	>UVLO	>UVLO	<UVLO	0	0	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	VGL	VGL	VGL	VGL	VGL	VGL	VSS1	VSS2
4	>UVLO	>UVLO	>UVLO	0	0	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i signal	VGL	VGL	VGL	VGL	Normal operation	Normal operation (Reverse)	VSS1	VSS2
5	>UVLO	>UVLO	>UVLO	1	0	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i signal	VGL	VGL	VGL	VGL	Normal operation	Normal operation (Reverse)	VSS1	VSS2
6	>UVLO	>UVLO	>UVLO	1	1	w/i signal	w/i signal	w/i signal	w/i signal	w/i signal	Normal operation	Normal operation	Normal operation	Normal operation	Normal operation	Normal operation (Reverse)	VSS1	VSS2
7	<UVLO	>UVLO	>UVLO	0	0	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	VGL	VGL	VGL	VGL	VGL	VGL	VSS1	VSS2
8	>UVLO	<UVLO	>UVLO	0	0	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	VGH	VGH	VGH	VGH	VGH	VGH	VGH	VGH

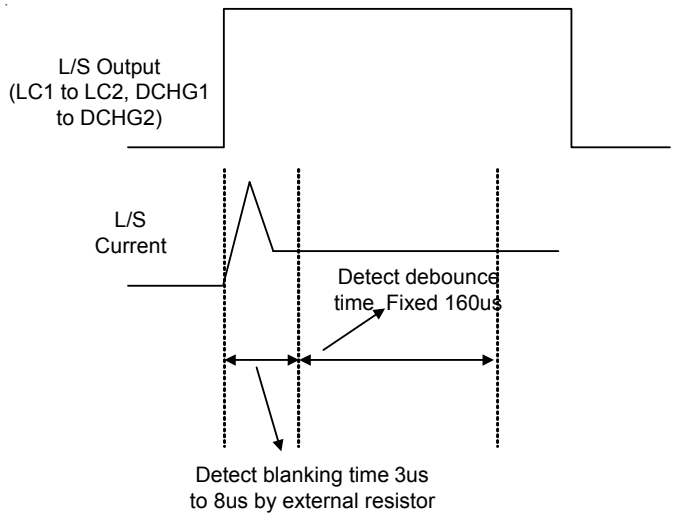
Power Off Table

Case	Analog Input Power/Condition					Level Shifter Input					Level Shifter Output							
	VDD	DIS_SENSE	VGH	Blanking 130ms	1st VST1 rising edge after 130ms blanking	VST1	VST2	CLK_INx	RESET_IN	LC	STV1	STV2	CLKx	RESET	LC1	LC2	DCHG1	DCHG2
1	>UVLO	>UVLO	>UVLO	1	1	w/i signal	w/i signal	w/i signal	w/i signal	w/i signal	Normal operation	Normal operation	Normal operation	Normal operation	Normal operation	Normal operation (Reverse)	VSS1	VSS2
2	<UVLO	>UVLO	>UVLO	0	0	w/i signal	w/i signal	w/i signal	w/i signal	w/i signal	Normal operation	Normal operation	Normal operation	Normal operation	Normal operation	Normal operation (Reverse)	VSS1	VSS2
3	<UVLO	<UVLO	>UVLO	0	0	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	VGL	VGL	VGH	VGH	VGH	VGH	VGH	VGH
4	<UVLO	<UVLO	<UVLO	0	0	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	w/i or w/o signal	VGL	VGL	VGH	VGH	VGH	VGH	VGH	VGH

OCP Setting

Level Shifter Output	Blanking 130ms	Blanking time	Deglitch time	OCP Cycle
CLK1~CLK12	V	3us~8us	2us	4 times
STV1	V	3us~8us	2us	1 time
STV2	V	3us~8us	2us	1 time
RESET	V	3us~8us	2us	1 time
LC1	X	3us~8us	160us	1 time
LC2	X	3us~8us	160us	1 time
DCHG1	V	3us~8us	160us	1 time
DCHG2	V	3us~8us	160us	1 time





Setting OCP Table

OCP Level Setting			
RSET_OCP (kΩ)	**OCP Threshold (mA)**	**RSET_OCP (kΩ)**	**OCP Threshold (mA)**
200	20	34.78	115
160	25	33.33	120
133.3	30	32	125
114.29	35	30.77	130
100	40	29.63	135
88.89	45	28.57	140
80	50	27.59	145
72.73	55	26.67	150
66.67	60	25.81	155
61.54	65	25	160
57.14	70	24.24	165
53.33	75	23.53	170
50	80	22.86	175
47.06	85	22.22	180
44.44	90	21.62	185
42.11	95	21.05	190
40	100	20.51	195
38.19	105	20	200
36.36	110		

I_{OCP} (mA) = 4000/RSET_OCP (kΩ)
When SET_OCP pin is floating, OCP function is disable

OCP Delay Time Setting	
RSET_Delay (kΩ)	**OCP Delay Time (μs)**
24.4	3
28	3.5
31.6	4
35.2	4.5
38.8	5
42.4	5.5
46	6
49.6	6.5
53.2	7
56.8	7.5
60.4	8

t_{DELAY} = 0.1388 x RSET_Delay (kΩ) – 0.388
Error = ±15%

CLK1 to CLK12

When over-current has continued for 4 times in one of CLK1 to CLK12 channels P-MOSFET or N-MOSFET, FLT will be pulled high and all 19-Channels output will become high impedance.

DCHG1/2, RESET, STV1/2, LC1/2 :

As long as over-current occurs one time in one of these 7-Channels P-MOSFET or N-MOSFET, FTT will be pulled high and all 19-Channels output will become high impedance.

Protection Function

CLK1 to CLK12, STV1, STV2, LC1, LC2, DCHG1, DCHG2, RESET OCP level could be set by SET_OCP pin.

Function / Protection	Output	FLT	Removal
OTP	Hi-Z	Pull high to VDD	IC re-start
OCP	Hi-Z	Pull high to VDD	IC re-start

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a VQFN-48L 6x6, the thermal resistance, θ_{JA}, is 34°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (34°C/W) = 2.94W for a VQFN-48L 6x6 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

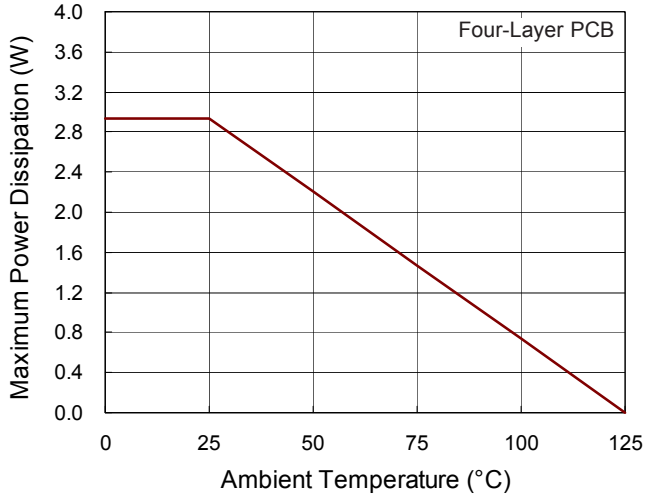


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Consideration

For the best performance of the RT8982B. The following descriptions are the guidelines for better PCB layout:

- Place the power components as close as possible. The traces should be wide and short especially for the high current loop.
- The exposed pad of the chip should be connected to a large negative voltage plane for thermal consideration.

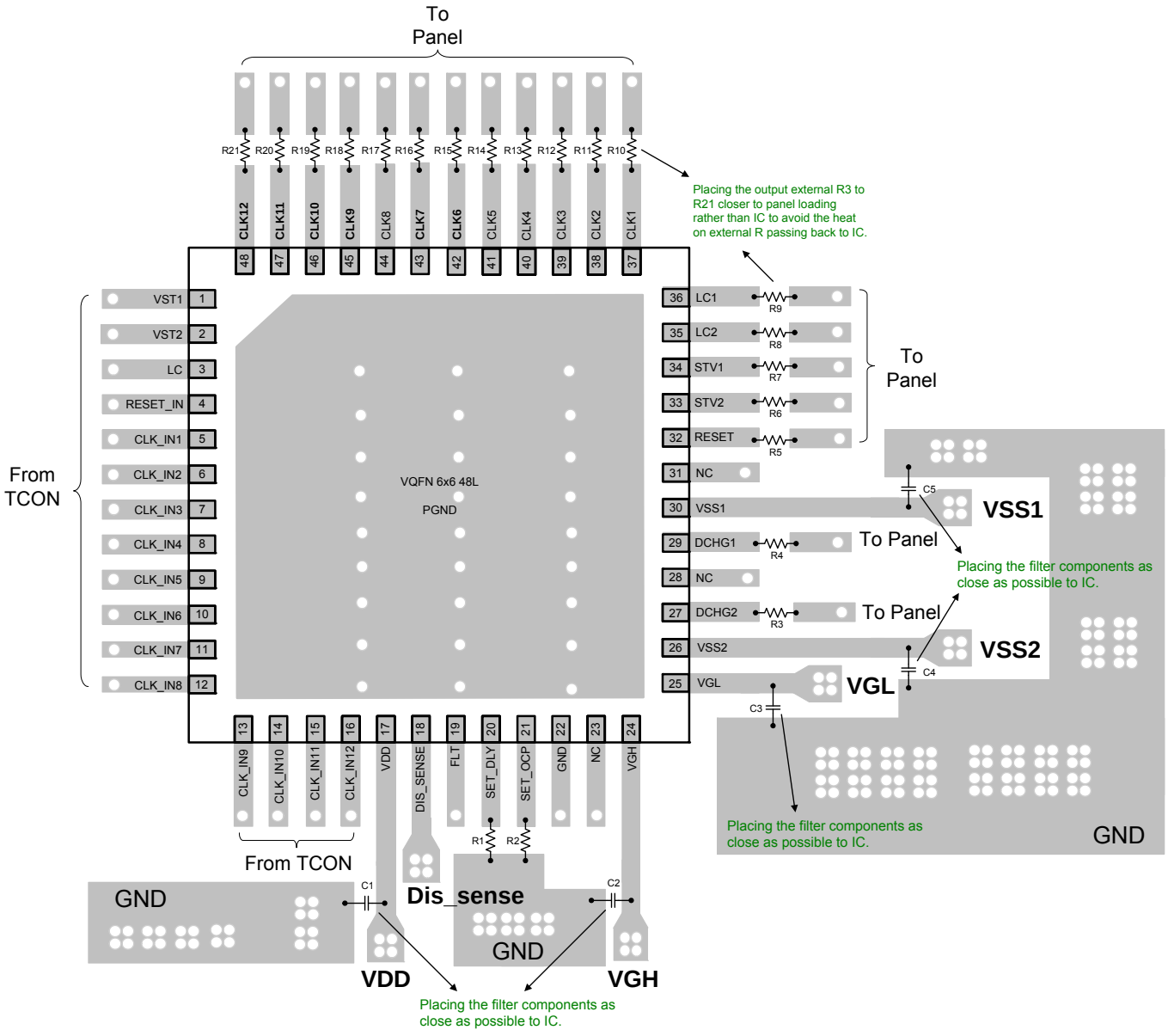
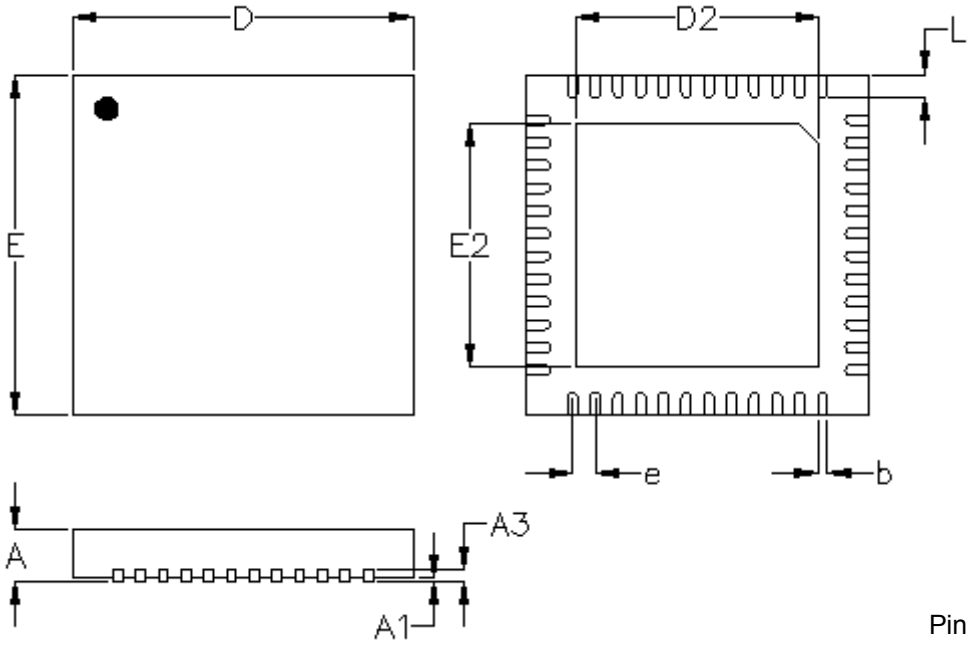
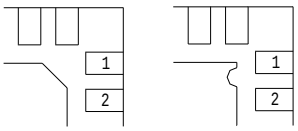


Figure 2. Layout Guide

Outline Dimension





DETAIL A

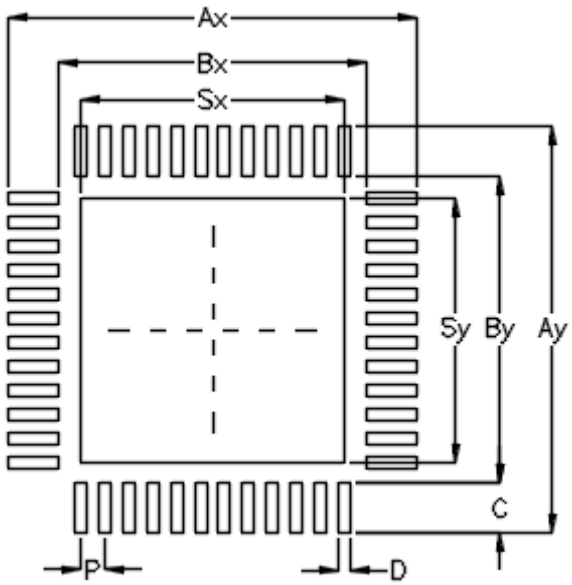
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	5.950	6.050	0.234	0.238
D2	4.250	4.350	0.167	0.171
E	5.950	6.050	0.234	0.238
E2	4.250	4.350	0.167	0.171
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

V-Type 48L QFN 6x6 Package

Footprint Information



Package		Number of Pin	Footprint Dimension (mm)									Tolerance
			P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN6*6-48	Option1	48	0.40	6.80	6.80	5.10	5.10	0.85	0.20	4.40	4.40	±0.05
	Option2									4.50	4.50	

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Datasheet Revision History

Version	Date	Item	Description
P00	2017/11/10		First Edition
P01	2018/5/4	Timing Diagram Operation Absolute Maximum Ratings Electrical Characteristics Typical Operating Characteristics Application Information	Modify