Application Note: SY7630C

High Efficiency Power Management IC for TFT LCD

General Description

The SY7630C is a power management IC with one boost regulator, two charge pumps, one gate pulse modulator, one OPAMP, and one open drain reset output for TFT LCD power. The SY7630C operates over a wide input voltage range from 2.3V to 5.5V to optimize the device for 5V, 3.3V applications.

Ordering Information

SY7630 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY7630CQCC	QFN4x4-24	----

Features

- 2.3-5.5V input voltage range
- Current mode boost regulator:
  - Low $R_{DS(ON)}$ for Boost internal switches: 140mΩ / 3.5A
  - 1.2MHz switching frequency
- Positive charge pump for VGH
- Negative charge pump for VGL
- Integrated gate pulse modulator with adjustable delay.
- Integrated operational amplifier
- Open drain reset output
- Compact package: QFN4x4-24

Applications

- TFT LCD Panels

Typical Applications

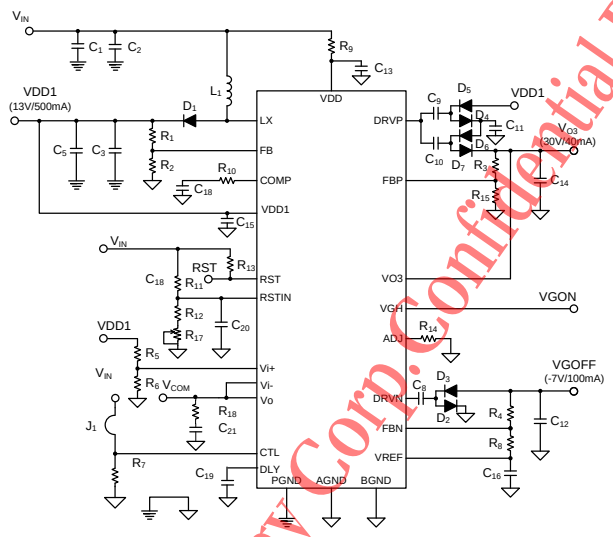


Figure 1.Schematic diagram

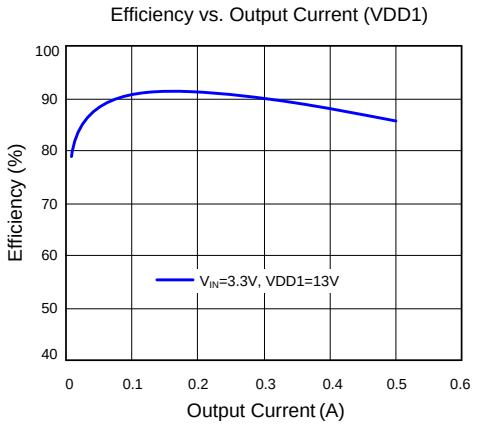
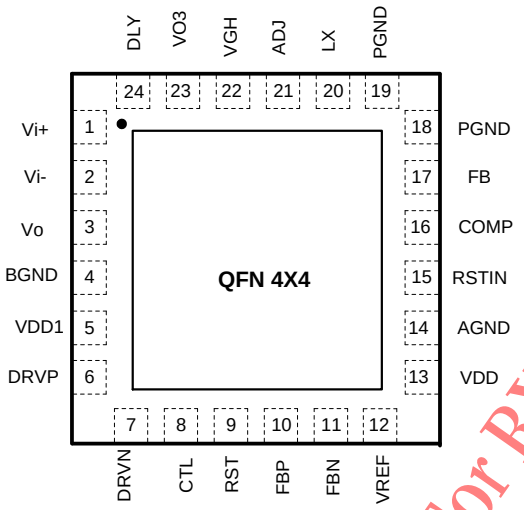


Figure 2. Boost Efficiency vs. Load Current

Pinout (top view)

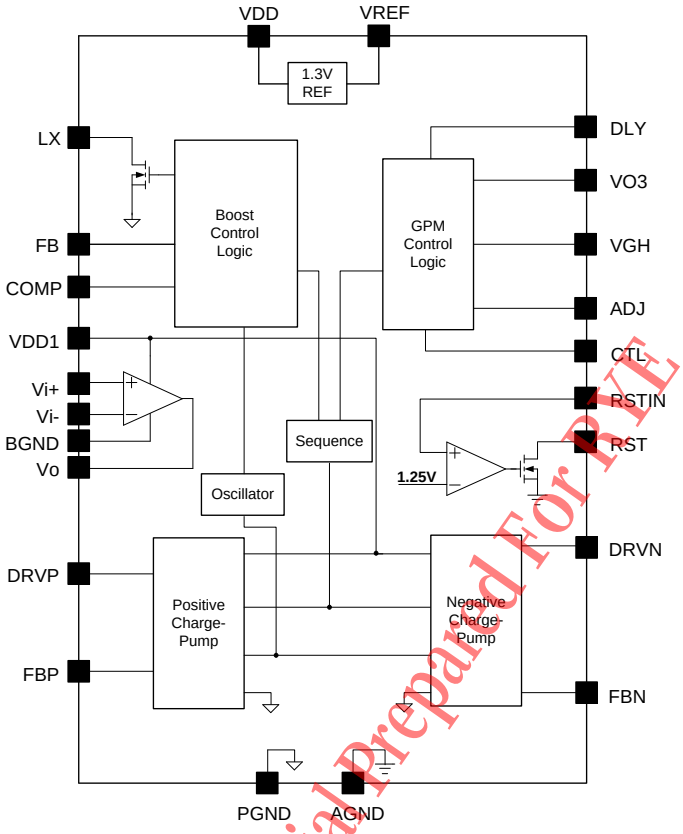


(QFN4x4-24)

Top Mark: CWT *xyz* (Device code: CWT, *x=year code, y=week code, z= lot number code*)

Pin Name	Pin Number	Pin Description
Vi+	1	VCOM buffer positive input pin
Vi-	2	VCOM buffer negative input pin
Vo	3	VCOM buffer output pin
BGND	4	Ground for VCOM buffer pin
VDD1	5	VCOM buffer and charge pump power supply pin
DRVP	6	Driver output of positive charge pump pin
DRVN	7	Driver output of negative charge pump pin
CTL	8	GPM (Gate Pulse Modulation) control pin
RST	9	Open drain reset output pin
FBP	10	Positive charge pump feedback pin
FBN	11	Negative charge pump feedback pin
VREF	12	Reference output pin
VDD	13	Supply voltage input pin
AGND	14	Analog ground pin
RSTIN	15	Reset input pin
COMP	16	Boost PWM compensation pin
FB	17	Boost PWM feedback pin
PGND	18	Power ground pin
PGND	19	Power ground pin
LX	20	Boost regulator switching node pin
ADJ	21	Pin to set the falling time of gate high voltage
VGH	22	Gate high output voltage for TFT pin
VO3	23	Gate High voltage input pin
DLY	24	VGH delay adjust pin

Block Diagram



Absolute Maximum Ratings (Note 1)

VDD ---------- 7V
CTL, RST, RSTIN---------- 7V
VDD1, LX---------- 22V
DRVP, DRVN, Vi+, Vi-, Vo---------- VDD1+0.3V
VO3---------- 36V
ADJ, VGH---------- VO3+0.3V
FBP, FBN, REF, COMP, FB, DLY---------- 4V
Power Dissipation, PD @ TA = 25℃ QFN4x4-24 ---------- 1.8W
Package Thermal Resistance (Note 2)
θJA ---------- 70℃/W
θJC ---------- 35℃/W
Junction Temperature Range ---------- 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃

Recommended Operating Conditions (Note 3)

VDD---------- 2.3V to 5.5V
VDD1 ---------- 0 to 18V
Ambient Temperature Range ---------- -40℃ to 85℃
Junction Temperature Range ---------- -40℃ to 125℃

Electrical Characteristics

(VDD =3.3V, VDD1=13V, TA = 25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Input Voltage Range	V_{DD}		2.3		5.5	V
VDD UVLO Threshold	V_{UVLO}	VDD Rising			2.3	V
VDD UVLO Hysteresis	V_{HYS}			0.14		V
Reference Voltage	V_{REF}		1.274	1.3	1.326	V
Reference Line Regulation		I_{VREF}=100μA,V_{DD}=2.5V~5.5V	-	1	5	mV/V
Reference Load Regulation		I_{VREF}=0~100μA,	-		1	%
Boost Regulator						
Feedback Voltage	V_{FB}		1.238	1.25	1.262	V
FB Input Current	I_{FB}		-40		40	nA
Output Voltage Range			V_{VDD}		18	V
Boost FET Current Limit	I_{LIM}		2.5	3.5		A
Boost FET On-Resistance	R_{ON1}			0.14		Ω
Oscillator Frequency	F_{OSC}		1.0	1.2	1.4	MHz
Charge Pump and Gate Pulse Modulator						
VDD1 Input Voltage Range	V_{H1}		6		18	V
Charge pump frequency	F_{OSC}		500	600	700	kHz
DLY Current	I_{DLY}			5		μA
DLY threshold	V_{DLY}			1.25		V
VO3-VGH resistance	R_H			20		Ω
VGH-ADJ resistance	R_L			32		Ω
CTL high voltage			2			V
CTL low voltage					0.6	V
DRVP/DRVN low side Switch R_{ON}	R_{ONP2}			5	10	Ω
DRVP/DRVN high side Switch R_{ON}	R_{ONP3}			3	6	Ω
FBP Feedback Voltage	V_{FBP}		1.22	1.25	1.28	V
FBN Feedback Voltage	V_{FBN}		270	300	330	mV
OPAMP						
Input Offset Voltage	V_{OS}	V_{i+}=5V			50	mV
Input Bias Current	I_{BS}	V_{i+}=5V	-1	0	1	μA
Output Voltage Swing High	V_{OH}	I_{OUT} = 5mA	V_{DD1}-200			mV
Output Voltage Swing Low	V_{OL}	I_{OUT} = -5mA			200	mV
Short-circuit current	I_{short}			200		mA
Slew Rate	SR	V_{i+}= 2V to 8V/ 8V to 2V 20% to 80%		40		V/μs
Reset Output						
RSTIN Threshold	V_{INR}		1.2	1.25	1.3	V
RST Output Voltage	V_{RST}	I_RST=1.2mA			0.2	V
RST Blank Time	$t_{BLK,RST}$	From VDD rises above UVLO		380		ms
Soft Start and Fault Detection						
Boost Soft Start Time	T_{SS1}			8		ms
VGL Soft Start Time	T_{SS2}			5		ms
VGH Soft Start Time	T_{SS3}			8		ms
Time out for fault protection	T_{FP}			130		ms
FB Fault Protection Voltage	V_{F1}		0.95	1.00	1.05	V
FBN Fault Protection Voltage	V_{F2}		0.40	0.50	0.60	V
FBP Fault Protection Voltage	V_{F3}		0.95	1.00	1.05	V

FB Under Voltage Protection	V_{F4}			0.1		V
Thermal Shutdown Temperature	T_{SD}			150		°C

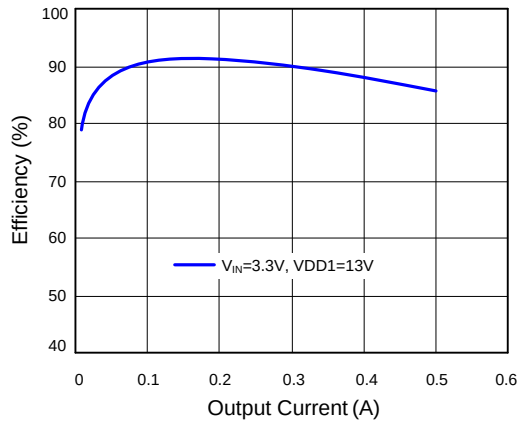
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θJA is measured in the natural convection at TA = 25℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

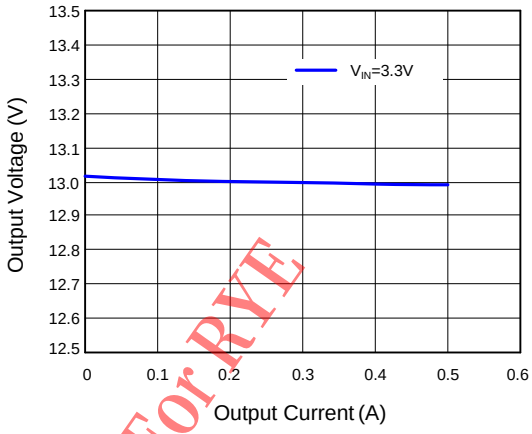
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

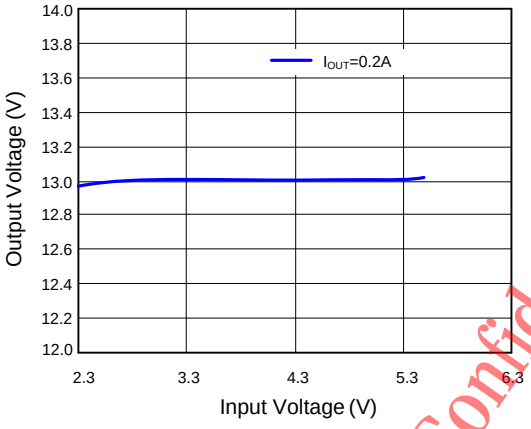
Efficiency vs. Output Current (VDD1)



Load Regulation (VDD1)

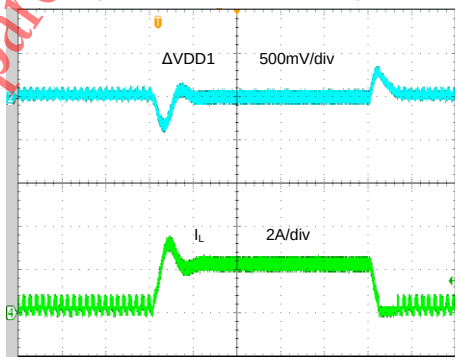


Line Regulation (VDD1)



VDD1 Load Transient

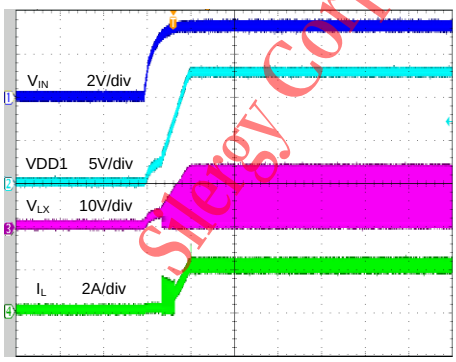
(V_{IN}=3.3V,VDD1=13V,I_{OUT}=0.05-0.5A)



Time (100μs/div)

VDD1 VIN ON

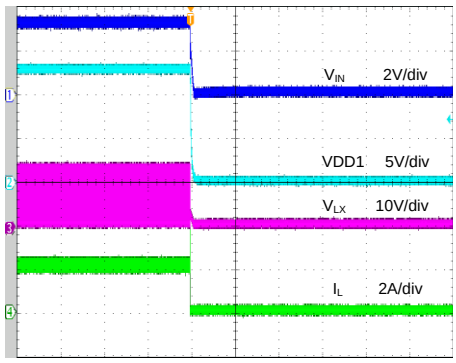
(V_{IN}=3.3V,VDD1=13V,I_{OUT}=0.5A)



Time (10ms/div)

VDD1 VIN Off

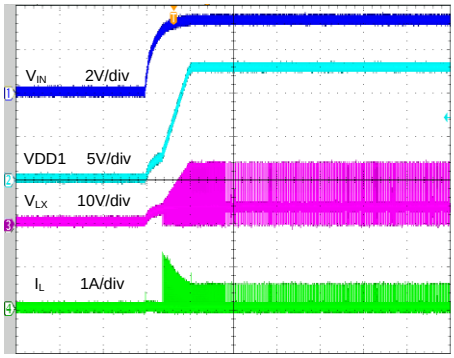
(V_{IN}=3.3V,VDD1=13V,I_{OUT}=0.5A)



Time (20ms/div)

VDD1 VIN ON

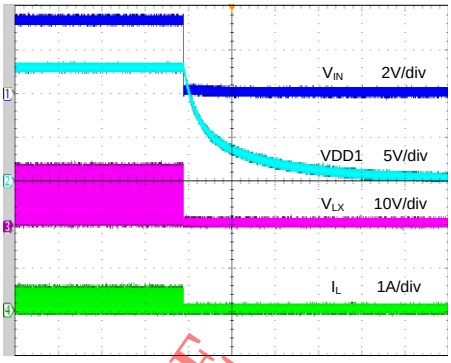
(V_{IN}=3.3V,VDD1=13V,I_{OUT}=0A)



Time (10ms/div)

VDD1 VIN Off

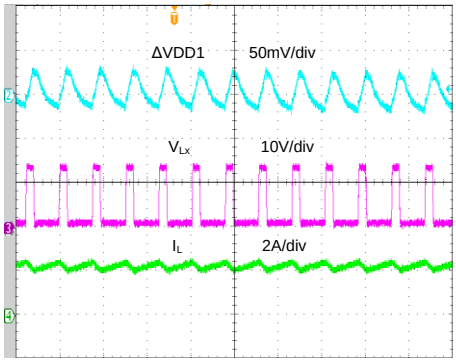
(V_{IN}=3.3V,VDD1=13V,I_{OUT}=0A)



Time (1s/div)

VDD1 Output Voltage Ripple

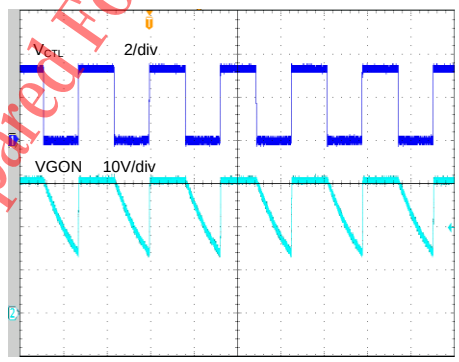
(V_{IN}=3.3V,VDD1=13V,I_{OUT}=0.5A)



Time (1μs/div)

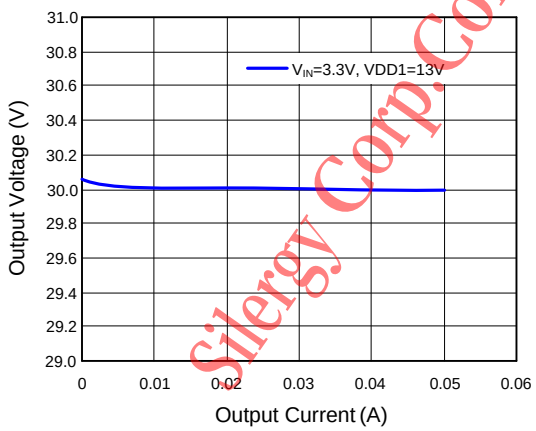
VGON Switch

(VO3=30V,C_{GON}=1nF,R_{ADJ}=10K)

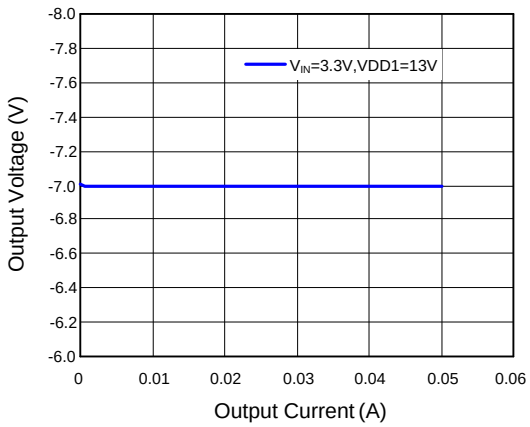


Time (10μs/div)

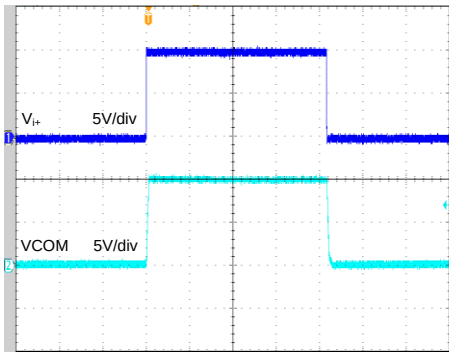
Load Regulation (VO3)



Load Regulation (VGOFF)

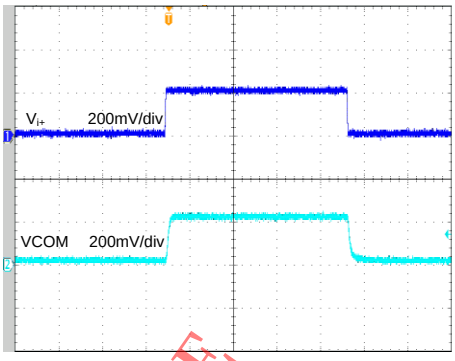


VCOM Large Signal Step Response



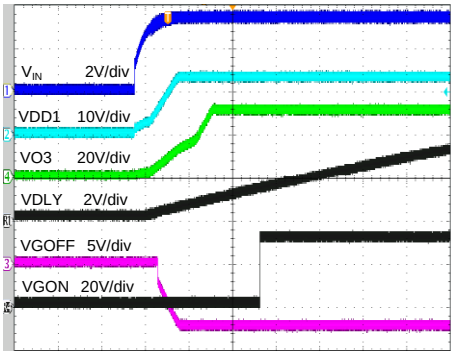
Time (4μs/div)

VCOM Small Signal Step Response



Time (1μs/div)

Power Up Sequence



Time (10ms/div)

Operation

SY7630C is a power management IC for TFT LCD bias supply. The device contains a Boost regulator to generate the source driver supply, and two charge-pump regulators to generate the gate driver supplies. Each regulator features adjustable output voltage and timer delayed fault protection. SY7630C also integrates a high performance OPAMP to drive the LCD backplane, and an open drain reset output.

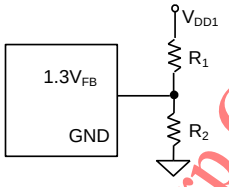
Boost Regulator

SY7630C adopts constant frequency peak current mode control to ensure reliable over current protection and cycle by cycle switch current limit. With 1.2MHz switching frequency, it allows choosing small size ceramic capacitors and inductors to adapt LCD panel design.

Feedback resistor dividers R1 and R2:

The output voltage can be set from VIN to 18V with feedback resistor dividers R1 and R2. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10k and 1M is recommended for both resistors. Output voltage VDD1 can be calculated to be:

$$V_{DD1} = (1 + R1/R2) \times V_{FB}$$



Where V_{FB}=1.25V is the reference voltage.

Inductor L1:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L1 = (\frac{V_{IN}}{V_{DD1}})^2 \times \frac{(V_{DD1} - V_{IN}) \times \eta}{F_S \times I_{VDD1,MAX} \times 40\%}$$

Where F_S is the switching frequency, $I_{VDD1,MAX}$ is the maximum load current of the boost regulator and η is the estimating efficiency of that operating point.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \frac{V_{DD1}}{V_{IN} \times \eta} \times I_{VDD1,MAX} + \frac{V_{IN} \times (V_{DD1} - V_{IN})}{2 \times F_S \times L1 \times V_{DD1}}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

Output capacitor C_{OUT1}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. The output capacitor is calculated as:

$$C_{OUT1} = \frac{I_{VDD1} \times (V_{DD1} - V_{IN})}{F_S \times V_{DD1} \times \Delta V_{DD1}}$$

Where ΔV_{DD1} is output voltage ripple.

Input capacitor

The input capacitor reduces the ripple current drawn from input supply and reduces the noise injection into IC. The RMS current in the capacitor can be calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \times (V_{DD1} - V_{IN})}{2\sqrt{3} \times L_1 \times F_S \times V_{DD1}}$$

It is recommended to used an X5R or better grade ceramic capacitor with greater than 10uF capacitance. Greater voltage variation can be tolerated on C_{IN} if VDD is decoupled from C_{IN} using an RC low pass filter.

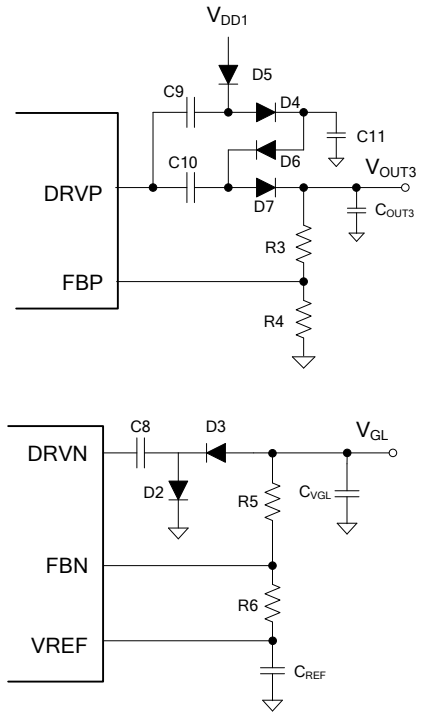
Fault Protection

During steady-state operation, if the output of the Boost regulator or any of charge pump outputs exceeds their respective fault-detection thresholds, the internal 130ms fault timer is activated. If fault condition continues, the fault timer will time out and the IC will shut down all outputs.

Charge-Pump Regulator

The positive charge-pump regulator is used to generate the positive supply rail for the TFT LCD gate-driver

ICs. And the negative charge-pump regulator is used to generate the negative supply rail for the TFT LCD gate-driver ICs. The output voltage is determined by the number of charge-pump stages and the setting of the feedback divider.



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The number of charge-pump stages

The number of positive charge-pump stages N_P is chosen by:

$$N_P \geq \frac{V_{OUT3} - V_{DD1}}{V_{DD1} - 2 \times V_D}$$

The number of negative charge-pump stages N_n is chosen by:

$$N_n \geq \frac{-V_{GL}}{V_{DD1} - 2 \times V_D}$$

Where V_{OUT3} is the output voltage of positive charge-pump regulator, V_{GL} is the output voltage of negative charge-pump regulator, V_D is the forward voltage drop of the charge-pump. The lowest number of charge-pump stages is always chosen for the highest efficiency.

The output voltage of charge-pump

Output voltage V_{OUT3} and V_{GL} can be calculated to be:

$$V_{OUT3} = (1 + R3/R4) \times V_{FBP}$$

$$V_{GL} = (V_{FBN} - V_{REF}) \times \frac{R5}{R6} + V_{FBN}$$

Where V_{FBP}=1.25V, V_{FBN}=0.3V, V_{REF}=1.3V.

Flying Capacitors(C_8,C_9,C_{10})

For the flying capacitors (C8, C9, C10), a 0.1μF ceramic capacitor is recommended, it works well in most low-current applications. The voltage rating V_{RX} of the flying capacitors as following:

$$V_{RX} > N \times V_{DD1}$$

Where N is the number of charge-pump stages.

The output capacitors of charge-pump(C_{OUT3},C_{VGL})

The output capacitor C_{OUT3} and C_{VGL} are selected to handle the output ripple noise requirements. The output capacitance is calculated as:

$$C_{OUT3} \geq \frac{I_{OUT3}}{2 \times F_S \times \Delta V_{OUT3}}$$

$$C_{VGL} \geq \frac{I_{VGL}}{2 \times F_S \times \Delta V_{VGL}}$$

Operational Amplifier

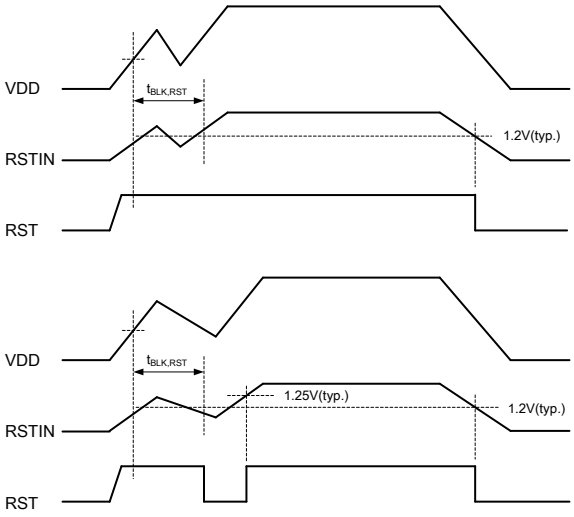
SY7630C contains one high performance operational amplifier to drive the LCD backplane or gamma-correction divider string. The OPAMP features ±200mA output short circuit current limitation, fast slew rate, wide bandwidth and rail-to-rail outputs.

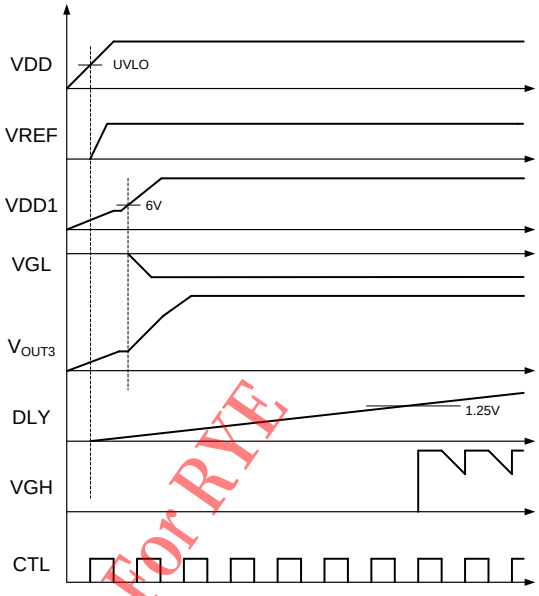
Gate Pulse Modulator

The gate pulse modulator contains two high voltage, p-channel MOSFETs. One MOSFET is between VO3 and VGH, the other is between VGH and ADJ. The control input pin CTL controls these two MOSFETs. Once CTL is activated, VGH connect to VO3 when CTL is high and VGH connect to ADJ when CTL is low. The CTL is not activated until all the following conditions are satisfied: the input voltage is higher than UVLO, all regulators finish soft-start routine, DLY pin voltage exceeds its turn-on threshold and there is no fault condition.

Reset Output

RST is an open-drain output. It is controlled by RSTIN and VDD. Once VDD voltage exceeds UVLO threshold, the reset circuit initiates a 380ms blanking period during which the drop on VDD is ignored and RST is set to high impedance. After this blanking period and if RSTIN goes below approximately 1.25V, RST is pulled low.





Power on sequence

When VDD exceed its UVLO threshold, the reference block turns on. After reference stabilize, the IC enables the boost regulator, the positive charge-pump regulator and the negative charge-pump regulator.

The start up delay time of gate pulse modulator block is determined by the capacitor C_{DEL}. After VDD exceed UVLO, a 5μA current source starts charging C_{DEL}, when V_{DEL} is higher than 1.25V, IC enable the gate pulse modulator, and the output of VGH is depending on the level of CTL pin. When VDD is less than UVLO, DLY pin is connected to AGND internally to discharge C_{DEL}. The delay time is calculated as:

$$T_{DELAY} = C_{DEL} \times \frac{1.25}{5uA}$$

Layout Design:

The layout design of SY7630C is very important for proper operation. Following are the tips for good PCB layout.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

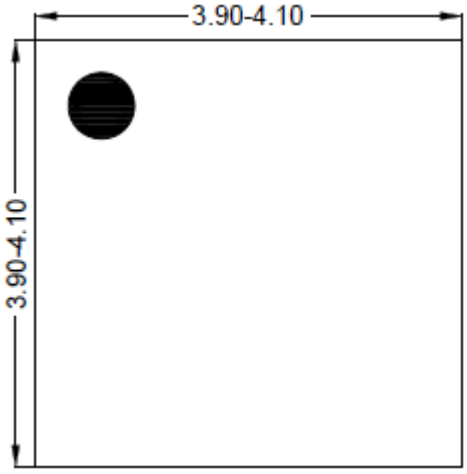
2) Place the VDD pin and REF pin bypass capacitors close to IC. The ground connection the bypass capacitor should be connected directly to the AGND pin with a wide trace.

3) Minimize the loop area formed by C_{VDD1}, D_1, LX and PGND of IC

4) The PCB copper area associated with switching nodes must be minimized to avoid the potential noise problem.

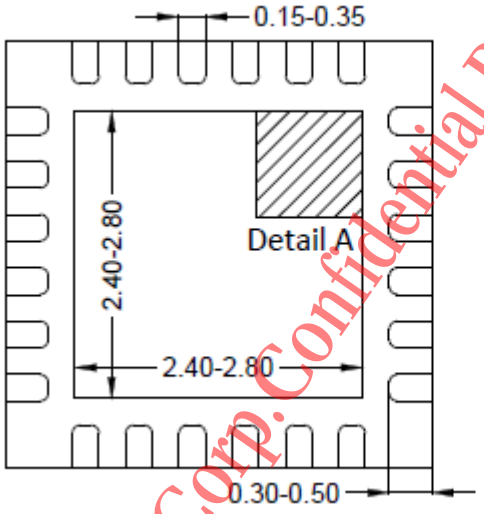
5) Place feedback resistors near to IC and avoid running feedback trace near to switching nodes.

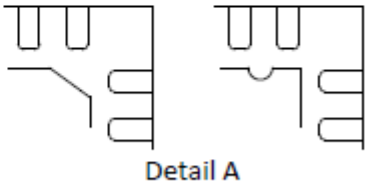
QFN4x4-24 Package Outline Drawing



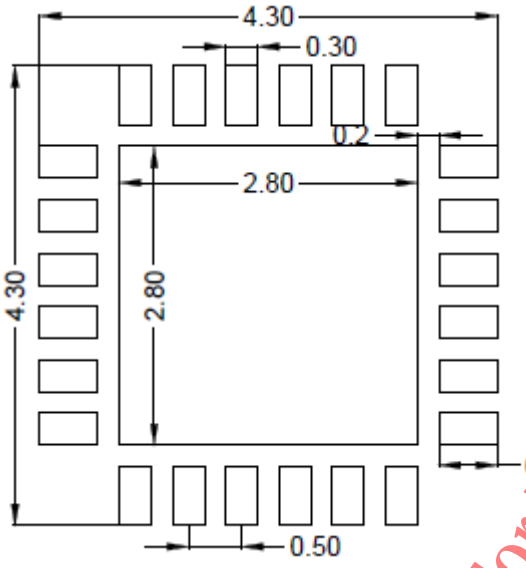
Top view

Side view





Bottom view



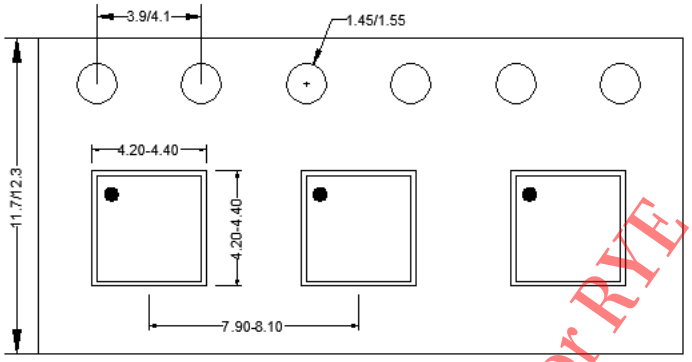
Recommended PCB layout
(Reference only)

Notes: All dimension in MM and exclude mold flash & metal burr

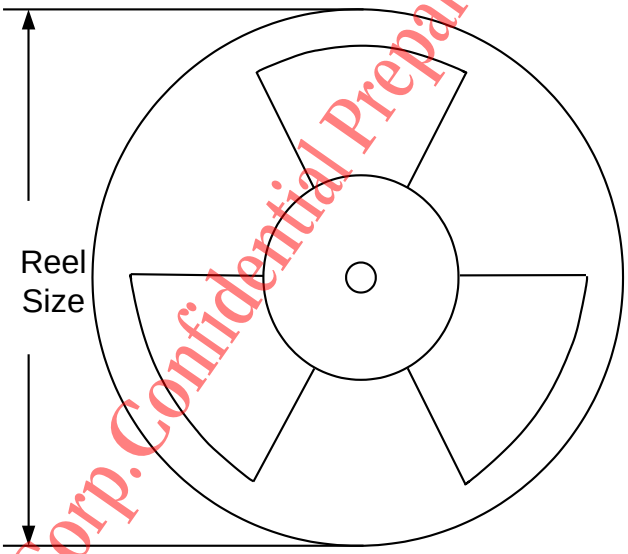
Taping & Reel Specification

1. Taping orientation

QFN4×4



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN4×4	12	8	13"	400	400	5000

3. Others: NA

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