ZL40240

Ten LVCMOS Output Low Additive Jitter Fanout Buffer

Features

- 3-to-1 Input Multiplexer
  - Two Inputs Accept Any Differential (LVPECL, HCSL, LVDS, SSTL, CML, LVCMOS) or a Single-Ended Signal.
  - The Third Input Accepts a Crystal or a Single-Ended Signal.
- Ten 1.5V/1.8V/2.5V/3.3V LVCMOS Outputs
- Supports Frequencies from 0 MHz to 250 MHz
- Ultra-Low System Level Additive Jitter at 17 fs (12 kHz to 20 MHz)
- Ultra-Low Noise Floor of −170 dBc/Hz
- Supports Crystals from 8 MHz to 160 MHz
- Supports 2.5V or 3.3V Power Supplies
- Output-to-Output Skew of 30 ps (Typical)
- Input-to-Output Delay of 2 ns (Typical)
- SPI or Hardware Control

Applications

- General Purpose Clock Distribution
- Low Jitter Clock Trees
- Logic Translation
- Clock and Data Signal Restoration
- Wired and Wireless Communications
- High Performance Microprocessor Clock Distribution
- Medical Imaging
- Test Equipment

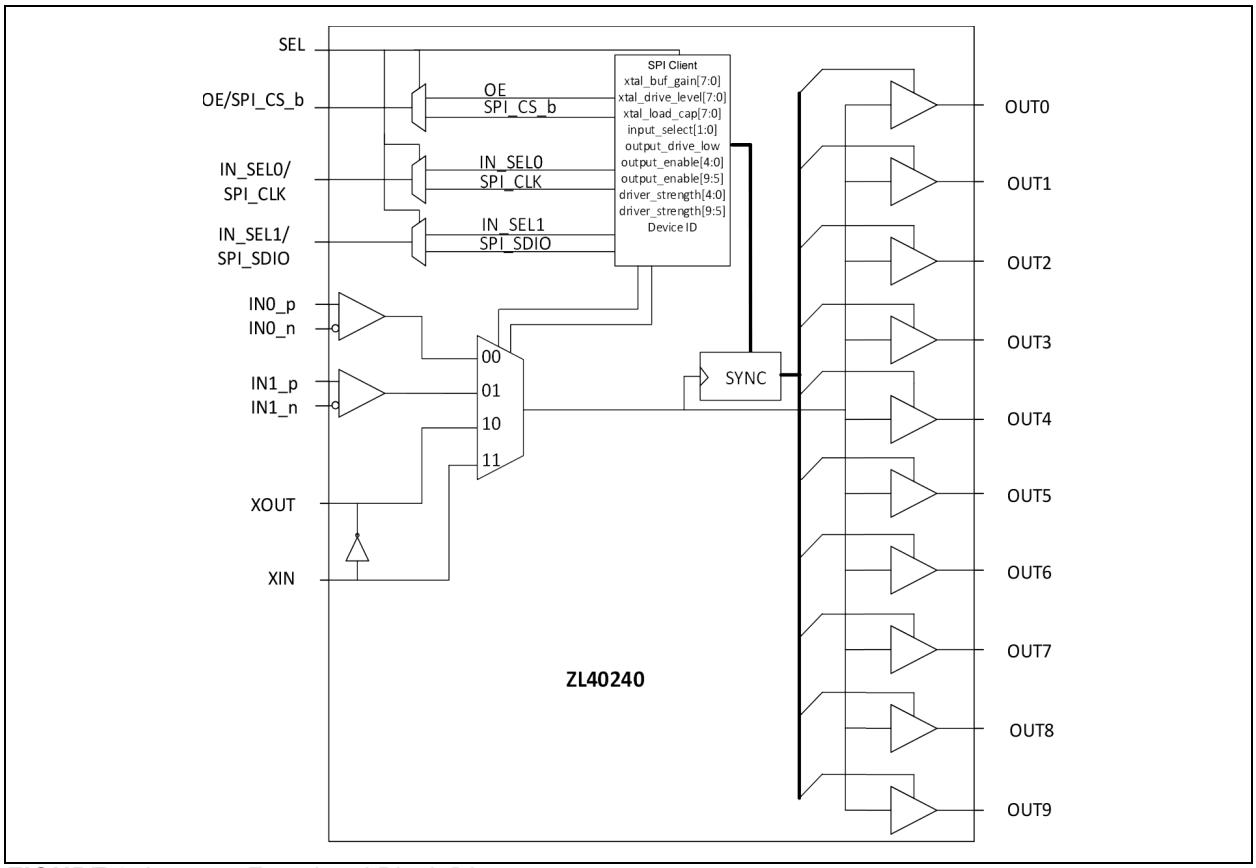


FIGURE 0-1: *Functional Block Diagram.*

© 2023 Microchip Technology Inc. and its subsidiaries

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; http://www.microchip.com
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

© 2023 Microchip Technology Inc. and its subsidiaries

TABLE OF CONTENTS

© 2023 Microchip Technology Inc. and its subsidiaries

List of Figures

© 2023 Microchip Technology Inc. and its subsidiaries

List of Tables

© 2023 Microchip Technology Inc. and its subsidiaries

1.0 PIN DESCRIPTION AND CONFIGURATION

The device is packaged in a 5 mm × 5 mm 32-lead VQFN.

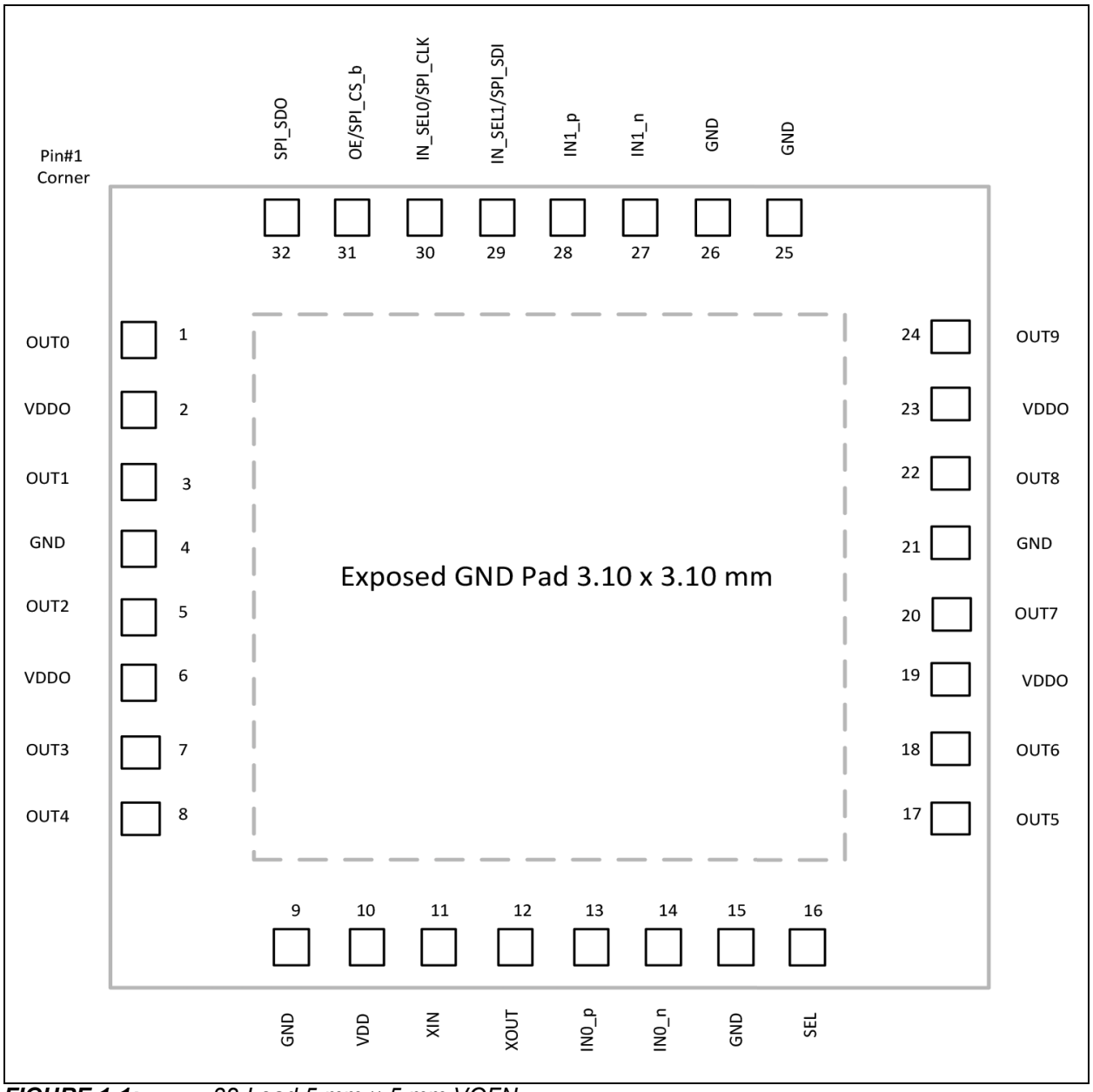


FIGURE 1-1: *32-Lead 5 mm × 5 mm VQFN.*

© 2023 Microchip Technology Inc. and its subsidiaries

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, I_{PU} – input with 300 kΩ internal pull-up resistor, I_{PD} – input with 300 kΩ internal pull-down resistor, I_{APU} – input with 30 kΩ internal pull-up resistor, I_{APD} – input with 30 kΩ internal pull-down resistor, $I_{APU/APD}$ – input biased at VDD/2 with 60 kΩ internal pull-up and 60 kΩ pull-down resistors, O – output, I/O – Input/Output pin, P – power supply pin.

TABLE 1-1: PIN DESCRIPTIONS

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">Input References</td></tr>
<tr><td>13</td><td>IN0_p</td><td>I_{APD}</td><td rowspan="4">Input Differential or Single Ended References 0 and 1

Input frequency range 0 Hz to 250 MHz.

Non inverting inputs (_p) are pulled down with internal 30 kΩ pull-down resistors. Inverting inputs (_n) are biased at VDD/2 with 60 kΩ pull-up and pull-down resistors to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference).</td></tr>
<tr><td>14</td><td>IN0_n</td><td>$I_{APU/APD}$</td></tr>
<tr><td>28</td><td>IN1_p</td><td>I_{APD}</td></tr>
<tr><td>27</td><td>IN1_n</td><td>$I_{APU/APD}$</td></tr>
<tr><td colspan="4">Output Clocks</td></tr>
<tr><td>1</td><td>OUT0</td><td rowspan="10">O</td><td rowspan="10">Ultra Low Additive Jitter LVCMOS Outputs 0 to 9

Output frequency range 0 Hz to 250 MHz.</td></tr>
<tr><td>3</td><td>OUT1</td></tr>
<tr><td>5</td><td>OUT2</td></tr>
<tr><td>7</td><td>OUT3</td></tr>
<tr><td>8</td><td>OUT4</td></tr>
<tr><td>17</td><td>OUT5</td></tr>
<tr><td>18</td><td>OUT6</td></tr>
<tr><td>20</td><td>OUT7</td></tr>
<tr><td>22</td><td>OUT8</td></tr>
<tr><td>24</td><td>OUT9</td></tr>
<tr><td colspan="4">Control</td></tr>
<tr><td rowspan="5">30</td><td rowspan="5">IN_SEL0/
SPI_CLK</td><td rowspan="5">I_{PD} or I_{PU}</td><td>Input Select 0/ Clock for Serial Interface. When SEL pin is low, this pin is Input Select 0 hardware control input pin, and it is pulled-low with 300 kΩ resistor.
When SEL pin is high, this pin provides clock for serial micro-port interface, and it is pulled-up with 300 kΩ resistor.</td></tr>
<tr><td>
<table>
<tr><th>IN_SEL1</th><th>IN_SEL0</th><th>OUTN</th></tr>
<tr><td>0</td><td>0</td><td>Input 0 (IN0)</td></tr>
<tr><td>0</td><td>1</td><td>Input 1 (IN1)</td></tr>
<tr><td>1</td><td>0</td><td>Crystal Oscillator or Overdrive</td></tr>
<tr><td>1</td><td>1</td><td>Crystal Bypass</td></tr>
</table>
</td></tr>
<tr><td>29</td><td>IN_SEL1/
SPI_SDI</td><td>I_{PD} or I_{PU}</td><td>Input Select 1/ Serial Interface Input. When SEL pin is low, this pin is Input Select 1 hardware control pin, and it is pulled down with 300 kΩ resistor.
When SEL pin is high, this pin is serial interface input stream, and it is pulled-up with 300 kΩ resistor. The serial data stream holds the access command, the address, and the write data bits.
Note: This input has low threshold voltage (V_{IH} = 1.2V), so it can be driven by low output voltage device from 1.5V or higher up to VDD.</td></tr>
<tr><td>32</td><td>SPI_SDO</td><td>I/O</td><td>Serial Interface Output. Serial interface output stream. As an output, the serial stream holds the read data bits.</td></tr>
</table>

© 2023 Microchip Technology Inc. and its subsidiaries

TABLE 1-1: PIN DESCRIPTIONS (CONTINUED)

Pin Number	Pin Name	Type	Description
31	OE/SPI_CS_b	I_{PD} or I_{PU}	**Output Enable/Chip Select for Serial Interface.** When SEL pin is low, this pin is Output Enable hardware control input, and it is pulled-down with 300 kΩ resistor. When SEL is high, this pin is serial interface chip select, and it is pulled-up with 300 kΩ resistor--this is an active low signal.
Crystal Oscillator			
11	XIN	I	**Crystal Oscillator Input or crystal bypass mode or crystal overdrive mode.** If crystal oscillator is not used pull down this pin or connect it to ground.
12	XOUT	O	**Crystal Oscillator Output.**
Hardware/SPI Control Selection			
16	SEL	I_{PD}	**Select Control.** When this pin is low, the device is controlled via hardware pins, IN_SEL0/1 and OE. When this pin is high, the device is controlled via SPI port. Any change of SEL pin value requires power cycle. Hence, SEL pin cannot be changed on the fly.
Power and Ground			
10	VDD	P	**Positive Supply Voltage.** Connect to 3.3V or 2.5V supply. VDD voltage must be higher or equal to VDDO.
2	VDDO	P	**Positive Supply Voltage for LVCMOS Outputs.** Connect 3.3V, 2.5V, 1.8V or 1.5V power supply.
6			
19			
23			
4	GND	P	**Ground.** Connect to ground.
9			
15			
21			
26			
25			
E-Pad			

© 2023 Microchip Technology Inc. and its subsidiaries

2.0 FUNCTIONAL DESCRIPTION

The ZL40240 is a programmable or hardware pin controlled low additive jitter, low power 3 × 10 LVCMOS fanout buffer.

Two inputs can accept signal in differential (LVPECL, SSTL, LVDS, HSTL, CML) or single ended (LVPECL or LVCMOS) format and the third input can accept a single ended signal or it can be used to build a crystal oscillator by connecting an external crystal resonator between its XIN and XOUT pins. All the other components for building crystal oscillator are built in device such as load capacitance, series and shunt resistors.

The ZL40240 has ten LVCMOS outputs which can be powered from 3.3V, 2.5V, 1.8V or 1.5V supply. Each output can be independently enabled/disabled via SPI bus. In addition, the strength of each output can be programmed.

The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

2.1 Clock Inputs

The following block diagrams show how to terminate different signals fed to the ZL40240 inputs. Figure 2-1 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each so that the transmission line is terminated with matched impedance (50Ω). However, if the driving strength of the output driver is not sufficient resistor values should be increased.

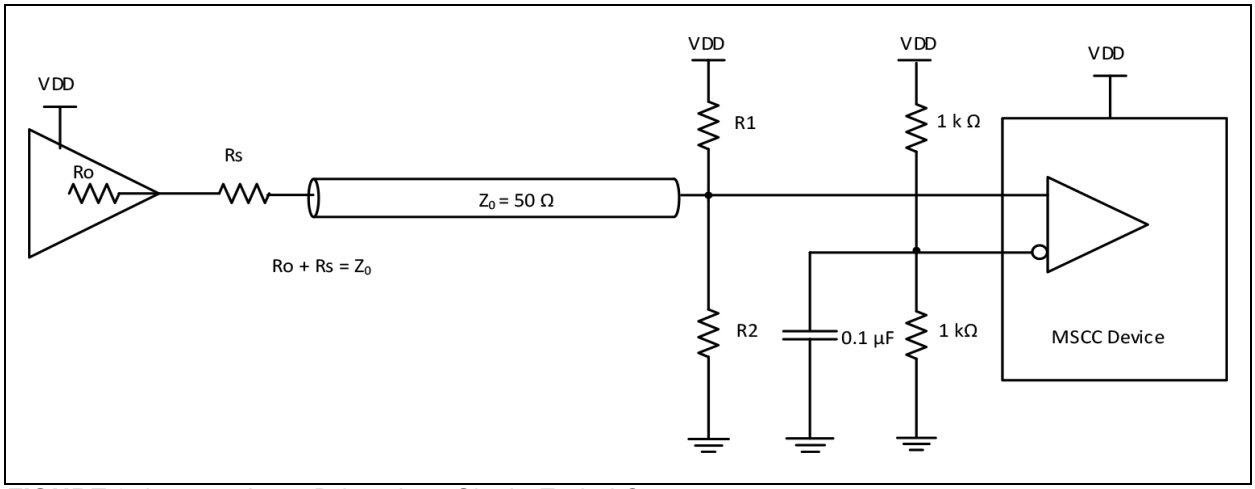


FIGURE 2-1: *Input Driven by a Single-Ended Output.*

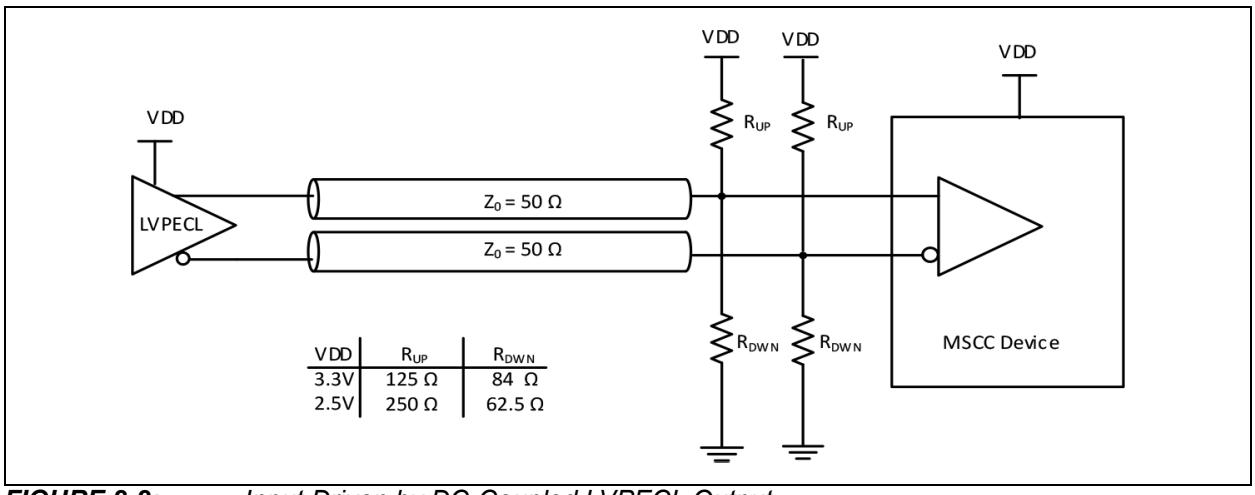


FIGURE 2-2: *Input Driven by DC-Coupled LVPECL Output.*

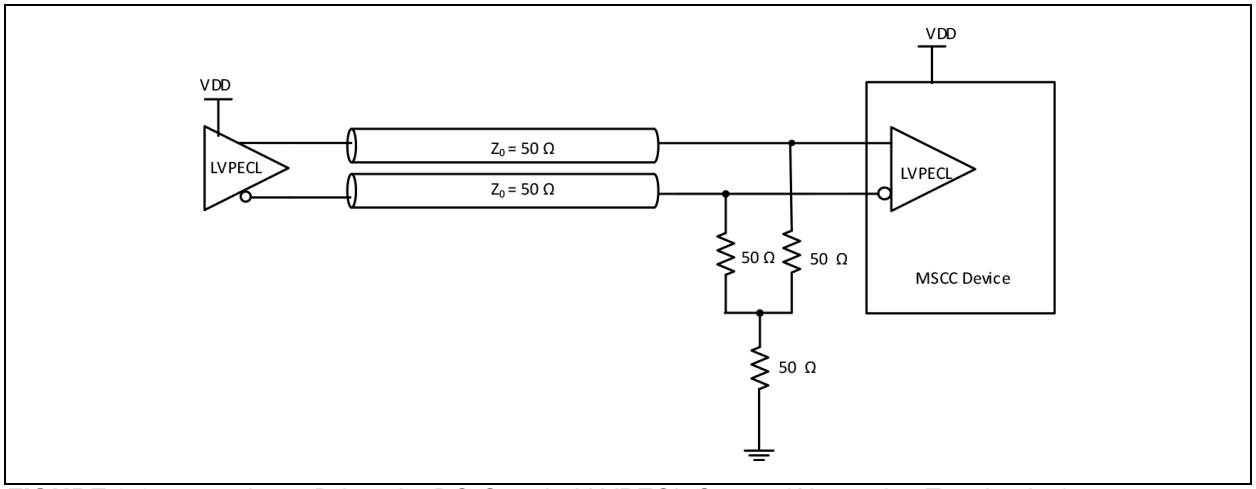


FIGURE 2-3: *Input Driven by DC-Coupled LVPECL Output (Alternative Termination).*

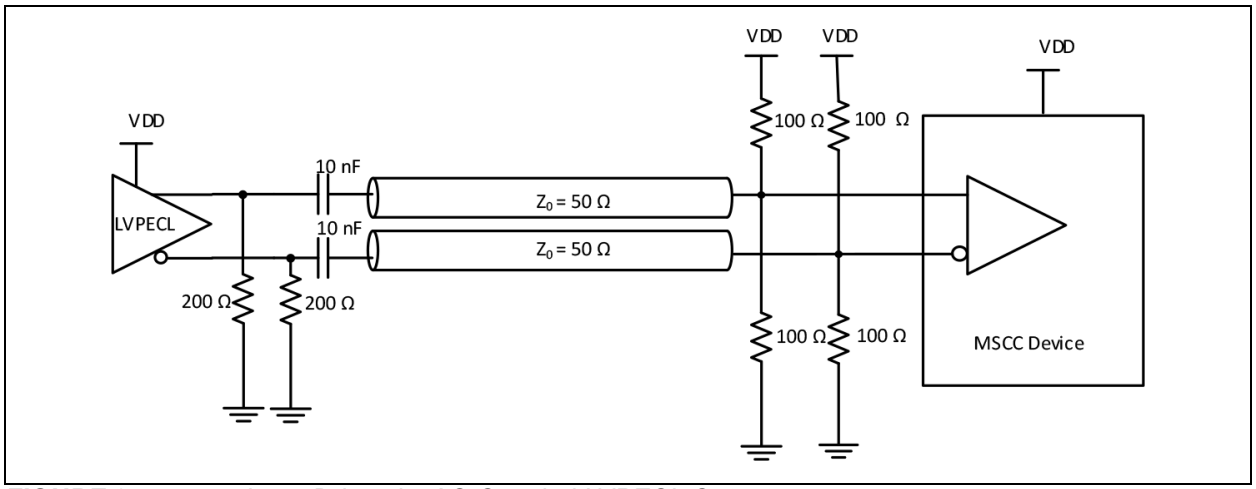


FIGURE 2-4: *Input Driven by AC-Coupled LVPECL Output.*

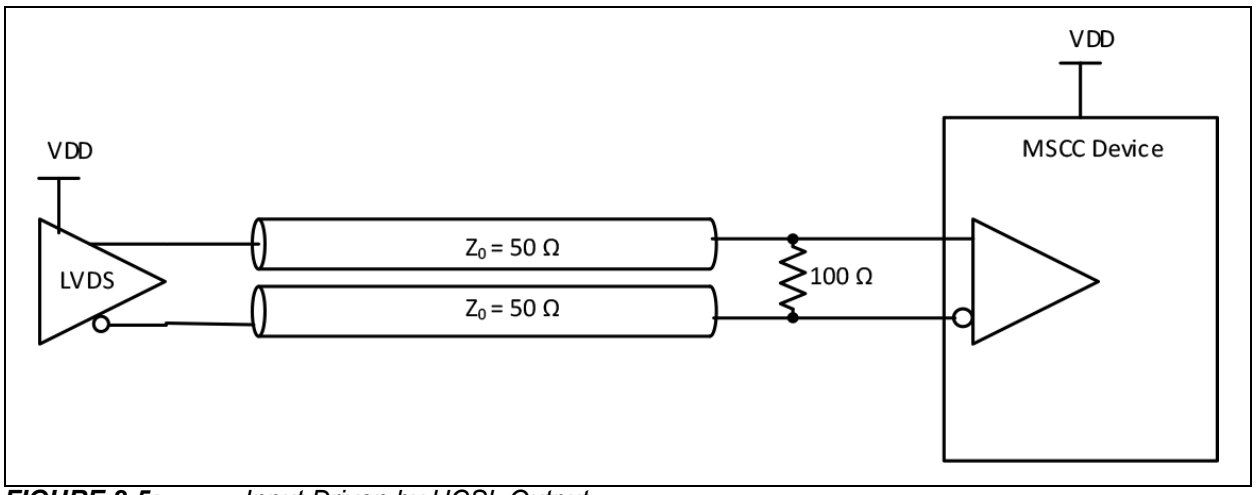


FIGURE 2-5: *Input Driven by HCSL Output.*

© 2023 Microchip Technology Inc. and its subsidiaries

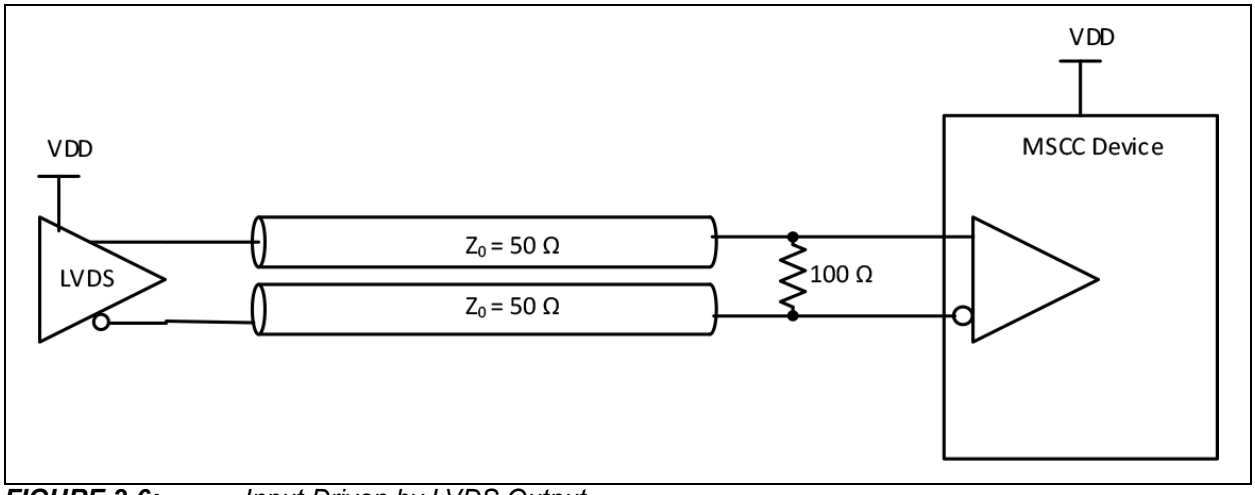


FIGURE 2-6: *Input Driven by LVDS Output.*

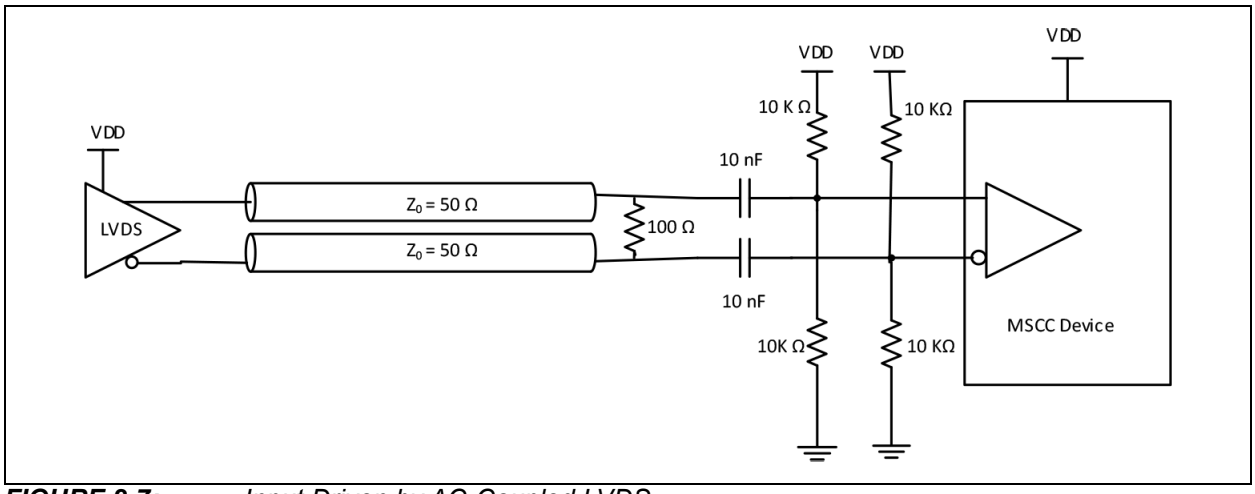


FIGURE 2-7: *Input Driven by AC-Coupled LVDS.*

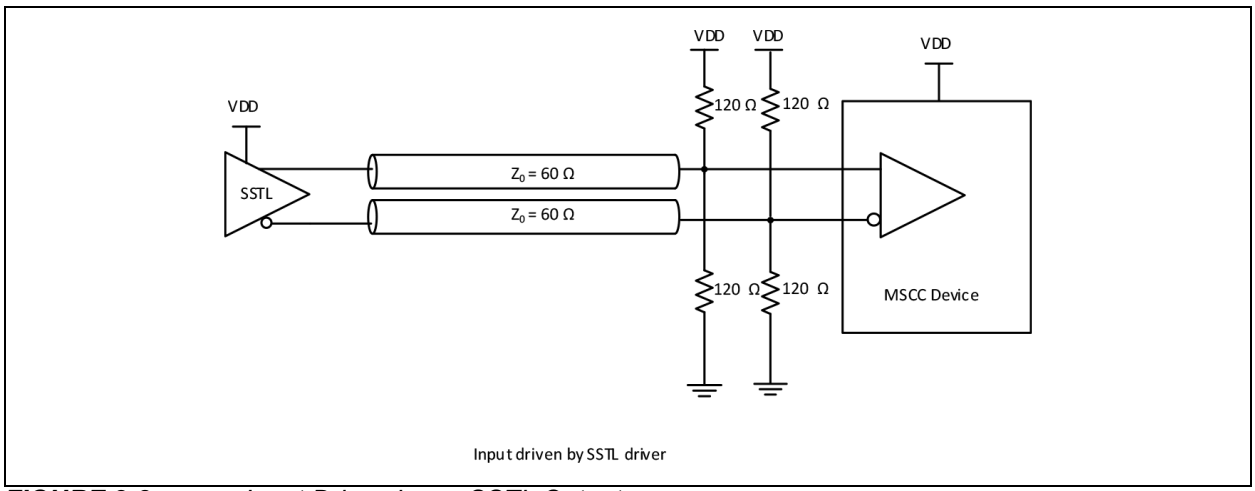


FIGURE 2-8: *Input Driven by an SSTL Output.*

2.2 Clock Outputs

LVCMOS outputs require only series termination resistor whose value is depending on LVCMOS output voltage as shown in Figure 2-9. The recommended series termination depends on programmed strength of the driver (low or high) and on the output driver supply voltage.

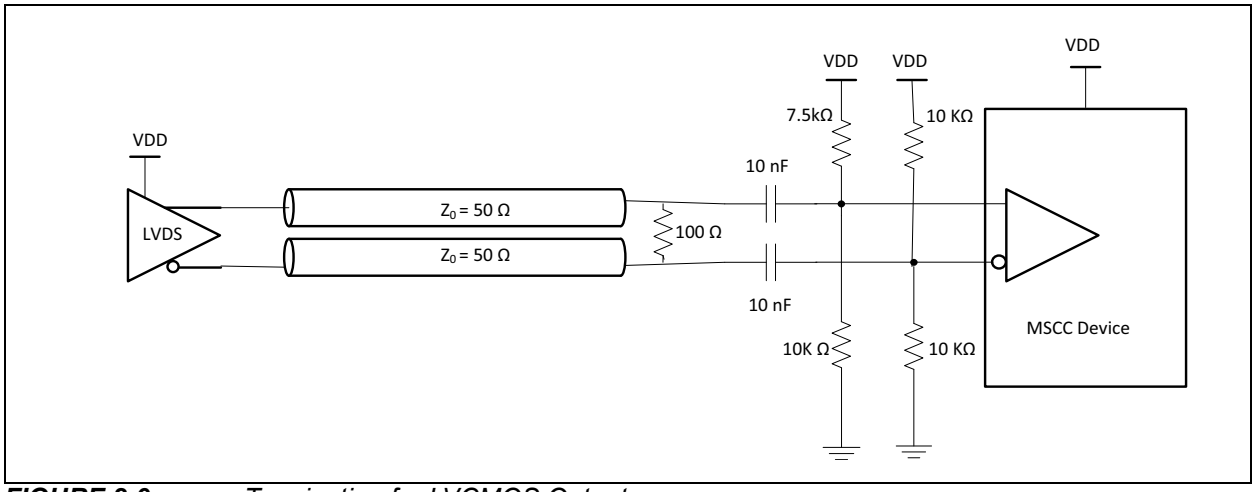


FIGURE 2-9: *Termination for LVCMOS Outputs.*

2.3 Crystal Oscillator Input

The crystal oscillator circuit can work with crystal resonators from 8 MHz to 160 MHz. To be able support crystal resonators with different characteristics all internal components are programmable in SPI Controlled mode.

Load capacitors can be programmed from 0 pF to 21.75 pF with resolution of 0.25 pF, which not only meets load requirement for most crystal resonator, but also allows for fine tuning of the crystal resonator frequency. The amplifier gain can be adjusted in eight steps and the series resistor in six steps. Shunt resistor has fixed value of 500 KΩ.

In Hardware Controlled mode, the capacitive load is set at 8 pF and cannot be changed. For Crystal requiring higher load, additional capacitance can be added externally, as shown in the Figure 2-10.

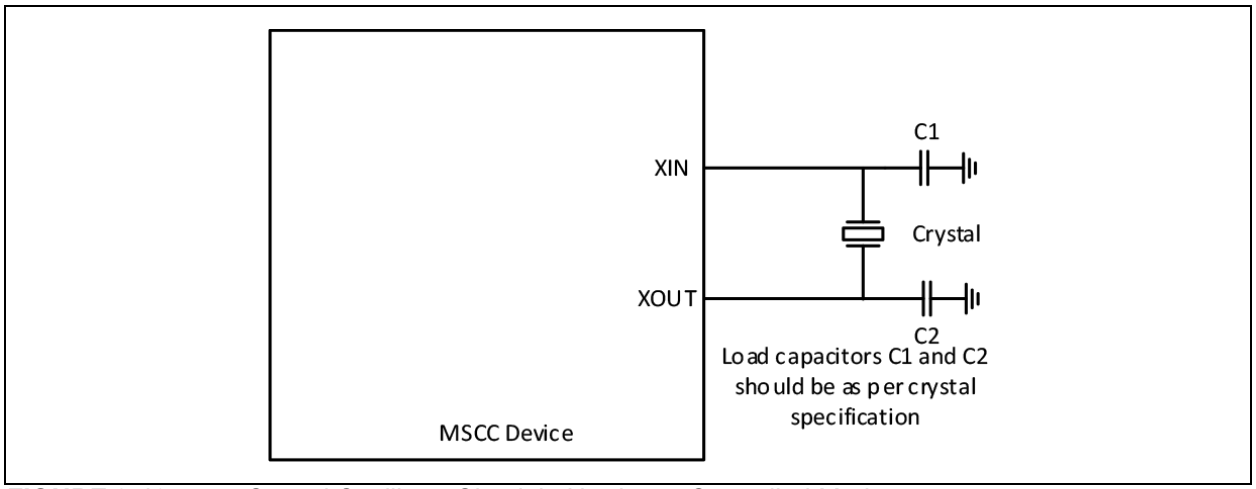


FIGURE 2-10: *Crystal Oscillator Circuit in Hardware Controlled Mode.*

If the crystal is not used, connect XIN pin to ground. This applies to both SPI and Hardware controlled mode.

The phase noise plot for 25 MHz crystal is shown in Figure 2-13. The phase noise floor of the device is below 170 dBc/Hz as can be seen on the figure. Figure 2-12 shows the phase noise plot with 125 MHz crystal.

© 2023 Microchip Technology Inc. and its subsidiaries

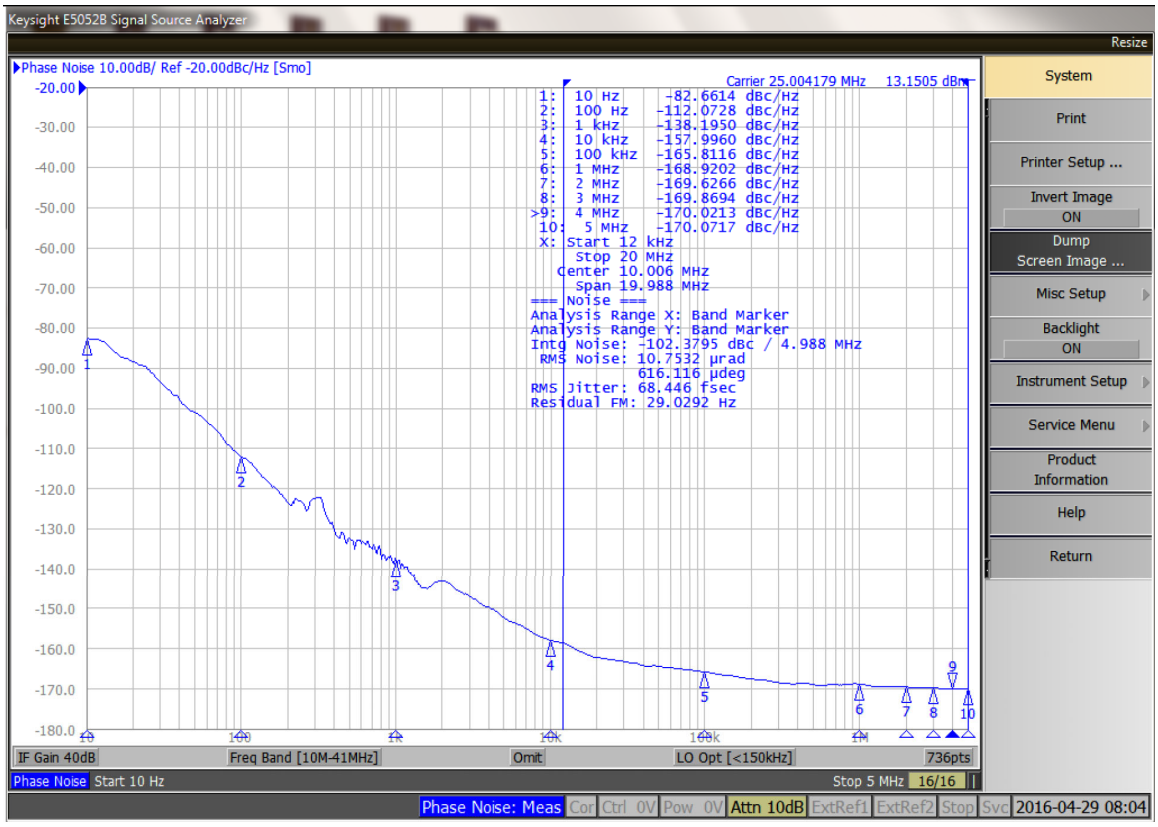


FIGURE 2-11: *Phase Noise Plot with 25 MHz Crystal.*

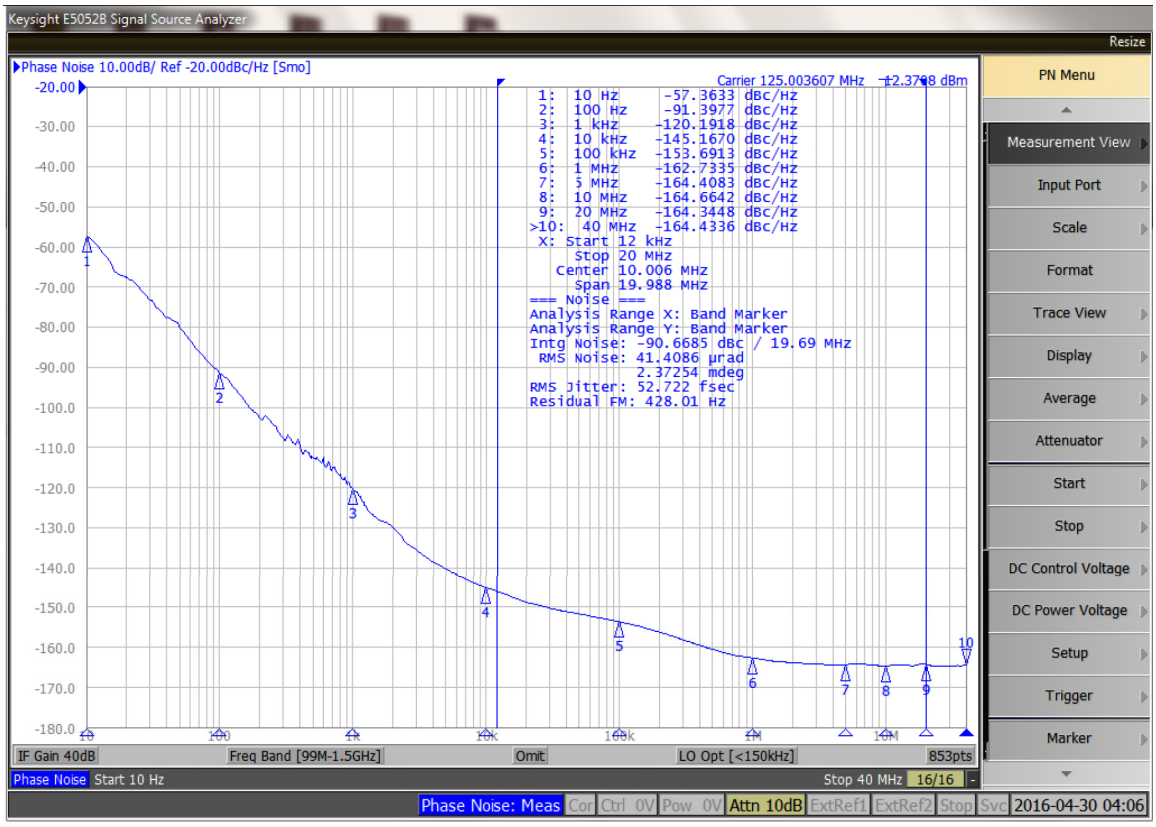


FIGURE 2-12: *Phase Noise Plot with 125 MHz Crystal.*

2.4 Termination of Unused Inputs and Outputs

Unused inputs can be left unconnected or alternatively IN_0/1 can be pulled-down by 1 KΩ resistor. Unused outputs should be left unconnected.

2.5 Power Consumption

The total device power consumption can be calculated as:

EQUATION 2-1:

$$P_T = P_S + P_{XTAL} + P_C + P_D$$

Where:

$P_S = V_{DD} \times I_S$	This is static power consumed by input buffers. If XTAL is running, this power should be set to zero. The static current (I_S) is specified in Table 4-2.
$P_{XTAL} = V_{DD} \times I_{DD\_XTAL}$	This is the power consumption of the XTAL circuit. The current of the XTAL circuit is provided in Table 4-2. If XTAL is not used, the power consumption is equal to zero.
$P_C = V_{DDO} \times I_{DDC}$	Common output power shared among all ten outputs. The current I_{DDC} is specified inTable 4-2.
$P_D = V_{DDO} \times (I_{DD} \times n \times f / 100\ MHz + V_{DD} \times C_{LOAD} \times f \times n)$	Dynamic power where dynamic current (I_{DD}) is specified in Table 4-2. C_{LOAD} is capacitive load driven by an output, f is frequency of hte output clock and n is number of active outputs.

© 2023 Microchip Technology Inc. and its subsidiaries

The power consumption for different clock frequencies and power supply voltages can be quickly estimated from Figure 2-13, Figure 2-14, and Figure 2-15.

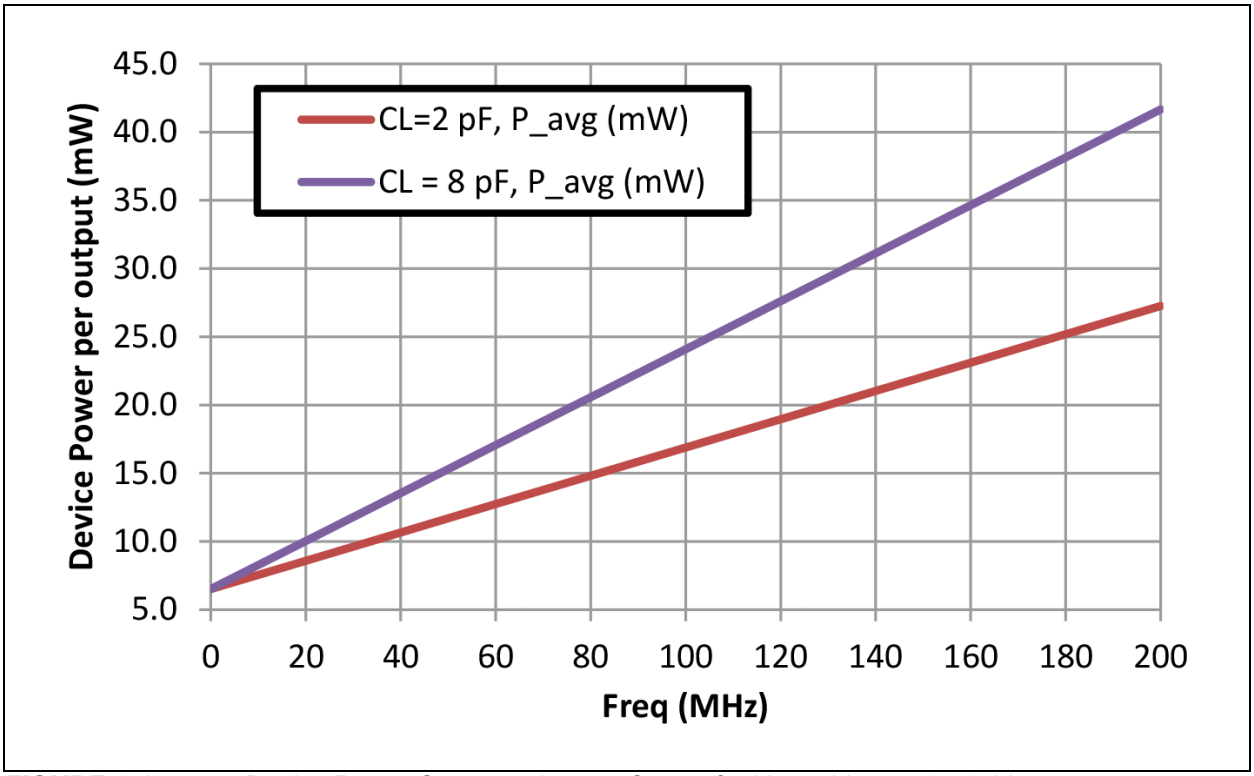


FIGURE 2-13: *Device Power Consumption per Output for V_{DD} = V_{DDO} = 3.465V.*

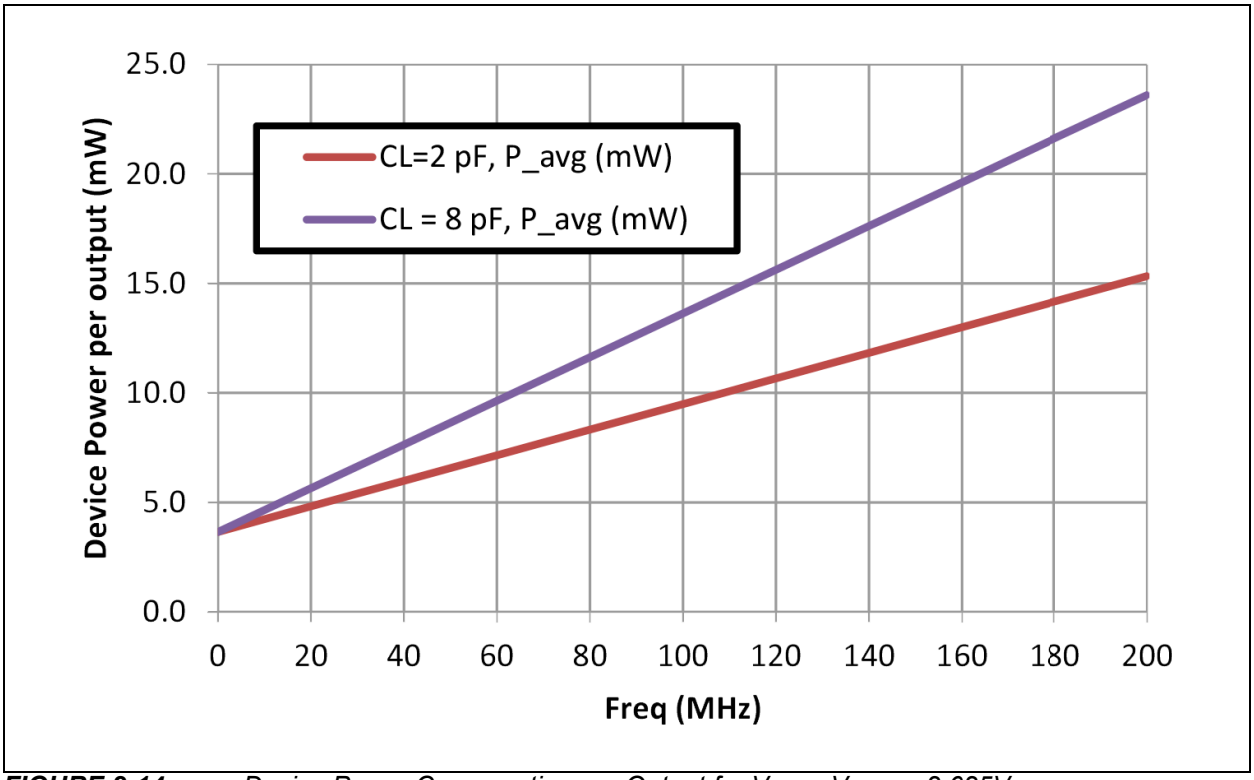


FIGURE 2-14: *Device Power Consumption per Output for V_{DD} = V_{DDO} = 2.625V.*

© 2023 Microchip Technology Inc. and its subsidiaries

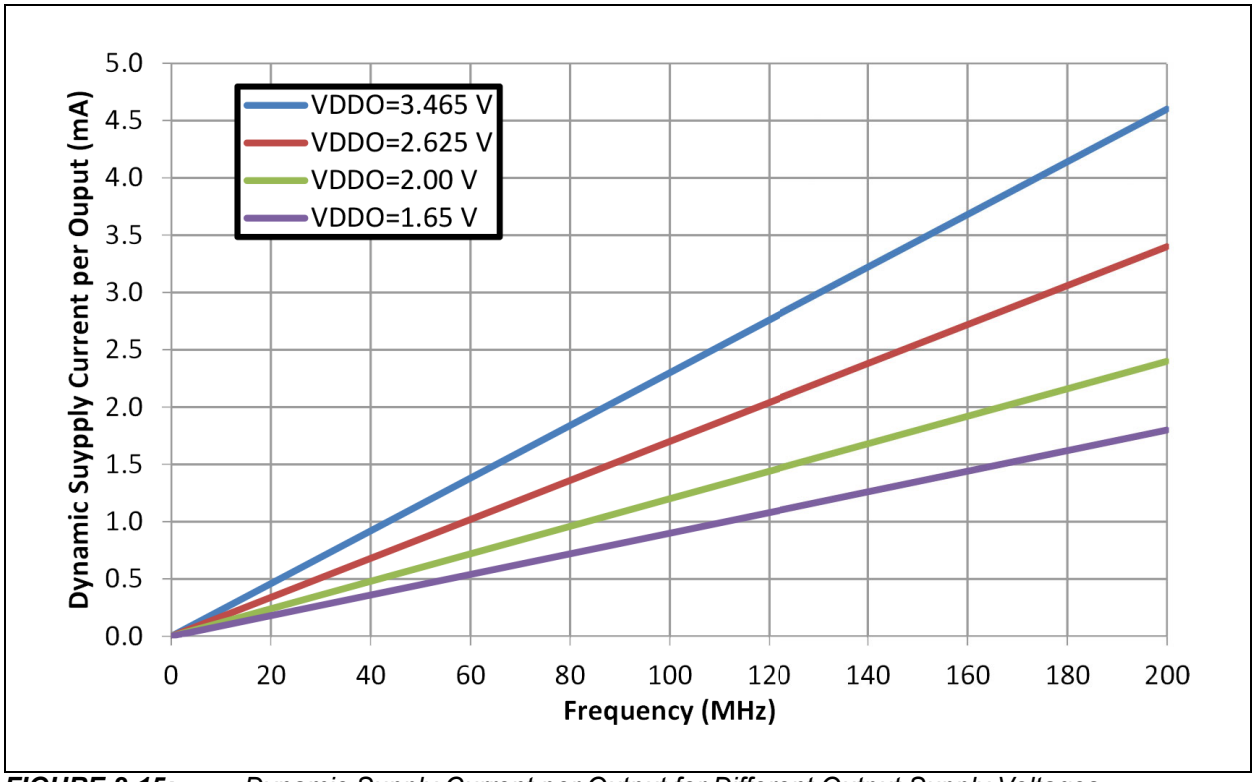


FIGURE 2-15: *Dynamic Supply Current per Output for Different Output Supply Voltages.*

2.6 Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with 0.1 µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example, 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board each power supply could be further insulated with low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Figure 2-16 shows recommended decoupling for each power pin.

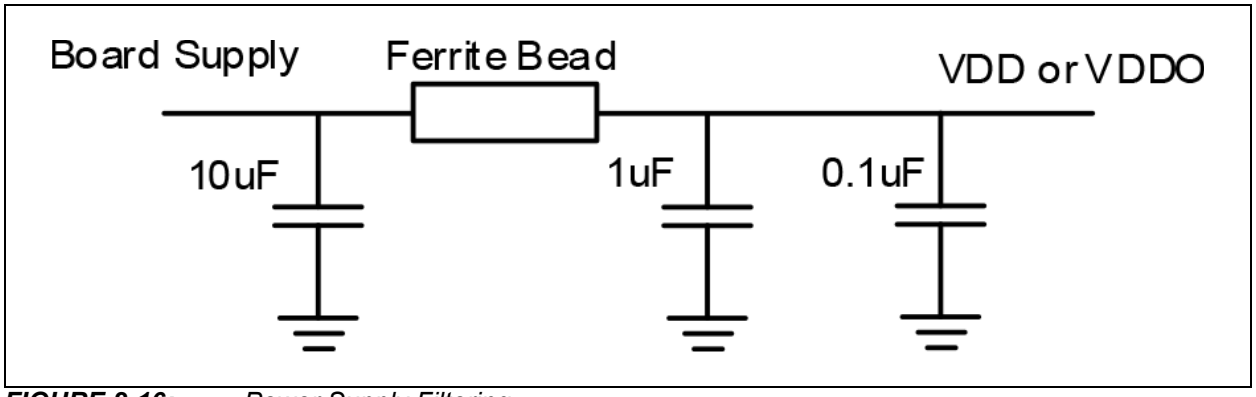


FIGURE 2-16: *Power Supply Filtering.*

2.7 Device Control

ZL30240 can be controlled via hardware pins (SEL pin tied low) or via SPI port (SEL pin tied high). The mode shall be selected during power up and it cannot be changed on the fly.

2.7.1 HARDWARE CONTROL MODE

In this mode, ZL40240 is controlled via Output Enable (OE) and Input Select (SEL0/1) input pins.

© 2023 Microchip Technology Inc. and its subsidiaries

2.7.2 SPI CONTROLLED MODE

In this mode ZL40240 is controlled via four pin SPI client interface as shown in Figure 2-17.

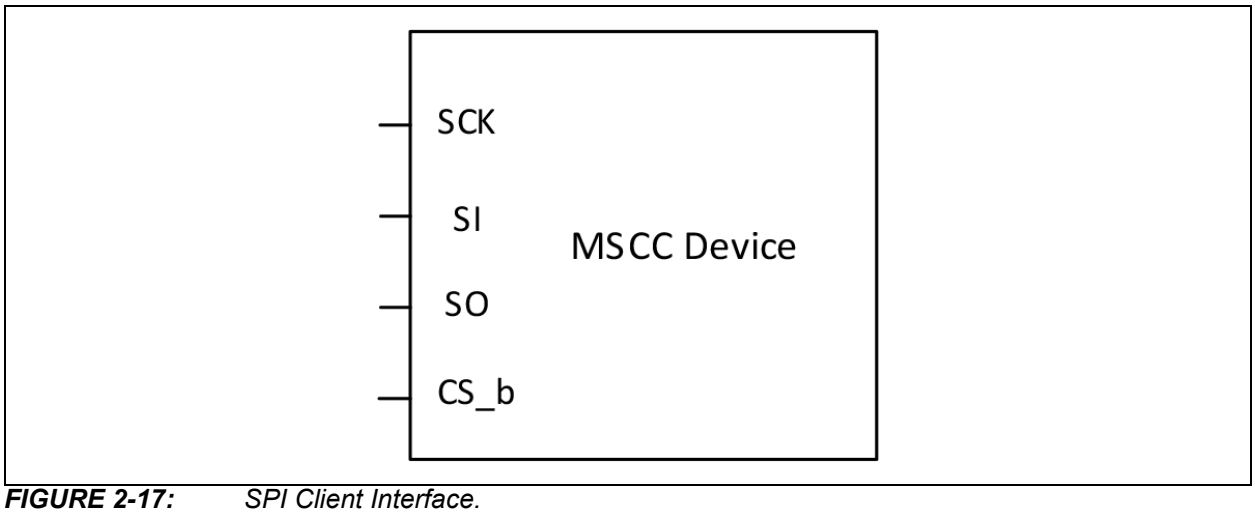


FIGURE 2-17: *SPI Client Interface.*

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the device, output data from the SO pin must be ignored. Similarly, the input data on the SI pin is ignored by the device during a read cycle.

The SPI interface supports two modes of access: Most Significant bit (MSb) first transmission or Least Significant bit (LSb) first transmission. The mode is automatically selected based on the state of SCK pin when the CS_b pin is active. If the SCK pin is low during CS_b activation, then MSb first timing is selected. If the SCK pin is high during CS_b activation, then LSb first timing is assumed.

The SPI port expects 1 bit to differentiate between read and write operation followed by 7-bit addressing and 8-bit data transmission. During SPI access, the CS_b pin must be held low until the operation is complete. Burst read/write mode is also supported by leaving the chip select signal CS_b is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

Functional waveforms for the LSb and MSb first mode, and burst mode are shown in Figure 2-18 and Figure 2-19 respectively. Figure 2-20 shows an example of burst mode operation which allows user to read or write consecutive location in the register map.

© 2023 Microchip Technology Inc. and its subsidiaries

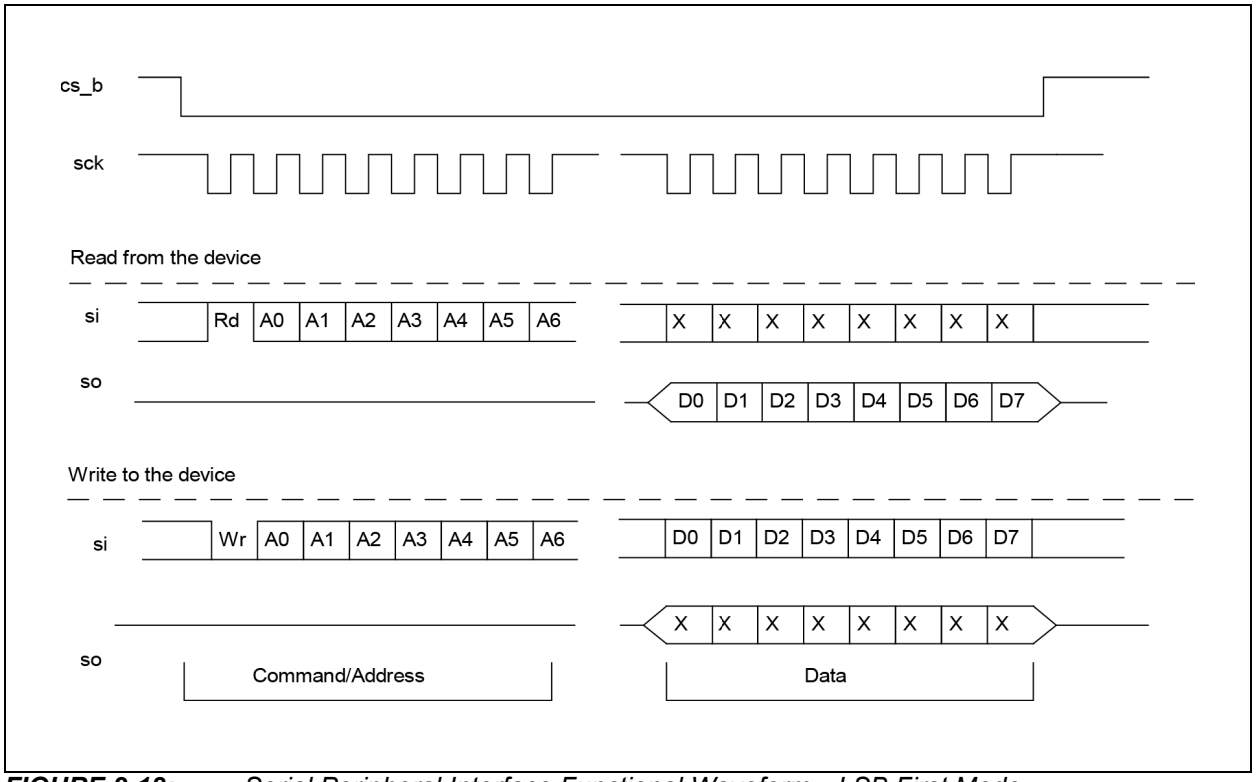


FIGURE 2-18: *Serial Peripheral Interface Functional Waveform—LSB First Mode.*

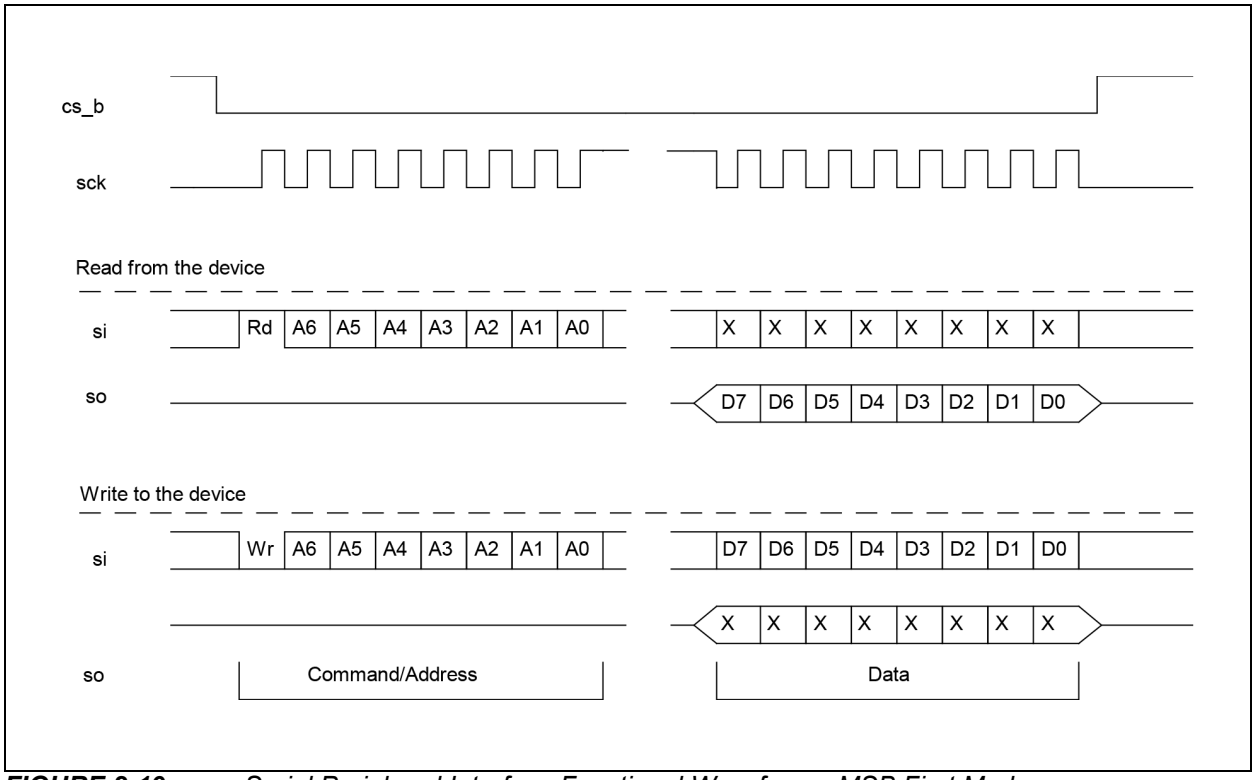


FIGURE 2-19: *Serial Peripheral Interface Functional Waveform—MSB First Mode.*

© 2023 Microchip Technology Inc. and its subsidiaries

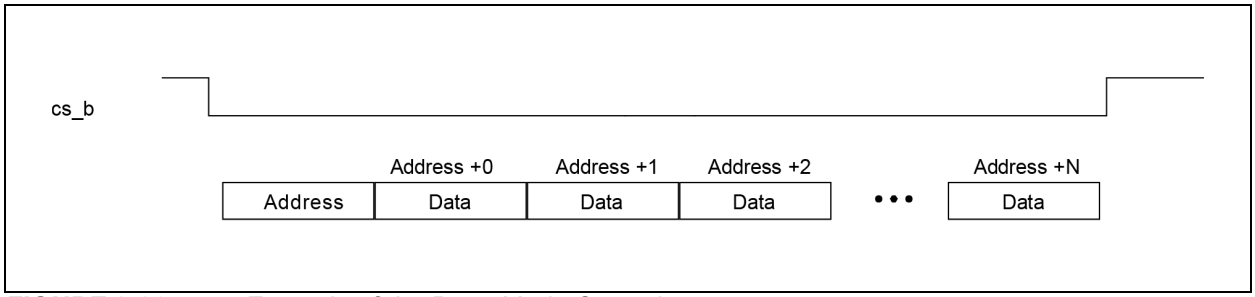


FIGURE 2-20: *Example of the Burst Mode Operation.*

NOTES:

© 2023 Microchip Technology Inc. and its subsidiaries

3.0 REGISTER MAP

The device is controlled by accessing registers through the serial interface. The following table provides a summary of the registers available for the configuration of the device.

TABLE 3-1: REGISTER MAP

Address SPI A[6:0] Hex (0x)	Name	Data D[7:0]
00	XTALBG	xtal_buf_gain[7:0]
01	XTALDL	xtal_drive_level[7:0]
02	XTALLC	xtal_load_cap[7:0]
03	XTALNR	xtal_normal_run
04	—	Not used
05	INSEL	input_select[1:0]
06	OUTLOW	output_drive_low
07	OUTEN0	output_enable[4:0]
08	OUTEN1	output_enable[9:5]
09	DRVSTR0	driver_strength[4.0]
0A	DRVSTR1	driver_strength[9.5]
0B/0C/0D/0E	—	Not used
0F/10	Reserved	Leave as default
11	DEVID	Device ID
12 to 1F	Reserved	Leave as default

TABLE 3-2: 0X00 XTALBG - XTAL BUFFER GAIN

Bit	Name	Description	Type	Reset
7:0	xtal_buf_gain[7:0]	Programs crystal buffer (inverting amplifier) gain. Every bit pair (bits: 01, 23, 45, 67) of this register correspond to additional equal gain block which can be added (bits set) or removed (bits cleared). Minimum gain is 0x00 (default) and 0xFF is maximum gain When reference input mode is “bypass XTAL mode” or “differential input modes” with HIGH xtal_normal_run bit, the buffer is disabled and follows “Input Selection”. When xtal_normal_run bit is LOW, XTAL buffer is in the “xtal forced run” mode and keep running. 8’b0000_0000: default crystal buffer strength. 8’b0000_0011: enable additional buffer strength 8’b0000_1100: enable additional buffer strength 8’b0011_0000: enable additional buffer strength 8’b1100_0000: enable additional buffer strength	RW	FF

TABLE 3-3: 0X01 XTALDL - XTAL DRIVE LEVEL

Bit	Name	Description	Type	Reset
7:0	xtal_drive_level[7:0]	Internal damping resistance of crystal circuit to limit external crystal's drive level uW. The value of damping resistor is determined by crystal's motion resistance of crystal's equivalent circuit. Drive level should be lower than crystal manufacturer's specification. Crystal's equivalent values should be requested to the manufacturer, (motion resistance and shunt capacitance). The selected resistors are connected to XOUT. Multiple bit combinations available by 7-bit control. Resistors are connected in parallel. Hence, 0xFF is the smallest resistance and 0x01 is the highest resistance. 8'b0000_0000: disable all resistors 8'b0000_0001: 312 Ω resistor 8'b0000_0010: 161 Ω resistor 8'b0000_0100: 84 Ω resistor 8'b0000_1000: 42 Ω resistor 8'b0001_0000: 21 Ω resistor 8'b0010_0000: 10.5 Ω resistor 8'b0100_0000: 0 Ω connection 8'b1000_0000: not used	RW	03

TABLE 3-4: 0X02 XTALLC - XTAL LOAD CAPACITANCE

Bit	Name	Description	Type	Reset
7:0	xtal_load_cap[7:0]	Internal load capacitance of crystal circuit (0 pF to 21.75 pF with the resolution of 0.25 pF). XIN and XOUT have each capacitor connected to GND. Multiple bit combinations available between 8 capacitors. 8'b0000_0000: disable all xtal load capacitors 8'b0000_0001: enable capacitor 0.25 pF 8'b0000_0010: enable capacitor 0.5 pF 8'b0000_0100: enable capacitor 1 pF 8'b0000_1000: enable capacitor 2 pF 8'b0001_0000: enable capacitor 2 pF 8'b0010_0000: enable capacitor 4 pF 8'b0100_0000: enable capacitor 4 pF 8'b1000_0000: enable capacitor 8 pF	RW	80 (8 pF)

© 2023 Microchip Technology Inc. and its subsidiaries

TABLE 3-5: 0X03 XTALNR - XTAL NORMAL RUN

Bit	Name	Description	Type	Reset
7:1	Unused	Unused	R	1111111
0	xtal_normal_run	When this bit is set high crystal oscillator circuit is running only if input_select[1:0] register at address 0x05 selects crystal mode (2'b10). This value is recommended because it provides best jitter performance—XO circuit is running only when it is needed. When this bit is set low the crystal oscillator will keep running even if crystal oscillator is not selected in input_select[1:0] register at address 0x05. This mode should only be used when fast switching between input references and crystal oscillator is required.	RW	1

TABLE 3-6: 0X03 XTALNR - XTAL NORMAL RUN

Bit	Name	Description	Type	Reset
7:1	Unused	Unused	R	1111111
0	xtal_normal_run	When this bit is set high crystal oscillator circuit is running only if input_select[1:0] register at address 0x05 selects crystal mode (2'b10). This value is recommended because it provides best jitter performance--XO circuit is running only when it is needed. When this bit is set low the crystal oscillator will keep running even if crystal oscillator is not selected in input_select[1:0] register at address 0x05. This mode should only be used when fast switching between input references and crystal oscillator is required.	RW	1

TABLE 3-7: 0X05 INSEL - INPUT SELECT REGISTER

Bit	Name	Description	Type	Reset
7:2	Unused	Unused	R	1111111
1:0	input_select[1:0]	Input reference clock selection. Proper external coupling and termination are required. 2'b00: differential input from IN0_p and IN0_n 2'b01: differential input from IN1_p and IN1_n 2'b10: 1) fundamental XTAL mode with XIN and XOUT (Use internal crystal oscillator circuits) OR 2) XTAL overdrive mode (single-ended clock signal with XIN) 2'b11: XTAL bypass mode (single-ended clock signal with XIN and disabled internal crystal buffer circuit in the analog block)	RW	10

TABLE 3-8: 0X06 OUTLOW - OUTPUT DRIVE LOW

Bit	Name	Description	Type	Reset
7:1	Unused	Unused	R	1111111
0	output_drive_low	After disabling outputs, output state is known state in logic LOW. (This bit is used for only disabled outputs. Otherwise, enabled outputs are not impacted by this bit.) 1'b0: All LVCMOS outputs will be in high-impedance state. 1'b1: All LVCMOS outputs will drive logic LOW.	RW	0

TABLE 3-9: 0X07 OUTEN0 - OUTPUT ENABLE 0

Bit	Name	Description	Type	Reset
7:5	Unused	Unused	R	111
4:0	output_enable[4.0]	Output enable for OUT0/1/2/3/4. Disabled state is dependent on "out_drive_low" control bit. Each bit controls one output. 5'b0_0000: disable outputs 5'b0_0001: enable OUT0 5'b0_0010: enable OUT1 5'b0_0100: enable OUT2 5'b0_1000: enable OUT3 5'b1_0000: enable OUT4	RW	11111

TABLE 3-10: 0X08 OUTEN1 - OUTPUT ENABLE 1

Bit	Name	Description	Type	Reset
7:5	Unused	Unused	R	111
4:0	output_enable[9:5]	Output enable for OUT5/6/7/8/9. Disabled state is dependent on "out_drive_low" control bit. Each bit controls one output. 5'b0_0000: disable outputs 5'b0_0001: enable OUT5 5'b0_0010: enable OUT6 5'b0_0100: enable OUT7 5'b0_1000: enable OUT8 5'b1_0000: enable OUT9	RW	11111

© 2023 Microchip Technology Inc. and its subsidiaries

TABLE 3-11: 0X09 DRVSTR0 - DRIVER STRENGTH 0

Bit	Name	Description	Type	Reset
7:5	Unused	Unused	R	111
4:0	driver_strength[4:0]	Output driver strength for OUT0/1/2/3/4. Each bit controls one output. Low driver strength and high driver strength. 5'b0_0000: low driver strength outputs 5'b0_0001: high driver strength for OUT0 5'b0_0010: high driver strength for OUT1 5'b0_0100: high driver strength for OUT2 5'b0_1000: high driver strength for OUT3 5'b1_0000: high driver strength for OUT4	RW	11111

TABLE 3-12: 0X0A DRVSTR1 - DRIVER STRENGTH 1

Bit	Name	Description	Type	Reset
7:5	Unused	Unused	R	111
4:0	driver_strength[9:5]	Output driver strength for OUT5/6/7/8/9. Each bit controls one output. Low driver strength and high driver strength. 5'b0_0000: low driver strength outputs 5'b0_0001: high driver strength for OUT5 5'b0_0010: high driver strength for OUT6 5'b0_0100: high driver strength for OUT7 5'b0_1000: high driver strength for OUT8 5'b1_0000: high driver strength for OUT9	RW	11111

TABLE 3-13: 0X11 DEVID - DEVICE IDENTIFICATION

Bit	Name	Description	Type	Reset
7:5	Unused	Unused	R	0
4:0	dev_id	Device ID. 5'h01: ZL40240	RO	01

© 2023 Microchip Technology Inc. and its subsidiaries

NOTES:

© 2023 Microchip Technology Inc. and its subsidiaries

4.0 ELECTRICAL CHARACTERISTICS

TABLE 4-1: ABSOLUTE MAXIMUM RATINGS (Note 1, Note 2, Note 3)

Parameter	Symbol	Min.	Max.	Units
Supply Voltage, 3.3V	V_{DD}/V_{DDO}	–0.5	+4.6	V
Supply Voltage, 2.5V	V_{DD}/V_{DDO}	–0.5	+4.6	V
Supply Voltage, 1.8V	V_{DDO}	–0.5	+2.5	V
Supply Voltage, 1.5V	V_{DDO}	–0.5	+2.0	V
Storage Temperature Range	T_{ST}	–55	+125.0	°C

Note 1: Exceeding these values may cause permanent damage.

2: Functional operation under these conditions is not implied.

3: Voltages are with respect to ground (GND) unless otherwise stated.

TABLE 4-2: RECOMMENDED OPERATING CONDITIONS (Note 1, Note 2)

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply Voltage, 3.3V	V_{DD}/V_{DDO}	3.135	3.300	3.465	V
Supply Voltage, 2.5V	V_{DD}/V_{DDO}	2.375	2.500	2.625	V
Supply Voltage, 1.8V	V_{DDO}	1.600	1.800	2.000	V
Supply Voltage, 1.5V	V_{DDO}	1.350	1.500	1.650	V
Operating Temperature	T_A	–40.000	+25.000	+8.000	°C
Input Voltage	V_{DD-IN}	–0.300	—	V_{DD} + 0.300	V

Note 1: Voltages are with respect to ground (GND) unless otherwise stated.

2: The device supports two power supply modes (3.3V and 2.5V).

TABLE 4-3: CURRENT CONSUMPTION

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Static device current	$I_{S\_3.3V}$	—	15	18	mA	V_{DD} = 3.465V
	$I_{S\_2.5V}$	—	12	15	mA	V_{DD} = 2.625V
Device current with 25 MHz XTAL input	$I_{DD\_XTAL\_3.3V}$	—	24	27	mA	V_{DD} = 3.465V
	$I_{DD\_XTAL\_2.5V}$	—	18	20	mA	V_{DD} = 2.625V
Dynamic current per output (f = 100MHz), Note 1, Note 2 Needs to be scaled for different frequencies by f/100 MHz, Driving Strength = 1 (registers 0x09, 0x0A)	$I_{DD\_3.3V}$	—	4.2	4.7	mA	V_{DD} = 3.465V
	$I_{DD\_2.5V}$	—	3.0	3.5	mA	V_{DD} = 2.625V
	$I_{DD\_1.8V}$	—	2.1	2.4	mA	V_{DD} = 2.000V
	$I_{DD\_1.5V}$	—	1.6	1.8	mA	V_{DD} = 1.650V
Dynamic current per output (f = 100MHz), Note 1, Note 2 Needs to be scaled for different frequencies by f/100 MHz, Driving Strength = 0 (registers 0x09, 0x0A)	$I_{DD\_3.3V}$	—	2.3	3.0	mA	V_{DD} = 3.465V
	$I_{DD\_2.5V}$	—	1.7	1.8	mA	V_{DD} = 2.625V
	$I_{DD\_1.8V}$	—	1.2	1.3	mA	V_{DD} = 2.000V
	$I_{DD\_1.5V}$	—	0.9	1.0	mA	V_{DD} = 1.650V

Note 1: Needs to be scaled for different frequencies by f/100 MHz.

2: To calculate total power consumption use following formula: $P = (I_S + I_{DD\_XTAL}) \times V_{DD} + (I_{DDC} + I_{DD} \times n \times f/100\ MHz + V_{DDO} \times C_{LOAD} \times f \times n) \times V_{DDO}$, where I_{DD_XTAL}: should be set to zero if XTAL is not used or Is should be set to zero if XTAL is used. Also, n = number of active outputs; f = frequency of the clock; C_{LOAD} = capacitive load driven by an output.

3: This current is consumed by device whenever one or more outputs are enabled. It is independent of the number of active outputs.

© 2023 Microchip Technology Inc. and its subsidiaries

TABLE 4-3: CURRENT CONSUMPTION (CONTINUED)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Common output current, Note 3	$I_{DD\_3.3V}$	—	3.8	4.8	mA	V_{DD} = 3.465V
	$I_{DD\_2.5V}$	—	1.9	2.4	mA	V_{DD} = 2.625V
	$I_{DD\_1.8V}$	—	1.2	1.5	mA	V_{DD} = 2.000V
	$I_{DD\_1.5V}$	—	1.0	1.3	mA	V_{DD} = 1.650V

Note 1: Needs to be scaled for different frequencies by f/100 MHz.

2: To calculate total power consumption use following formula: $P = (I_S + I_{DD\_XTAL}) \times V_{DD} + (I_{DDC} + I_{DD} \times n \times f/100\ MHz + V_{DDO} \times C_{LOAD} \times f \times n) \times V_{DDO}$, where I_{DD_XTAL}: should be set to zero if XTAL is not used or Is should be set to zero if XTAL is used. Also, n = number of active outputs; f = frequency of the clock; C_{LOAD} = capacitive load driven by an output.

3: This current is consumed by device whenever one or more outputs are enabled. It is independent of the number of active outputs.

TABLE 4-4: INPUT CHARACTERISTICS (Note 1, Note 2)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
CMOS high-level input voltage for SPI_CLK, SPI_CS and SPI_SDI	V_{CIH}	1.20	—	—	V	—
CMOS low-level input voltage for SPI_CLK, SPI_CS and SPI_SDI	V_{CIL}	—	—	0.45	V	—
CMOS input leakage current for SPI_CLK, SPI_CS and SPI_SDI	I_{IL}	–40	—	10	µA	VI = VDD or 0 V
Differential input common mode voltage for IN0_p/n and IN1_p/n	V_{CM}	0.5	—	V_{DD} – 0.85	V	—
Differential input voltage difference for IN0_p/n and IN1_p/n	V_{ID}	0.15	—	1.3	V	—
Differential input leakage current for IN0_p/n and IN1_p/n (includes current in pull-up and pull-down resistors)	I_{IL}	–200	—	100	µA	VI = VDD or 0 V
Single ended input high voltage for IN_0_p and IN_1_p	V_{SIH}	2	—	V_{DD} + 0.3	V	VDD = 3.3V+/-5%
		1.6	—	V_{DD} + 0.3	V	VDD = 2.5V+/-5%
Single ended input low voltage for IN_0_p and IN_1_p	V_{SIL}	–0.3	—	1.3	V	VDD = 3.3V+/-5%
		–0.3	—	0.9	V	VDD = 2.5V+/-5%
Input frequency	f_{IN}	0	—	250	MHz	—
Input duty cycle	DC	35	—	65	%	@250MHz; for lower frequencies duty cycle can be scaled proportionally
Input slew rate	slew	—		—	V/ns	—
Input pull-up/pull-down resistance	R_{PU}/R_{PD}	—		—	kΩ	—
Input pull-down resistance (INx_p)	R_{PD}	—		—	kΩ	—

Note 1: Values are over recommended operating conditions.

2: Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).

© 2023 Microchip Technology Inc. and its subsidiaries

TABLE 4-5: CRYSTAL OSCILLATOR CHARACTERISTICS (Note 1)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Mode of oscillation	mode	Fundamental			—	—
Frequency	f	8	—	160	MHz	—
On chip load capacitance	C_L	0	—	21.75	pF	Programmable
On chip series resistor	R_S	0	—	312	Ω	Programmable
On chip shunt resistor	R	—	0.5	—	MΩ	—
Maximum frequency in over-drive mode, Note 2	f_{OV}	0.1	—	200	MHz	Functional, but may not meet AC parameters Minimum depends on AC coupling Capacitor (0.1 uF assumed)
Maximum frequency in bypass mode, Note 3	f_{BP}	0	—	200	MHz	

Note 1: Values are over recommended operating conditions. Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).

2: Maximum input level is 2.0V.

3: Maximum output level is V_{DD}.

TABLE 4-6: LVCMOS OUTPUT CHARACTERISTICS (Note 1)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output high voltage	V_{OH}	0.8 × V_{DDO}	—	—	V	V_{DDO} = 3.3V±5%
		0.8 × V_{DDO}	—	—	V	V_{DDO} = 2.5V±5%
		0.7 × V_{DDO}	—	—	V	V_{DDO} = 1.8V±10%
		0.7 × V_{DDO}	—	—	V	V_{DDO} = 1.5V±10%
Output low voltage	V_{OL}	—	—	0.2 × V_{DDO}	V	V_{DDO} = 3.3V±5%
		—	—	0.2 × V_{DDO}	V	V_{DDO} = 2.5V±5%
		—	—	0.3 × V_{DDO}	V	V_{DDO} = 1.8V±10%
		—	—	0.3 × V_{DDO}	V	V_{DDO} = 1.5V±10%
Output impedance	R_O	—	17	—	Ω	V_{DDO} = 3.3V
		—	21	—	Ω	V_{DDO} = 2.5V
		—	30	—	Ω	V_{DDO} = 1.8V
		—	42	—	Ω	V_{DDO} = 1.5V
Output slew rate, rise or fall (20% to 80%)	t_r, t_f	3.19	5.14	6.33	V/ns	V_{DDO} = 3.3V±5%
		1.72	3.74	4.61	V/ns	V_{DDO} = 2.5V±5%
		1.64	2.52	3.32	V/ns	V_{DDO} = 1.8V±10%
		1.20	1.96	2.54	V/ns	V_{DDO} = 1.5V±10%
Output frequency	F_O	0	—	250	MHz	—
Output duty cycle		50.26	—	53.18	%	Input. duty-cycle 50%
Output enable or disable time		—	—	2	cycle	—
Output to output skew	t_{OOSK}	—	—	27	ps	—
Device-to-device output skew	t_{DOOSK}	—	—	1.6	ns	—
Input to output delay	t_{IOD}	1.15	2.09	2.54	ns	VDD = 3.3V
		1.57	2.27	2.77	ns	VDD = 2.5V
Input multiplexer isolation	ISO	75	—	—	dB	Tested with 125 MHz clocks

Note 1: Values are over recommended operating conditions. Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V). Load 50Ω to V_{DDO}/2.

© 2023 Microchip Technology Inc. and its subsidiaries

TABLE 4-7: LVCMOS OUTPUT ADDITIVE JITTER AND PHASE NOISE (Note 1)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
System level additive jitter, Note 2		—	17	—	fs – RMS	V_{DD} = 3.3V, V_{DDO} = 3.3V f_{in} = 125 MHz, single ended input
		—	31	—	fs – RMS	V_{DD} = 2.5V, V_{DDO} = 1.5V to 2.5V f_{in} = 125 MHz, single ended input
		—	22	—	fs – RMS	V_{DD} = 3.3V, V_{DDO} = 3.3V f_{in} = 125 MHz, differential input
		—	37	—	fs – RMS	V_{DD} = 2.5V, V_{DDO} = 1.5V to 2.5V f_{in} = 125 MHz, differential input
Additive jitter, Note 3, Note 4		—	45.18	93.11	fs – RMS	V_{DD} = 3.3V, V_{DDO} = 3.3V f_{in} = 125 MHz, single ended input
		—	80.46	126.92	fs – RMS	V_{DD} = 2.5V, V_{DDO} = 1.5V to 2.5V f_{in} = 125 MHz, single ended input
		—	39.95	68.98	fs – RMS	V_{DD} = 3.3V, V_{DDO} = 3.3V f_{in} = 125 MHz, differential input
		—	67.18	117.26	fs – RMS	V_{DD} = 2.5V, V_{DDO} = 1.5V to 2.5V f_{in} = 125 MHz, differential input
Phase noise floor (VDD = 3.3V, VDDO = 3.3V)		—	–145.08	–138.67	dBc/Hz	@10 kHz, f_{in} = 125 MHz, single ended input
		—	–152.46	–145.82	dBc/Hz	@100 kHz, f_{in} = 125 MHz, single ended input
		—	–160.67	–155.66	dBc/Hz	@1 MHz, f_{in} = 125 MHz, single ended input
		—	–162.66	–160.55	dBc/Hz	@10 MHz, f_{in} = 125 MHz, single ended input
		—	–162.71	–160.19	dBc/Hz	@20 MHz, f_{in} = 125 MHz, single ended input
		—	–145.34	–137.83	dBc/Hz	@10 kHz, f_{in} = 125 MHz, single ended input
		—	–152.60	–146.93	dBc/Hz	@100 kHz, f_{in} = 125 MHz, single ended input
		—	–161.06	–156.99	dBc/Hz	@1 MHz, f_{in} = 125 MHz, single ended input
		—	–163.22	–160.84	dBc/Hz	@10 MHz, f_{in} = 125 MHz, single ended input
		—	–163.38	–161.42	dBc/Hz	@20 MHz, f_{in} = 125 MHz, single ended input

Note 1: Values are over recommended operating conditions. Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).

2: System level additive jitter is calculated as $J_{RMS\_SYS\_AJ} = J_{RMS\_OUT} - J_{RMS\_IN}$.

3: Additive jitter is calculated as $J_{RMS\_\_AJ} = \text{sqrt}\ (J_{RMS\_OUT}^2 - J_{RMS\_IN}^2)$ where jitter is integrated in 12 kHz to 20 MHz band.

4: Tester measures jitter at 156.25 MHz. Since this frequency won't appear in the data sheet, it should be removed from the PPGT. Data sheet jitter is guaranteed by lab char. The ATE jitter measurement will be used to screen outliers only, with limits based on ATE distribution.

© 2023 Microchip Technology Inc. and its subsidiaries

TABLE 4-7: LVCMOS OUTPUT ADDITIVE JITTER AND PHASE NOISE (Note 1) (CONTINUED)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Phase noise floor (VDD = 2.5V, VDDO = 2.5V)		—	–139.93	–134.59	dBc/Hz	@10 kHz, f_{in} = 125 MHz, single ended input
		—	–147.22	–144.21	dBc/Hz	@100 kHz, f_{in} = 125 MHz, single ended input
		—	–157.11	–154.78	dBc/Hz	@1 MHz, f_{in} = 125 MHz, single ended input
		—	–160.58	–158.21	dBc/Hz	@10 MHz, f_{in} = 125 MHz, single ended input
		—	–160.78	–158.19	dBc/Hz	@20 MHz, f_{in} = 125 MHz, single ended input
		—	–141.69	–134.26	dBc/Hz	@10 kHz, f_{in} = 125 MHz, single ended input
		—	–149.19	–144.73	dBc/Hz	@100 kHz, f_{in} = 125 MHz, single ended input
		—	–158.66	–156.22	dBc/Hz	@1 MHz, f_{in} = 125 MHz, single ended input
		—	–161.60	–159.32	dBc/Hz	@10 MHz, f_{in} = 125 MHz, single ended input
		—	–161.85	–159.36	dBc/Hz	@20 MHz, f_{in} = 125 MHz, single ended input

Note 1: Values are over recommended operating conditions. Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V).

2: System level additive jitter is calculated as $J_{RMS\_SYS\_AJ} = J_{RMS\_OUT} - J_{RMS\_IN}$.

3: Additive jitter is calculated as $J_{RMS\_\_AJ} = \text{sqrt}\ (J_{RMS\_OUT}^2 - J_{RMS\_IN}^2)$ where jitter is integrated in 12 kHz to 20 MHz band.

4: Tester measures jitter at 156.25 MHz. Since this frequency won't appear in the data sheet, it should be removed from the PPGT. Data sheet jitter is guaranteed by lab char. The ATE jitter measurement will be used to screen outliers only, with limits based on ATE distribution.

© 2023 Microchip Technology Inc. and its subsidiaries

TABLE 4-8: LVCMOS OUTPUT JITTER PHASE NOISE WITH 25 MHZ XTAL (Note 1)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Jitter RMS in 12 kHz to 20 MHz band		—	72.63	—	fs	V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	87.59	—	fs	V_{DD} = 2.5V; V_{DDO} = 2.5V
Phase noise floor		—	–75.96	—	dBc/Hz	@10 Hz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–107.50	—	dBc/Hz	@100 Hz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–132.34	—	dBc/Hz	@1 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–157.36	—	dBc/Hz	@10 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–165.82	—	dBc/Hz	@100 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–168.85	—	dBc/Hz	@1 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–168.88	—	dBc/Hz	@5 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–70.52	—	dBc/Hz	@10 Hz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–102.60	—	dBc/Hz	@100 Hz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–129.14	—	dBc/Hz	@1 kHz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–153.93	—	dBc/Hz	@10 kHz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–164.00	—	dBc/Hz	@100 kHz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–167.34	—	dBc/Hz	@1 MHz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–167.41	—	dBc/Hz	@5 MHz, V_{DD} = 2.5V; V_{DDO} = 2.5V

Note 1: Values are over recommended operating conditions. Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V). XTAL frequency is 25 MHz.

TABLE 4-9: LVCMOS OUTPUT JITTER PHASE NOISE WITH 125 MHZ XTAL (Note 1)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Jitter RMS in 12 kHz to 20 MHz band		—	48.70	—	fs	VDD = 3.3V, VDDO = 3.3V
Phase noise floor		—	66.69	—	fs	VDD = 2.5V; VDDO = 2.5V
		—	–54.84	—	dBc/Hz	@10 Hz , V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–83.69	—	dBc/Hz	@100 Hz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–122.61	—	dBc/Hz	@1 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–145.38	—	dBc/Hz	@10 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–154.19	—	dBc/Hz	@100 kHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–163.44	—	dBc/Hz	@1 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–163.88	—	dBc/Hz	@5 MHz, V_{DD} = 3.3V, V_{DDO} = 3.3V
		—	–54.21	—	dBc/Hz	@10 Hz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–82.60	—	dBc/Hz	@100 Hz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–119.11	—	dBc/Hz	@1 kHz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–140.96	—	dBc/Hz	@10 kHz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–152.05	—	dBc/Hz	@100 kHz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–160.86	—	dBc/Hz	@1 MHz, V_{DD} = 2.5V; V_{DDO} = 2.5V
		—	–161.44	—	dBc/Hz	@5 MHz, V_{DD} = 2.5V; V_{DDO} = 2.5V

Note 1: Values are over recommended operating conditions. Values are over all two power supply modes (VDD = 3.3V and VDD = 2.5V). XTAL frequency is 125 MHz.

© 2023 Microchip Technology Inc. and its subsidiaries

TABLE 4-10: AC ELECTRICAL CHARACTERISTICS (Note 1) - SPI (SERIAL PERIPHERAL INTERFACE) TIMING

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
sck period		124	—	—	ns	See Figure 4-1 and Figure 4-2
sck pulse width low		62	—	—	ns	
sck pulse width high		62	—	—	ns	
si setup (write) from sck rising edge		10	—	—	ns	
si hold (write) from sck rising edge		10	—	—	ns	
so delay (read) from sck falling edge		—	—		ns	
cs_b to output high impedance		—	—		ns	
cs_b setup from sck falling edge (LSB first)		20	—	—	ns	See Figure 4-1
cs_b hold from sck rising edge (LSB first)		10	—	—	ns	
cs_b setup from sck rising edge (MSB first)		20	—	—	ns	See Figure 4-2
cs_b hold from sck falling edge (MSB first)		10	—	—	ns	

Note 1: Values are over recommended operating conditions. For LSB first mode timing diagram, refer to Figure 4-1. For MSB first mode timing diagram, refer to Figure 4-2. Values shown are proposed for the data sheet, these values are to be confirmed.

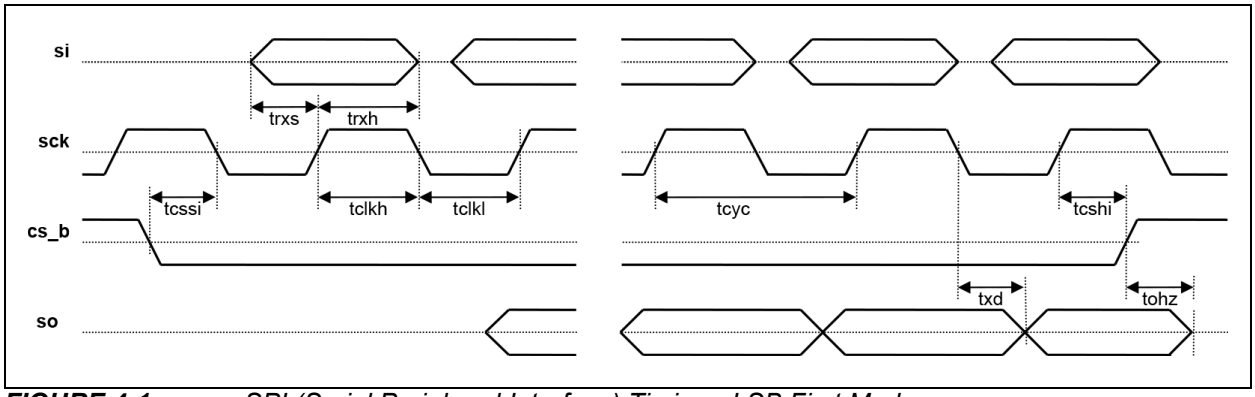


FIGURE 4-1: *SPI (Serial Peripheral Interface) Timing - LSB First Mode.*

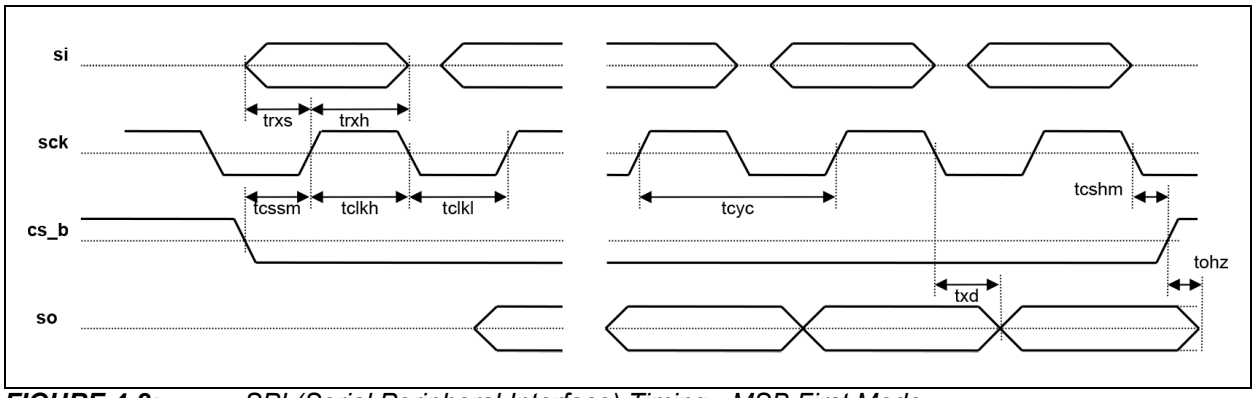


FIGURE 4-2: *SPI (Serial Peripheral Interface) Timing - MSB First Mode.*

© 2023 Microchip Technology Inc. and its subsidiaries

TABLE 4-11: 5 MM × 5 MM VQFN PACKAGE THERMAL PROPERTIES

Parameter	Symbol	Conditions	Value	Units
Maximum ambient temperature	T_A	—	85	°C
Maximum junction temperature	$T_{J(MAX)}$	—	125	°C
Junction to ambient thermal resistance, Note 1	θ_{JA}	Still air	26.8	°C/W
		1 m/s airflow	21.8	°C/W
		2.5 m/s airflow	19.9	°C/W
Junction to board thermal resistance	θ_{JB}	—	10.8	°C/W
Junction to case thermal resistance	θ_{JC}	—	19.5	°C/W
Junction to pad thermal resistance, Note 2	θ_{JP}	Still air	6.5	°C/W
Junction to top-center thermal characterization parameter	ψ_{JT}	Still air	0.6	°C/W

Note 1: θ_{JA} is the thermal resistance from junction to ambient when the package is mounted on a 4-layer JEDEC standard test board and dissipating maximum power.

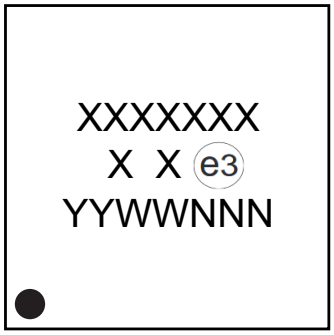
2: θ_{JP} is the thermal resistance from junction to the center exposed pad on the bottom of the package.

© 2023 Microchip Technology Inc. and its subsidiaries

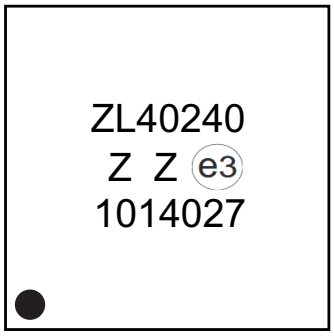
5.0 PACKAGE OUTLINE

5.1 Package Marking Information

32-Lead QFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

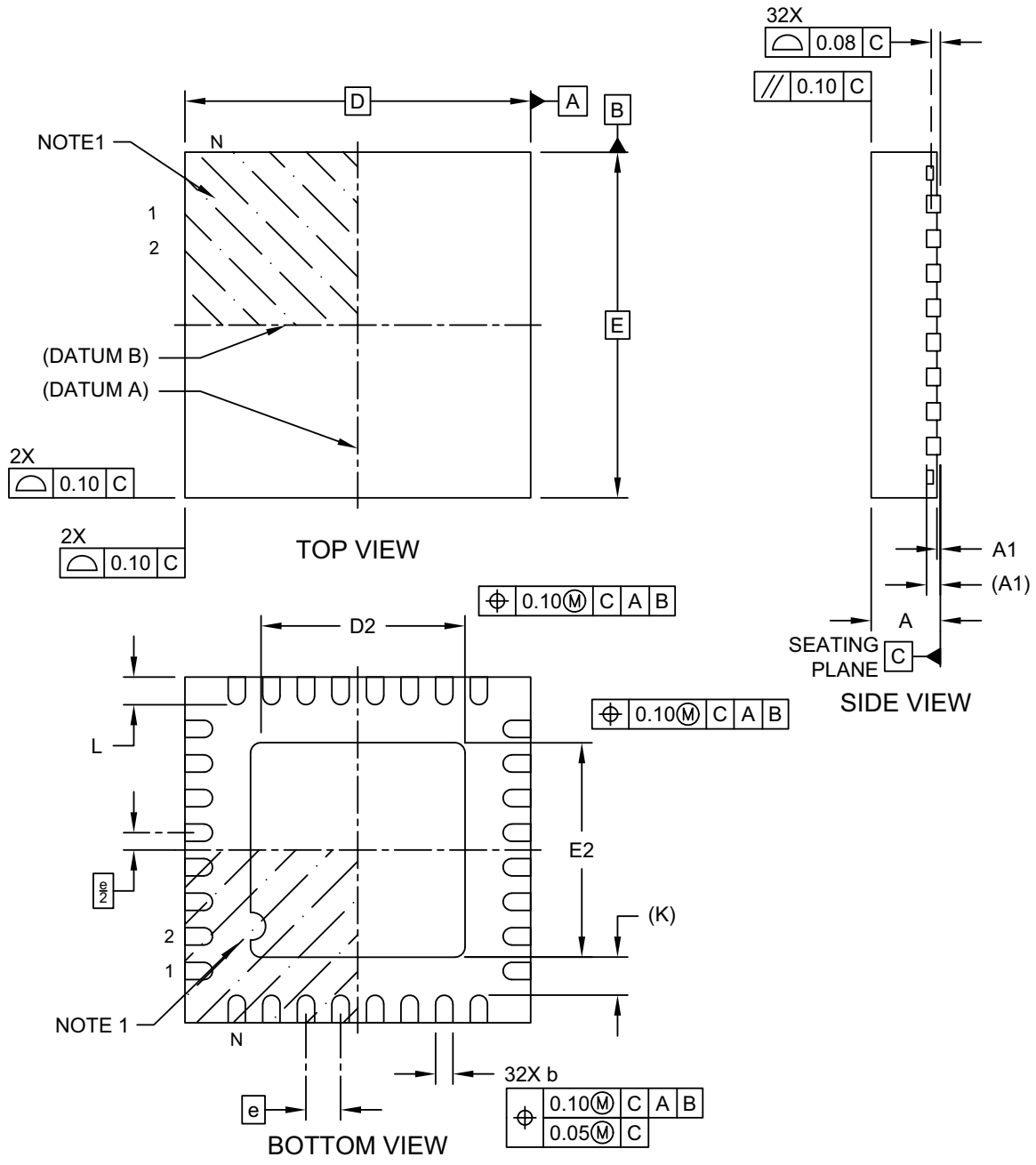
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

© 2023 Microchip Technology Inc. and its subsidiaries

32-Lead 5 mm x 5 mm VQFN Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

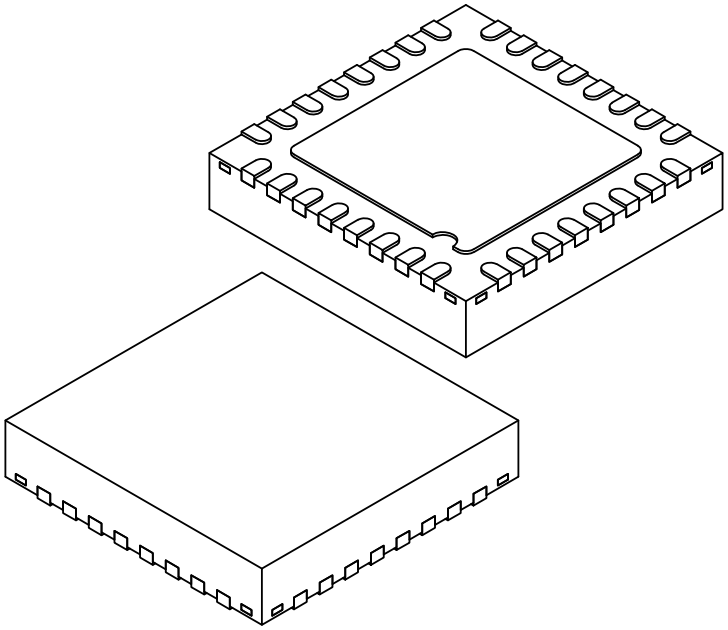


Microchip Technology Drawing C04-25400 Rev A Sheet 1 of 2

© 2023 Microchip Technology Inc. and its subsidiaries

32-Lead 5 mm x 5 mm VQFN Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.00	3.10	3.20
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.00	3.10	3.20
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	–	–

Notes:

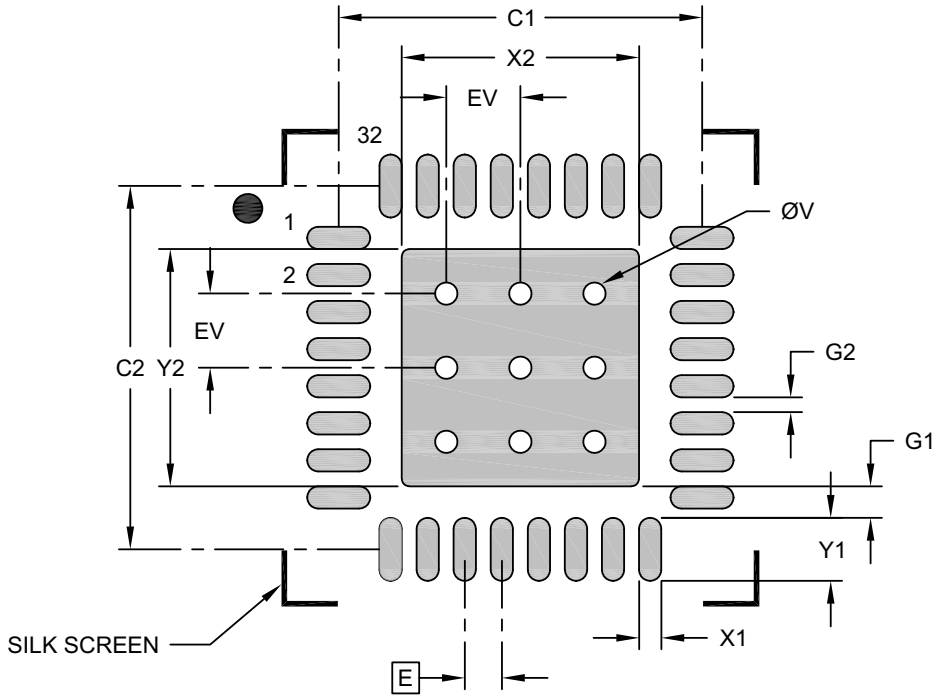
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25400 Rev A Sheet 2 of 2

© 2023 Microchip Technology Inc. and its subsidiaries

32-Lead 5 mm x 5 mm VQFN Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.20
Optional Center Pad Length	Y2			3.20
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.85
Contact Pad to Center Pad (X32)	G1	0.23		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27400 Rev A

© 2023 Microchip Technology Inc. and its subsidiaries

NOTE:

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20006782A (11-27-23)	Various	Converted Microsemi data sheet ZL40240 to Microchip DS20006782A. Updated Figure 2-9 as requested by Applications. Minor text changes throughout.

© 2023 Microchip Technology Inc. and its subsidiaries

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Device	X	X	X	X
Part Number	Chip Carrier Type	Package	Media Type	Finish

Device:	ZL40240: Ten LVCMOS Output Low Additive Jitter Fanout Buffer
Chip Carrier Type:	L = Leadless Chip Carrier
Package:	D = 32-Lead 5 mm x 5 mm VQFN
Media Type:	G = 490/Tray F = 4,000/Reel
Finish:	1 = Pb Free with Matte Sn Lead Finish, RoHS e3 Compliant

Examples:

a) ZL40240LDG1:

Ten LVCMOS Output Low Additive Jitter Fanout Buffer, Leadless Chip Carrier, 32-Lead 5 mm x 5 mm VQFN, 490/Tray, Pb Free with Matte Sn Lead Finish, RoHS e3 Compliant

b) ZL40240LDF1:

Ten LVCMOS Output Low Additive Jitter Fanout Buffer, Leadless Chip Carrier, 32-Lead 5 mm x 5 mm VQFN, 4,000/Reel, Pb Free with Matte Sn Lead Finish, RoHS e3 Compliant

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

© 2023 Microchip Technology Inc. and its subsidiaries

NOTES:

© 2023 Microchip Technology Inc. and its subsidiaries

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable" Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at https://www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet- Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, KoD, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2023, Microchip Technology Incorporated and its subsidiaries.

All Rights Reserved.

ISBN: 978-1-6683-3527-7

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

© 2023 Microchip Technology Inc. and its subsidiaries

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Microchip:

ZL40240LDG1 ZL40240LDF1