

Description

The US5D306 is a 2.1-GHz, 6-output differential high-performance clock fanout buffer.

The input clock can be selected from two differential inputs or one crystal input. The selected input clock is distributed to two banks of 3 differential outputs and one LVCMOS output. Both differential output banks can be independently configured as LVPECL, LVDS, or HCSL drivers, or disabled. The LVCMOS output has a synchronous enable input for runt-pulse-free operation when enabled or disabled. The outputs are at a defined level when inputs are open.

The internal oscillator circuit is automatically disabled if the crystal input is not selected. The crystal pin can be driven by a single-ended clock.

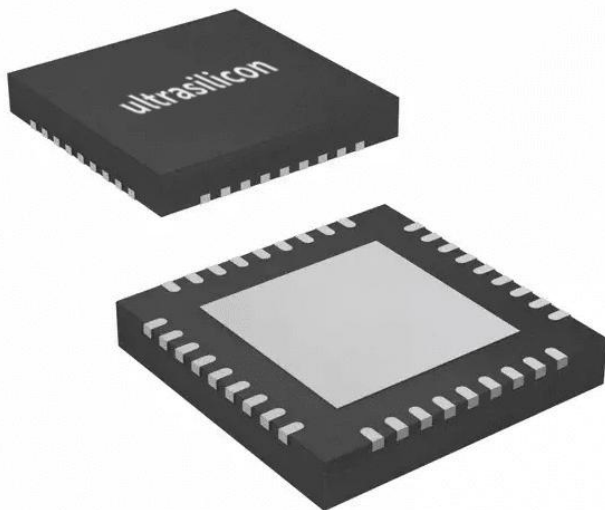
The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.

Applications

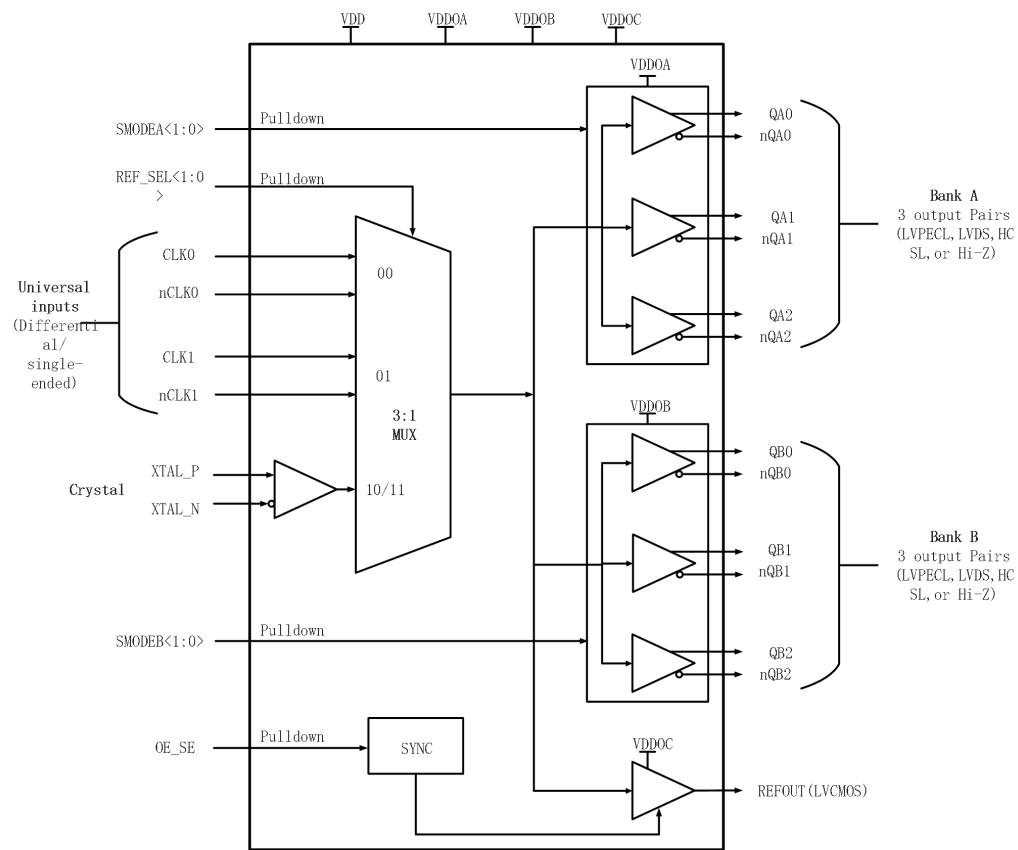
- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Ethernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH, CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express (PCIe 3.0, 4.0, 5.0)
- Remote Radio Units and Baseband Units

Features

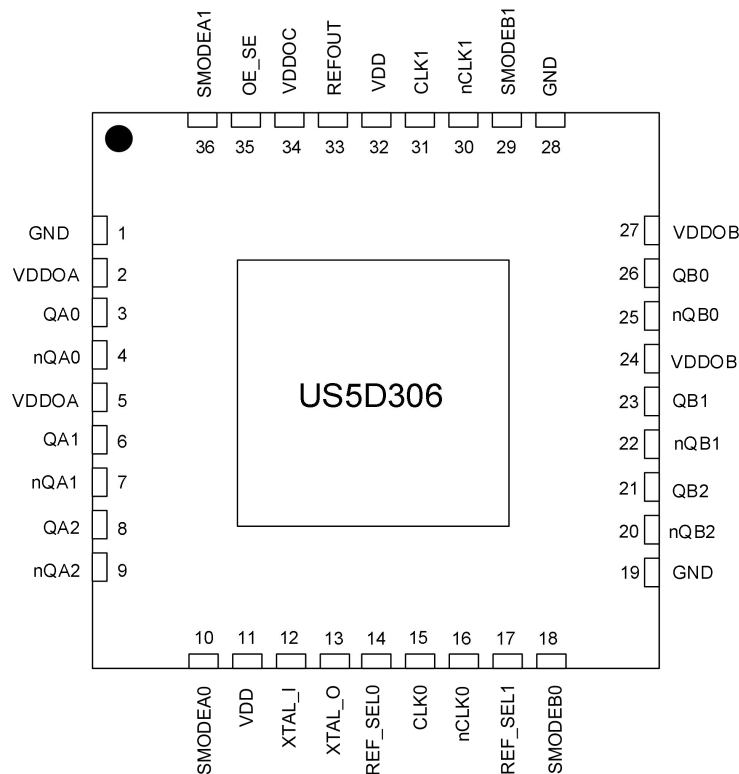
- Two differential reference clock input pairs
- Differential input pairs can accept the following differential input levels: LVPECL, LVDS, HCSL, HSTL or Single Ended
- Crystal Input accepts 10MHz to 40MHz Crystal or Single Ended Clock
- Maximum Output Frequency
 - LVPECL - 2.1GHz
 - LVDS - 2.1GHz
 - HCSL - 250MHz
 - LVCMOS - 250MHz
- Two banks, each has three differential output pairs that can be configured as LVPECL or LVDS or HCSL or HiZ
- One single-ended reference output with synchronous enable to avoid clock glitch
- Output skew: 20ps (typical)
(Bank A and Bank B at the same output level)
- Part-to-part skew: 200ps (typical)
- Additive RMS phase jitter @ 156.25MHz:
 - 12.5 fs RMS (10kHz - 1 MHz), typical @ 3.3V/ 3.3V
 - 50.5 fs RMS (10kHz - 20MHz), typical @ 3.3V/ 3.3V
- Supply voltage modes:
 - V_{DD}/V_{DDO}
 - 3.3V/3.3V
 - 3.3V/2.5V
 - 2.5V/2.5V
- Industrial Temperature Range: -40°C to 85°C
- Compatible with Imk00306
- Available in a 36-pin, 6mm*6mm WQFN package



Block Diagram



Pin Assignment for 6mm x 6mm 36-Lead WQFN Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions¹

| Number | Name | Type | | Description |
|--------|-------------------|--------|---------------------|---|
| 1 | GND | Power | | Ground. |
| 2 | V _{DDOA} | Power | | Output supply pins for Bank QA outputs. 3.3V or 2.5V. |
| 3 | QA0 | Output | | Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 4 | nQA0 | Output | | Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 5 | V _{DDOA} | Power | | Output supply pins for Bank QA outputs. 3.3V or 2.5V. |
| 6 | QA1 | Output | | Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 7 | nQA1 | Output | | Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 8 | QA2 | Output | | Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 9 | nQA2 | Output | | Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 10 | SMODEA0 | Input | Pulldown | Output driver select for Bank A outputs. See Table 8 for function. LVCMOS/LVTTL interface levels. |
| 11 | V _{DD} | Power | | Power supply for Core and input Buffer blocks, 3.3V or 2.5V. |
| 12 | XTAL_I | Input | | Crystal oscillator interface. |
| 13 | XTAL_O | Input | | Crystal oscillator interface. |
| 14 | REF_SEL0 | Input | Pulldown | Input clock selection. LVCMOS/LVTTL interface levels. See Table 3 for function. |
| 15 | CLK0 | Input | Pulldown | Non-inverting differential clock. Internally biased to ground. |
| 16 | nCLK0 | Input | Pullup/ Pulldown | Inverting differential clock. Internally biased to 0.5V _{DD} . |
| 17 | REF_SEL1 | Input | Pulldown | Input clock selection. LVCMOS/LVTTL interface levels. See Table 3 for function. |
| 18 | SMODEB0 | Input | Pulldown | Output driver select for Bank B outputs. See Table 9 for function. LVCMOS/LVTTL interface levels. |
| 19 | GND | Power | | Ground. |
| 20 | nQB2 | Output | | Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 21 | QB2 | Output | | Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 22 | nQB1 | Output | | Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 23 | QB1 | Output | | Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 24 | V _{DDOB} | Power | | Output supply pins for Bank QB outputs. 3.3V or 2.5V. |
| 25 | nQB0 | Output | | Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 26 | QB0 | Output | | Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels. |
| 27 | V _{DDOB} | Power | | Output supply pins for Bank QB outputs. 3.3V or 2.5V. |
| 28 | GND | Power | | Ground. |
| 29 | SMODEB1 | Input | Pulldown | Output driver select for Bank B outputs. See Table 9 for function. LVCMOS/LVTTL interface levels. |
| 30 | nCLK1 | Input | Pullup/ Pulldown | Inverting differential clock. Internally biased to 0.5V _{DD} . |
| 31 | CLK1 | Input | Pulldown | Non-inverting differential clock. Internally biased to ground. |
| 32 | V _{DD} | Power | | Power supply for Core and input Buffer blocks, 3.3V or 2.5V. |

Table 1: Pin Descriptions¹ (Continued)

| Number | Name | Type | | Description |
|--------|---------|--------|----------|---|
| 33 | REFOUT | Output | | Single-ended reference clock output. LVCMOS/LVTTL interface levels. |
| 34 | VDDOC | Power | | Output supply pin for REFOUT output. |
| 35 | OE_SE | Input | Pulldown | REFOUT output enable. LVCMOS/LVTTL interface levels. See Table 4. |
| 36 | SMODEA1 | Input | Pulldown | Output driver select for Bank A outputs. See Table 8 for function. LVCMOS/LVTTL interface levels. |
| ePad | GND_EP | Power | | Connect ePad to ground to ensure proper heat dissipation. |

NOTE 1. *Pulldown* and *Pullup* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2: Pin Characteristics

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------------|----------------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | OE_SE, SMODEx[1:0], REF_SEL[1:0] | | | 2 | | pF |
| R _{PULLDOWN} | Input Pulldown Resistor | | | | 50 | | kΩ |
| R _{PULLUP} | Input Pullup/down Resistor | nCLK0 | | | 40/40 | | kΩ |
| | | nCLK1 | | | 40/40 | | kΩ |
| C _{PD} | Power Dissipation Capacitance | REFOUT | VDDOC = 3.465V | | 5.3 | | pF |
| | | REFOUT | VDDOC = 2.625V | | 6.3 | | pF |
| R _{OUT} | Output Impedance | REFOUT | VDDOC = 3.3V | | 50 | | Ω |
| | | REFOUT | VDDOC = 2.5V | | 60 | | Ω |

Function Tables

Table 3: REF_SELx Function Table

| Control Input | Selected Input Reference Clock |
|---------------|--------------------------------|
| REF_SEL[1:0] | |
| 00 (default) | CLK0, nCLK0 |
| 01 | CLK1, nCLK1 |
| 10 | XTAL |
| 11 | XTAL |

Table 4: OE_SE Function Table¹

| OE_SE | REFOUT |
|-------------|----------------|
| 0 (default) | High-Impedance |
| 1 | Enabled |

NOTE 1. Synchronous output enable to avoid clock glitch.

Table 5: Input/Output Operation Table, OE_SE

| Input Status | | | Output State |
|--------------|---------------|--------------------------------------|---------------------------|
| OE_SE | REF_SEL [1:0] | CLKx and nCLKx | REFOUT |
| 0 (default) | Don't care | Don't Care | High Impedance |
| 1 | 10 or 11 | Don't Care | Fanout crystal oscillator |
| 1 | 00 (default) | CLK0 and nCLK0 are both open circuit | Logic Low |
| | | CLK0 and nCLK0 are tied to ground | Logic Low |
| | | CLK0 is high, nCLK0 is low | Logic High |
| | | CLK0 is low, nCLK0 is high | Logic Low |
| 1 | 01 | CLK1 and nCLK1 are both open circuit | Logic Low |
| | | CLK1 and nCLK1 are tied to ground | Logic Low |
| | | CLK1 is high, nCLK1 is low | Logic High |
| | | CLK1 is low, nCLK1 is high | Logic Low |

Table 6: Input/Output Operation Table, SMOEA[1:0]

| Input Status | | | Output State |
|--------------|--------------|--------------------------------------|----------------------------------|
| SMOEA[1:0] | REF_SEL[1:0] | CLKx and nCLKx | QA[3:0], nQA[3:0] |
| 11 | Don't care | Don't Care | High Impedance |
| 00, 01 or 10 | 10 or 11 | Don't Care | Fanout crystal oscillator |
| 00, 01 or 10 | 00 (default) | CLK0 and nCLK0 are both open circuit | QA[3:0] = Low nQA[3:0] = High |
| | | CLK0 and nCLK0 are tied to ground | QA[3:0] = Low nQA[3:0] = High |
| | | CLK0 is high, nCLK0 is low | QA[3:0] = High nQA[3:0] = Low |
| | | CLK0 is low, nCLK0 is high | QA[3:0] = Low nQA[3:0] = High |
| 00, 01 or 10 | 01 | CLK1 and nCLK1 are both open circuit | QA[3:0] = Low nQA[3:0] = High |
| | | CLK1 and nCLK1 are tied to ground | QA[3:0] = Low nQA[3:0] = High |
| | | CLK1 is high, nCLK1 is low | QA[3:0] = High nQA[3:0] = Low |
| | | CLK1 is low, nCLK1 is high | QA[3:0] = Low nQA[3:0] = High |

Table 7: Input/Output Operation Table, SMODEB[1:0]

| Input Status | | | Output State |
|--------------|--------------|--------------------------------------|----------------------------------|
| SMODEB[1:0] | REF_SEL[1:0] | CLKx and nCLKx | QB[3:0], nQB[3:0] |
| 11 | Don't care | Don't Care | High Impedance |
| 00, 01 or 10 | 10 or 11 | Don't Care | Fanout crystal oscillator |
| 00, 01 or 10 | 00 (default) | CLK0 and nCLK0 are both open circuit | QB[3:0] = Low nQB[3:0] = High |
| | | CLK0 and nCLK0 are tied to ground | QB[3:0] = Low nQB[3:0] = High |
| | | CLK0 is high, nCLK0 is low | QB[3:0] = High nQB[3:0] = Low |
| | | CLK0 is low, nCLK0 is high | QB[3:0] = Low nQB[3:0] = High |
| 00, 01 or 10 | 01 | CLK1 and nCLK1 are both open circuit | QB[3:0] = Low nQB[3:0] = High |
| | | CLK1 and nCLK1 are tied to ground | QB[3:0] = Low nQB[3:0] = High |
| | | CLK1 is high, nCLK1 is low | QB[3:0] = High nQB[3:0] = Low |
| | | CLK1 is low, nCLK1 is high | QB[3:0] = Low nQB[3:0] = High |

Table 8: Output Level Selection Table, QA[0:4], nQA[0:4]

| SMODEA1 | SMODEA0 | Output Type |
|---------|---------|------------------|
| 0 | 0 | LVPECL (default) |
| 0 | 1 | LVDS |
| 1 | 0 | HCSL |
| 1 | 1 | HiZ |

Table 9: Output Level Selection Table, QB[0:4], nQB[0:4]

| SMODEB1 | SMODEB0 | Output Type |
|---------|---------|------------------|
| 0 | 0 | LVPECL (default) |
| 0 | 1 | LVDS |
| 1 | 0 | HCSL |
| 1 | 1 | HiZ |

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied.

| Item | Rating |
|---------------------------------|------------------------------|
| V_{DD}, V_{DDOX}^1 | 4.6V |
| V_{IN} | -0.3V to $V_{DDOX}^1 + 0.3V$ |
| T_J : Junction Temperature | 150°C |
| T_{STG} : Storage Temperature | -65°C to 150°C |

NOTE 1. V_{DDOX} denotes V_{DDOA} , V_{DDOB} and V_{DDOC} .

ESD Ratings

| | | Max | Unit |
|-----------------------------------|---|-------|------|
| V(ESD) Electrostatic discharge | Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017 | ±2500 | V |
| | Machine model (MM), JEDEC Std. JESD22-A115-C | ±250 | |
| | Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018 | ±750 | |

Latch up

| | | Max | Unit |
|----------|---------------------------|------|------|
| Latch up | I-test, JEDEC STD JESD78E | ±200 | mA |
| | V-test, JEDEC STD JESD78E | 4.6 | V |

Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------|---|------------------|------------|------------------|------|
| T_A | Ambient air temperature | -40 | | 85 | °C |
| T_J | Junction temperature | | | 125 | °C |
| V_{DD} | Power supply for Core and input Buffer blocks | 3.3-5% 2.5-5% | 3.3 2.5 | 3.3+5% 2.5+5% | V |
| V_{DDOX}^1 | Power supply for Bank QA or QB or REFOUT | 3.3-5% 2.5-5% | 3.3 2.5 | 3.3+5% 2.5+5% | V |

NOTE 1. V_{DDOX} denotes V_{DDOA} , V_{DDOB} and V_{DDOC} .

Electrical Characteristics

Unless otherwise specified: VDD = 3.3 V \pm 5%, VDDO = 3.3 V \pm 5%, 2.5 V \pm 5%, -40 °C \leq T_A \leq 85 °C, CLK_{in} driven differentially, input slew rate \geq 3 V/ns. Typical values represent most likely parametric norms at VDD = 3.3 V, VDDO = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.⁽¹⁾

| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|--|---|--|------|-------|-----|------|
| Current Consumption ⁽²⁾ | | | | | | |
| I _{DD_CORE} | Core Supply Current, All Outputs Disabled | CLK_X selected | | 11.5 | | mA |
| | | XTAL selected | | 21.5 | | mA |
| I _{DD_PECL} | Additive Core Supply Current, Per LVPECL Bank Enabled | | | 31.7 | | mA |
| I _{DD_LVDS} | Additive Core Supply Current, Per LVDS Bank Enabled | | | 39.5 | | mA |
| I _{DD_HCSL} | Additive Core Supply Current, Per HCSL Bank Enabled | | | 14.8 | | mA |
| I _{DD_CMOS} | Additive Core Supply Current, LVCMOS Output Enabled | | | 3.4 | | mA |
| I _{DDO_PECL} | Additive Output Supply Current, Per LVPECL Bank Enabled | Includes Output Bank Bias and Load Currents, R _T = 50 Ω to VDDO - 2V on all outputs in bank | | 188 | | mA |
| I _{DDO_LVDS} | Additive Output Supply Current, Per LVDS Bank Enabled | | | 42 | | mA |
| I _{DDO_HCSL} | Additive Output Supply Current, Per HCSL Bank Enabled | Includes Output Bank Bias and Load Currents, R _T = 50 Ω on all outputs in bank | | 118.5 | | mA |
| I _{DDO_CMOS} | Additive Output Supply Current, LVCMOS Output Enabled | 200 MHz, C _L = 5 pF | | 1.6 | | mA |
| Power Supply Ripple Rejection (PSRR) | | | | | | |
| PSRR _{PECL} | Ripple-Induced Phase Spur Level ⁽³⁾ Differential LVPECL Output | 100 kHz, 100 mVpp Ripple Injected on VDDO, VDDO = 3.3 V 156.25 MHz | | -65 | | dBc |
| PSRR _{HCSL} | Ripple-Induced Phase Spur Level ⁽³⁾ Differential HCSL Output | | | -76 | | dBc |
| PSRR _{LVDS} | Ripple-Induced Phase Spur Level ⁽³⁾ Differential LVDS Output | | | -112 | | dBc |
| CMOS Control Inputs (REF_SEL[1:0], SMODEA[1:0],SMODEB[1:0], OE_SE) | | | | | | |
| V _{IH} | High-Level Input Voltage | | 1.65 | | VDD | V |
| V _{IL} | Low-Level Input Voltage | | GND | | 1.5 | V |
| I _{IH} | High-Level Input Current | V _{IH} = VDD, Internal pull-down resistor | | | 67 | μA |
| I _{IL} | Low-Level Input Current | V _{IL} = 0 V, Internal pull-down resistor | -5 | 0.2 | | μA |

- (1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) See *Power Considerations* for more information on current consumption and power dissipation calculations.
- (3) Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the VDDO supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows: DJ (ps pk-pk) = $[(2 * 10^{(PSRR / 20)}) / (\pi * f_{CLK})] * 1E12$

Electrical Characteristics(continued)

Unless otherwise specified: VDD = 3.3 V ± 5%, VDDO = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T_A ≤ 85 °C, CLK_{in} driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at VDD = 3.3 V, VDDO = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.⁽¹⁾

| Parameter | | Test Conditions | | Min | Typ | Max | Unit |
|---|--|---|------------------------------|--------|-----------|-----|-----------------|
| Universal Clock Inputs (CLK0/nCLK0, CLK1/nCLK1) | | | | | | | |
| f _{CLKin} | Input Frequency Range ⁽⁴⁾ | Functional up to 2.1 GHz Output frequency range and timing specified per output type (refer to LVPECL, LVDS, HCSL, LVCMOS output specifications) | | DC | 2.1 | | GHz |
| V _{IHD} | Differential Input High Voltage | CLKin driven differentially | | VDD | | | V |
| V _{ILD} | Differential Input Low Voltage | | | GND | | | V |
| V _{ID} | Differential Input Voltage Swing ⁽⁵⁾ | | | 0.15 | 1.3 | | V |
| V _{CMD} | Differential Input Common Mode Voltage | V _{ID} = 150 mV | | 0.25 | VDD - 1.2 | | V |
| | | V _{ID} = 350 mV | | 0.25 | VDD - 1.1 | | |
| | | V _{ID} = 800 mV | | 0.25 | VDD - 0.9 | | |
| V _{IH} | Single-Ended Input High Voltage | CLK _X driven single-ended (AC or DC coupled), nCLK _X AC coupled to GND or externally biased within V _{CM} range | | VDD | | | V |
| V _{IL} | Single-Ended Input Low Voltage | | | GND | | | V |
| V _{I_SE} | Single-Ended Input Voltage Swing ⁽⁶⁾⁽⁷⁾ | | | 0.3 | 2 | | V _{pp} |
| V _{CM} | Single-Ended Input Common Mode Voltage | | | 0.25 | VDD - 1.2 | | V |
| ISO _{MUX} | Mux Isolation, CLK0 to CLK1 | f _{OFFSET} > 50 kHz, P _{CLK_X} = 0 dBm | f _{CLK0} = 100 MHz | -112.5 | | | dBc |
| | | | f _{CLK0} = 200 MHz | -82 | | | |
| | | | f _{CLK0} = 500 MHz | -71 | | | |
| | | | f _{CLK0} = 1000 MHz | -65 | | | |
| Crystal Interface (XTAL_I, XTAL_O) | | | | | | | |
| F _{CLK} | External Clock Frequency Range ⁽⁴⁾ | XTAL_I driven single-ended, XTAL_O floating | | 250 | | | MHz |
| F _{XTAL} | Crystal Frequency Range | Fundamental mode crystal ESR ≤ 200 Ω (10 to 30 MHz) ESR ≤ 125 Ω (30 to 40 MHz) ⁽⁸⁾ | | 10 | 40 | | MHz |
| C _{IN} | XTAL Input Capacitance | | | 4 | | | pF |

(4) Specification is ensured by characterization and is not tested in production.

(5) See V_{ID} = Differential input Voltage Swing, V_{OD} = Differential output Voltage Swing.

(6) Parameter is specified by design, not tested in production.

(7) For clock input frequency ≥ 100 MHz, CLK_X can be driven with single-ended (LVCMOS) input swing up to 3.3 V_{pp}. For clock input frequency < 100 MHz, the single-ended input swing should be limited to 2 V_{pp} max to prevent input saturation.

(8) The ESR requirements stated must be met to ensure that the oscillator circuitry has no startup issues. However, lower ESR values for the crystal may be necessary to stay below the maximum power dissipation (drive level) specification of the crystal.

Electrical Characteristics(continued)

Unless otherwise specified: VDD = 3.3 V \pm 5%, VDDO = 3.3 V \pm 5%, 2.5 V \pm 5%, -40 °C \leq T_A \leq 85 °C, CLKIn driven differentially, input slew rate \geq 3 V/ns. Typical values represent most likely parametric norms at VDD = 3.3 V, VDDO = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.⁽¹⁾

| Parameter | | Test Conditions | | Min | Typ | Max | Unit |
|------------------------|---|---|---|------------|-------------|------------|--------|
| LVPECL Outputs | | | | | | | |
| f _{CLKout_FS} | Maximum Output Frequency Full V _{OD} Swing ⁽⁴⁾ (9) | V _{OD} ≥ 600 mV, R _L = 100 Ω differential | VDDO = 3.3 V ± 5%, R _T = 160 Ω to GND | 0.8 | | | GHz |
| | | | VDDO=2.5 V ± 5%, R _T = 91 Ω to GND | 1.0 | | | |
| f _{CLKout_RS} | Maximum Output Frequency Reduced V _{OD} Swing ⁽⁴⁾ (9) | V _{OD} ≥ 400 mV, R _L = 100 Ω differential | VDDO = 3.3 V ± 5%, R _T = 160 Ω to GND | 2.1 | | | GHz |
| | | | VDDO=2.5 V ± 5%, R _T = 91 Ω to GND | 2.3 | | | |
| Jitter _{ADD} | Additive RMS Jitter, Integration Bandwidth 10 kHz to 20 MHz ⁽⁶⁾ (10)(11) | VDDO=3.3 V ± 5%: R _T = 160 Ω to GND, R _L = 100 Ω differential | CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns | 50.5 | | | fs |
| Jitter _{ADD} | Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz ⁽¹⁰⁾ | VDDO = 3.3 V, R _T = 160 Ω to GND, R _L = 100 Ω differential | CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns | 48.6 | | | fs |
| Noise Floor | Noise Floor f _{OFFSET} ≥ 10 MHz ⁽¹³⁾ (14) | VDDO = 3.3 V, R _T = 160 Ω to GND, R _L = 100 Ω differential | CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns | -162.5 | | | dBc/Hz |
| DUTY | Duty Cycle ⁽⁴⁾ | 50% input clock duty cycle | | 45% | | 55% | |
| V _{OH} | Output High Voltage | T _A = 25 °C, DC Measurement, R _T = 50 Ω toVDDO - 2 V | | VDDO - 1.2 | VDDO - 0.99 | VDDO - 0.7 | V |
| V _{OL} | Output Low Voltage | | | VDDO - 2.0 | VDDO - 1.75 | VDDO - 1.5 | V |
| V _{OD} | Output Voltage Swing ⁽⁵⁾ | | | 600 | 760 | 1000 | mV |
| t _R | Output Rise Time 20% to 80% ⁽⁶⁾ | R _T = 160 Ω to GND, Uniform transmission line up to 10 in. with 50-Ω characteristic impedance, R _L = 100 Ω differential, C _L ≤ 5 pF | | 200 | | | ps |
| t _F | Output Fall Time 80% to 20% ⁽⁶⁾ | | | 200 | | | ps |

(9) See *Typical Characteristics* for output operation over frequency.

(10) For the 156.25 MHz clock input conditions, Additive RMS Jitter (J_{ADD}) is calculated using Method : J_{ADD} = SQRT(J_{OUT}² - J_{SOURCE}²), where J_{OUT} is the total RMS jitter measured at the output driver and J_{SOURCE} is the RMS jitter of the clock source applied to CLKIn.

(11) 156.25 MHz LVDS input clock source from Epson SG3225VEN(LVDS) Low-Noise SPXO.

(12) 156.25 MHz LVPECL input clock source from Epson SG3225VEN(LVPECL) Low-Noise SPXO.

(13) The noise floor of the output buffer is measured as the far-out phase noise of the buffer. Typically this offset is \geq 10 MHz.

(14) Phase noise floor will degrade as the clock input slew rate is reduced. Compared to a single-ended clock, a differential clock input (LVPECL, LVDS) will be less susceptible to degradation in noise floor at lower slew rates due to its common mode noise rejection. However, it is recommended to use the highest possible input slew rate for differential clocks to achieve optimal noise floor performance at the device outputs.

Electrical Characteristics(continued)

Unless otherwise specified: VDD = 3.3 V \pm 5%, VDDO = 3.3 V \pm 5%, 2.5 V \pm 5%, -40 °C \leq T_A \leq 85 °C, CLKIn driven differentially, input slew rate \geq 3 V/ns. Typical values represent most likely parametric norms at VDD = 3.3 V, VDDO = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.⁽¹⁾

| Parameter | | Test Conditions | | Min | Typ | Max | Unit |
|------------------------|--|--|--|--------|------|-------|--------|
| LVDS Outputs | | | | | | | |
| f _{CLKout_FS} | Maximum Output Frequency Full V _{OD} Swing ⁽⁴⁾⁽⁹⁾ | V _{OD} ≥ 250 mV, R _L = 100 Ω differential | | 1.37 | | | GHz |
| f _{CLKout_RS} | Maximum Output Frequency Reduced V _{OD} Swing ⁽⁴⁾⁽⁹⁾ | V _{OD} ≥ 200 mV, R _L = 100 Ω differential | | 2.1 | | | GHz |
| Jitter _{ADD} | Additive RMS Jitter, Integration Bandwidth 10 kHz to 20 MHz ⁽⁶⁾⁽¹⁰⁾⁽¹¹⁾ | VDDO = 3.3 V, R _L = 100 Ω differential | CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns | 59 | | | fs |
| Jitter _{ADD} | Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz ⁽¹⁰⁾ | VDDO = 3.3 V, R _L = 100 Ω differential | CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns | 57.5 | | | fs |
| Noise Floor | Noise Floor f _{OFFSET} ≥ 10 MHz ⁽¹³⁾⁽¹⁴⁾ | VDDO = 3.3 V, R _L = 100 Ω differential | CLKin: 156.25 MHz, Slew rate ≥ 3 V/ns | -160.6 | | | dBc/Hz |
| DUTY | Duty Cycle ⁽⁴⁾ | 50% input clock duty cycle | | 45% | | 55% | |
| V _{OD} | Output Voltage Swing ⁽⁵⁾ | T _A = 25 °C, DC Measurement, R _L = 100 Ω differential | | 250 | 400 | 450 | mV |
| ΔV _{OD} | Change in Magnitude of V _{OD} for Complementary Output States | | | -50 | | 50 | mV |
| V _{OS} | Output Offset Voltage | | | 1.125 | 1.25 | 1.375 | V |
| ΔV _{OS} | Change in Magnitude of V _{OS} for Complementary Output States | | | -35 | | 35 | mV |
| t _R | Output Rise Time 20% to 80% ⁽⁶⁾ | Uniform transmission line up to 10 inches with 50-Ω characteristic impedance, R _L = 100 Ω differential, C _L ≤ 5 pF | | 200 | | | ps |
| t _F | Output Fall Time 80% to 20% ⁽⁶⁾ | | | 200 | | | ps |

Electrical Characteristics(continued)

Unless otherwise specified: VDD = 3.3 V \pm 5%, VDDO = 3.3 V \pm 5%, 2.5 V \pm 5%, -40 °C \leq T_A \leq 85 °C, CLKIn driven differentially, input slew rate \geq 3 V/ns. Typical values represent most likely parametric norms at VDD = 3.3 V, VDDO = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.⁽¹⁾

| Parameter | | Test Conditions | | Min | Typ | Max | Unit |
|-----------------------|---|--|---|------|------|-----|--------|
| HCSL Outputs | | | | | | | |
| f _{CLKout} | Output Frequency Range ⁽⁴⁾ | R _L = 50 Ω to GND, C _L ≤ 5 pF | | DC | | 250 | MHz |
| Jitter _{ADD} | Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz ⁽¹⁰⁾ | VDDO = 3.3 V, R _T = 50 Ω to GND | CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns | | 70 | | fs |
| Noise Floor | Noise Floor f _{OFFSET} ≥ 10 MHz ⁽¹³⁾ (14) | VDDO = 3.3 V, R _T = 50 Ω to GND | CLKin: 156.25 MHz, Slew rate ≥ 2.7 V/ns | | -160 | | dBc/Hz |
| DUTY | Duty Cycle ⁽⁴⁾ | 50% input clock duty cycle | | 45% | | 55% | |
| V _{OH} | Output High Voltage | T _A = 25 °C, DC Measurement, R _T = 50 Ω to GND | | 520 | 800 | 920 | mV |
| V _{OL} | Output Low Voltage | | | -150 | 0.5 | 150 | mV |
| V _{CROSS} | Absolute Crossing Voltage (4) (15) | R _L = 50 Ω to GND, C _L ≤ 5 pF | | 160 | 350 | 460 | mV |
| ΔV _{CROSS} | Total Variation of V _{CROSS} (4) (15) | | | | | 140 | mV |
| t _R | Output Rise Time 20% to 80% ⁽⁶⁾ (15) | 250 MHz, Uniform transmission line up to 10 inches with 50-Ω characteristic impedance, R _L = 50 Ω to GND, C _L ≤ 5 pF | | | 300 | 500 | ps |
| t _F | Output Fall Time 80% to 20% ⁽⁶⁾ (15) | | | | 300 | 500 | ps |

(15) AC timing parameters for HCSL or CMOS are dependent on output capacitive loading.

Electrical Characteristics(continued)

Unless otherwise specified: VDD = 3.3 V ± 5%, VDDO = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T_A ≤ 85 °C, CLK_{in} driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at VDD = 3.3 V, VDDO = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.⁽¹⁾

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------------------------------|---|--|--------------------------------------|----------|----------|
| LVC MOS Output (REFOUT) | | | | | |
| f _{CLKout} | Output Frequency Range ⁽⁴⁾ | C _L ≤ 5 pF | | DC | 300 MHz |
| Jitter _{RADD} | Additive RMS Jitter Integration Bandwidth 1 MHz to 20 MHz ⁽¹⁰⁾ | VDDO = 3.3 V, C _L ≤ 5 pF | 156.25 MHz, Input Slew rate ≥ 3 V/ns | 61 | fs |
| Noise Floor | Noise Floor f _{OFFSET} ≥ 10 MHz ⁽¹³⁾ (14) | VDDO = 3.3 V, C _L ≤ 5 pF | 156.25 MHz, Input Slew rate ≥ 3 V/ns | -160 | dBc/Hz |
| DUTY | Duty Cycle ⁽⁴⁾ | 50% input clock duty cycle | | 45% | 55% |
| V _{OH} | Output High Voltage | 1 mA load | | VDDO-0.1 | V |
| V _{OL} | Output Low Voltage | | | 0.1 | V |
| I _{OH} | Output High Current (Source) | V _O = VDDO / 2 | VDDO = 3.3 V | 28 | mA |
| | | | VDDO = 2.5 V | 20 | |
| I _{OL} | Output Low Current (Sink) | | VDDO = 3.3 V | 28 | mA |
| | | | VDDO = 2.5 V | 20 | |
| t _R | Output Rise Time 20% to 80% ⁽⁶⁾ (15) | 250 MHz, Uniform transmission line up to 10 inches with 50-Ω characteristic impedance, R _L = 50 Ω to GND, C _L ≤ 5 pF | | 225 | 400 ps |
| t _F | Output Fall Time 80% to 20% ⁽⁶⁾ (15) | | | 225 | 400 ps |
| t _{EN} | Output Enable Time ⁽¹⁶⁾ | C _L ≤ 5 pF | | | 3 cycles |
| t _{DIS} | Output Disable Time ⁽¹⁶⁾ | | | | 3 cycles |

(16) Output Enable Time is the number of input clock cycles it takes for the output to be enabled after OE_SE is pulled high. Similarly, Output Disable Time is the number of input clock cycles it takes for the output to be disabled after OE_SE is pulled low. The OE_SE signal should have an edge transition much faster than that of the input clock period for accurate measurement.

Electrical Characteristics(continued)

Unless otherwise specified: VDD = 3.3 V ± 5%,VDDO = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ T_A ≤ 85 °C, CLKin driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at VDD = 3.3 V,VDDO = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.⁽¹⁾

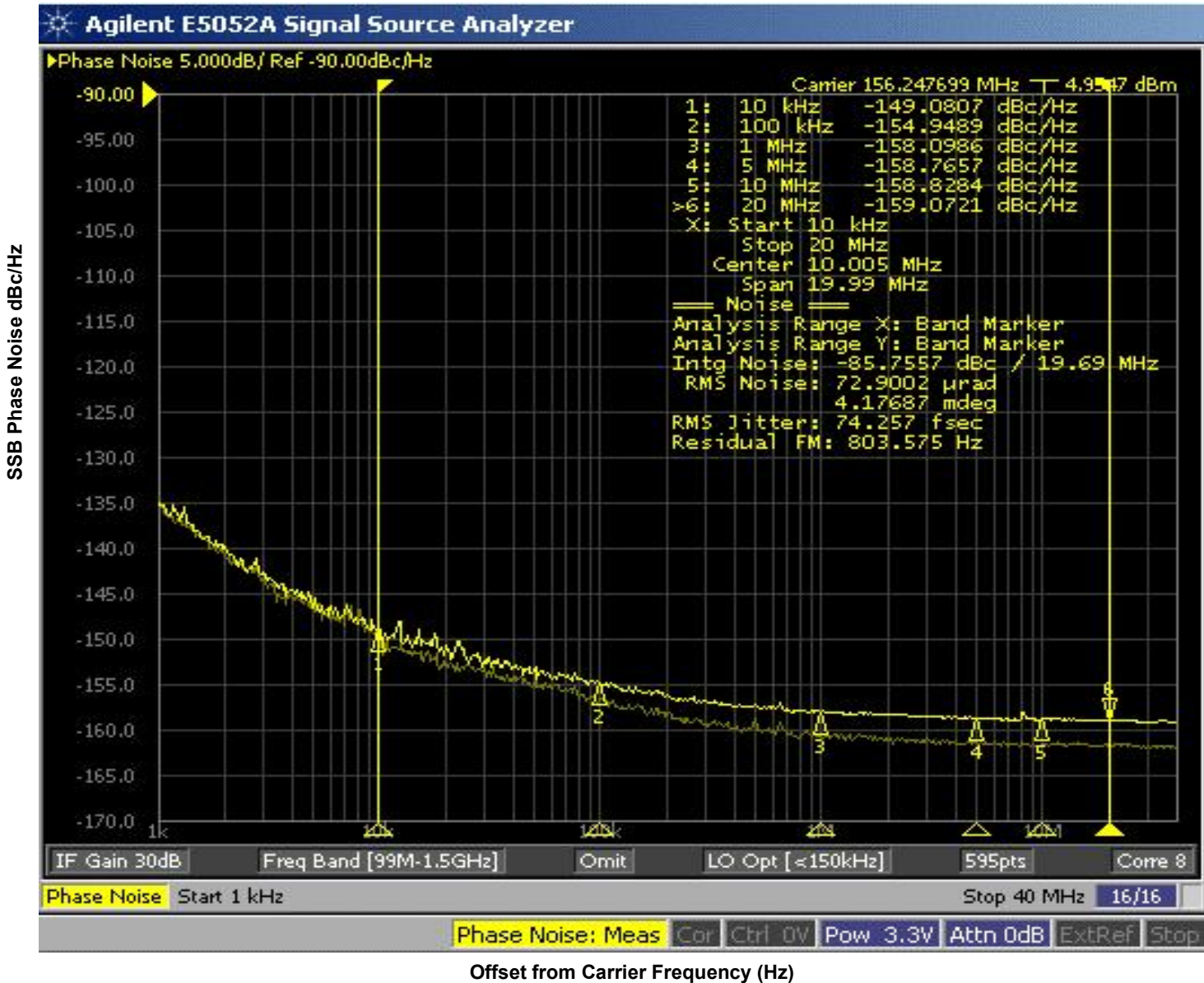
| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|-----------------------------------|---|---|--------------|------|------|---------|
| Propagation Delay and Output Skew | | | | | | |
| t _{PD_PECL} | Propagation Delay CLKin-to-LVPECL ⁽⁶⁾ | R _T = 160 Ω to GND, R _L = 100 Ω differential, C _L ≤ 5 pF | | 180 | 360 | 540 ps |
| t _{PD_LVDS} | Propagation Delay CLKin-to-LVDS ⁽⁶⁾ | R _L = 100 Ω differential, C _L ≤ 5 pF | | 200 | 400 | 600 ps |
| t _{PD_HCSL} | Propagation Delay CLKin-to-HCSL ⁽⁶⁾⁽¹⁵⁾ | R _T = 50 Ω to GND, C _L ≤ 5 pF | | 295 | 590 | 885 ps |
| t _{PD_CMOS} | Propagation Delay CLKin-to-LVCMOS ⁽⁶⁾⁽¹⁵⁾ | C _L ≤ 5 pF | VDDO = 3.3 V | 900 | 1475 | 2300 ps |
| | | | VDDO = 2.5 V | 1000 | 1550 | 2700 ps |
| t _{SK(O)} | Output Skew LVPECL/LVDS/HCSL (4) (15) (17) | Skew specified between any two CLKouts with the same buffer type. Load conditions per output type are the same as propagation delay specifications. | | | 30 | 50 ps |
| t _{SK(PP)} | Part-to-Part Output Skew LVPECL/LVDS/HCSL (6) (15) (17) | | | | 80 | 120 ps |

(17) Output skew is the propagation delay difference between any two outputs with identical output buffer type and equal loading while operating at the same supply voltage and temperature conditions.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

The additive phase jitter for this device was measured using an EPSON Clock Driver SG3225VEN as an input source and Agilent E5052A phase noise analyzer.

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, 1k Ω resistors can be tied from CLK to ground and nCLK to V_{DD}.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_I and XTAL_O can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from XTAL_I to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

Outputs:

LVCMOS Output (REFOUT)

If LVCMOS output is not used, then disable the output and it can be left floating.

LVPECL and HCSL Outputs

Any unused output pairs can be left floating. We recommend that there is no trace attached.

LVDS Outputs

Any unused LVDS output pairs can be either left floating or terminated with 100 Ω across. If they are left floating, we recommend that there is no trace attached.

Differential Outputs

If all the outputs of any bank are not used, then disable all outputs to High-Impedance.

Crystal Input Interface

The US5D306 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. In addition, the recommended 12pF parallel resonant crystal tuning is shown in *Figure 2*. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

Power Up Ramp Sequence

This device has multiple supply pins dedicated for different blocks. Output power supplies V_{DDOx} (V_{DDOA}, V_{DDOB}, V_{DDOC}) must ramp up after, or concurrently with core power supply V_{DD}. All power supplies must ramp up in a linear fashion and monotonically. Both V_{DDOA} and V_{DDOB} power supplies must be powered-up even when only one bank of outputs is in use.

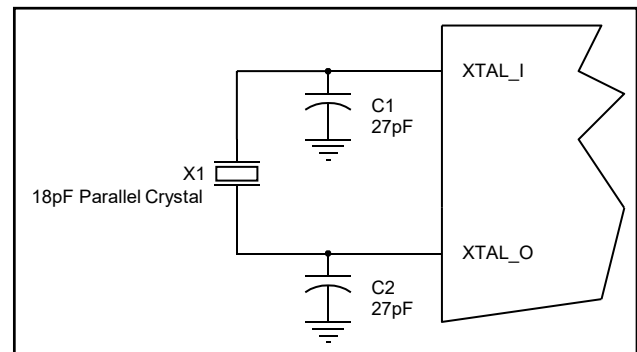


Figure 1: Crystal Input Interface

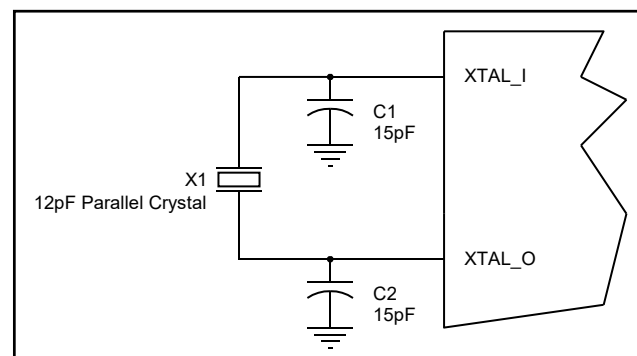


Figure 2: Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_I input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_O pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 3 shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50 Ω applications, R_1 and R_2 can be 100 Ω . This can also be accomplished by removing R_1 and changing R_2 to 50 Ω . The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Figure 4 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_I input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

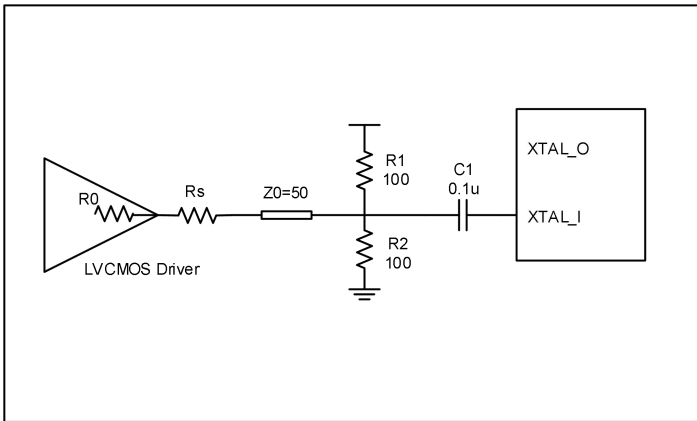


Figure 3: General Diagram for LVCMOS Driver to XTAL Input Interface

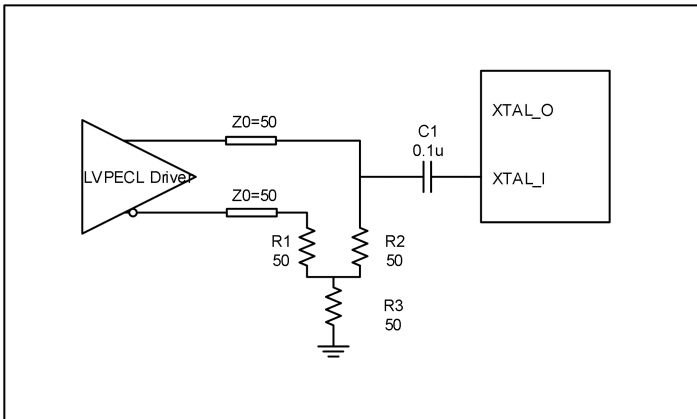


Figure 4: General Diagram for LVPECL Driver to XTAL Input Interface

Wiring the Differential Input to Accept Single-Ended Levels

Figure 5 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{DD} = 3.3V$, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω.

The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than $V_{DD} + 0.3V$. Suggest edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

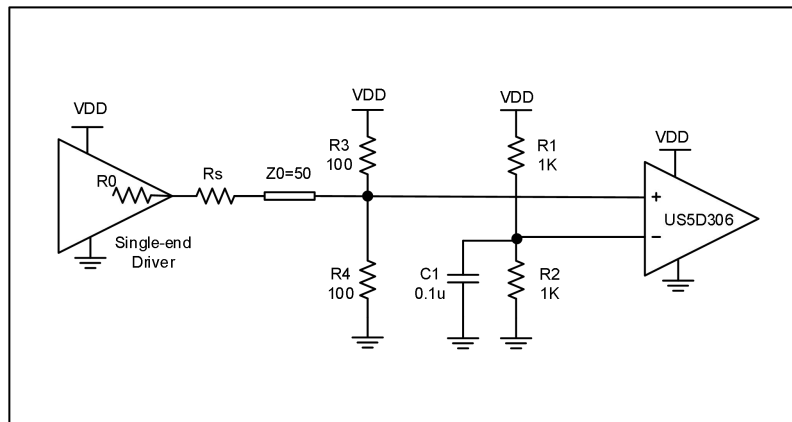


Figure 5: Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. Figure 6 to Figure 9 show interface examples for the CLK/nCLK input driven by the most common driver types. The input

interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

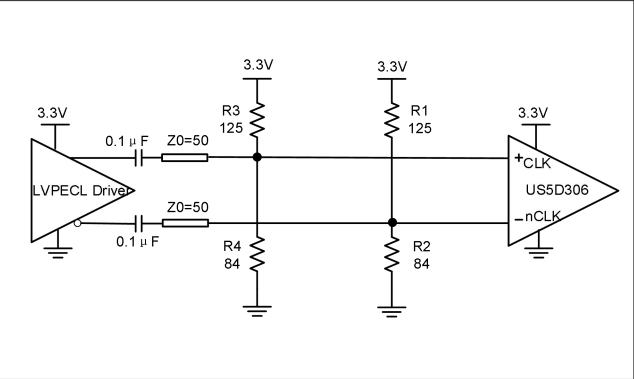


Figure 6: CLK/nCLK Input Driven by a 3.3V LVPECL Driver

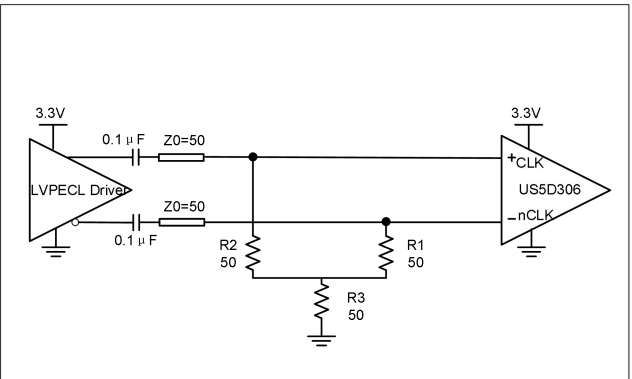


Figure 8: CLK/nCLK Input Driven by a 3.3V LVPECL Driver

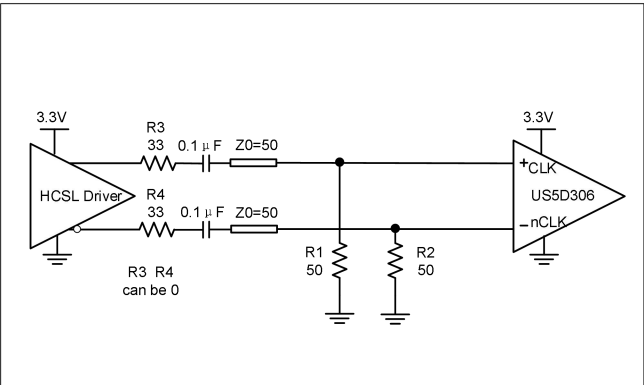


Figure 7: CLK/nCLK Input Driven by a 3.3V HCSL Driver

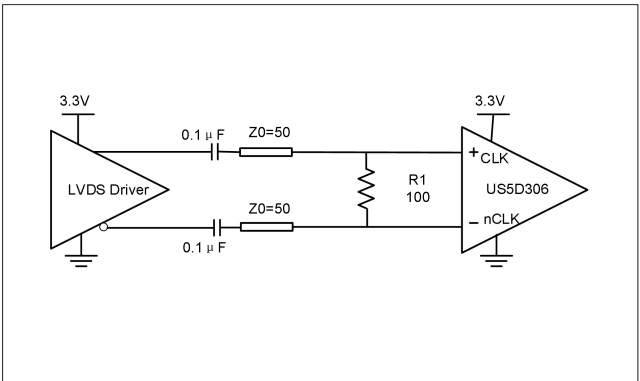


Figure 9: CLK/nCLK Input Driven by a 3.3V LVDS Driver

2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figure10 toFigure13* show interface examples for the CLK/nCLK input driven by the most common driver types. The input

interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

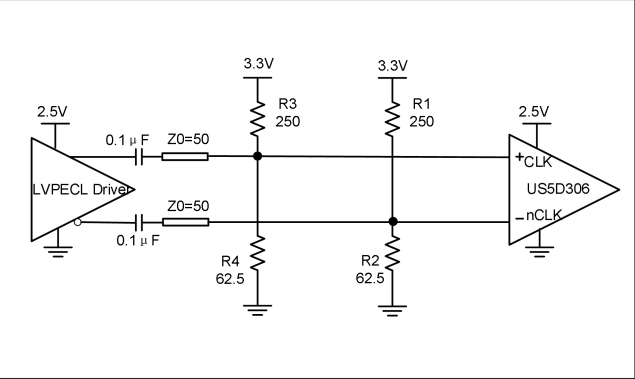


Figure 10: CLK/nCLK Input Driven by a 2.5V LVPECL Driver

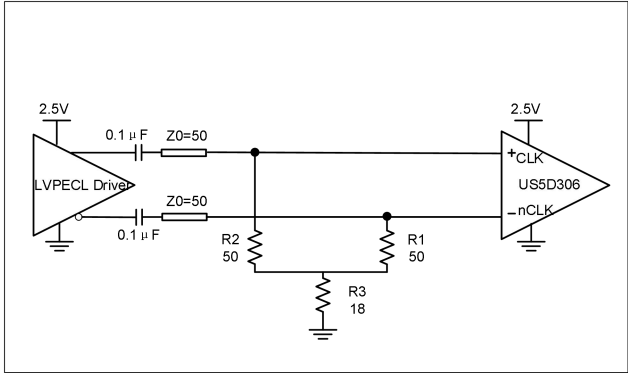


Figure 11: CLK/nCLK Input Driven by a 2.5V LVPECL Driver

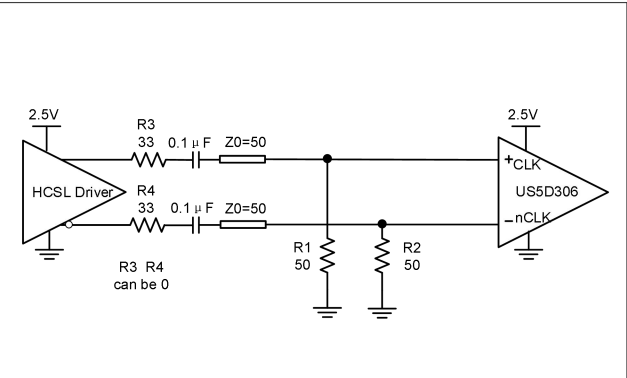


Figure 12: CLK/nCLK Input Driven by a 2.5V HCSL Driver

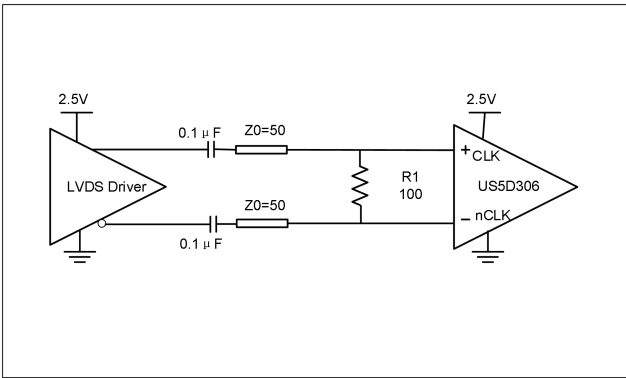


Figure 13: CLK/nCLK Input Driven by a 2.5V LVDS Driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. The standard termination schematic as shown in Figure 14 can be used.

Figure 15, which can also be used, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF .

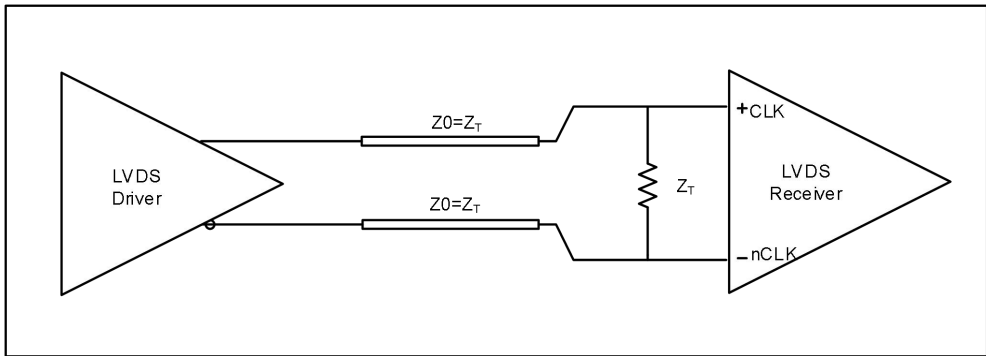


Figure 14: Standard LVDS Termination

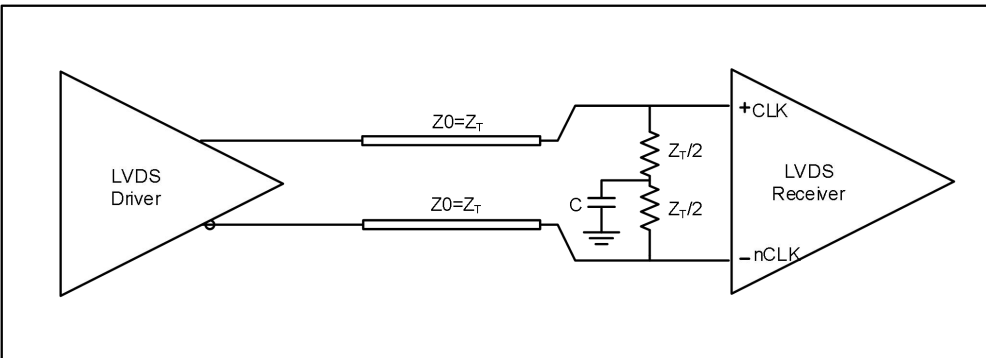


Figure 15: Optional LVDS Termination

Termination for 3.3V LVPECL Outputs

The clock topology shown below is a typical termination for LVPECL outputs. The two different terminations mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be

used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

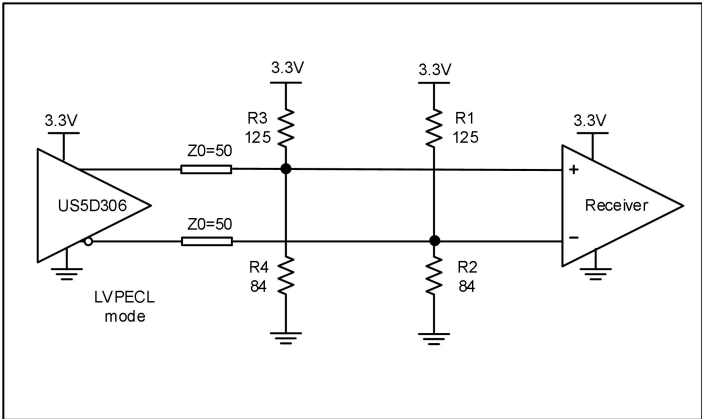


Figure 16: 3.3V LVPECL Output Termination

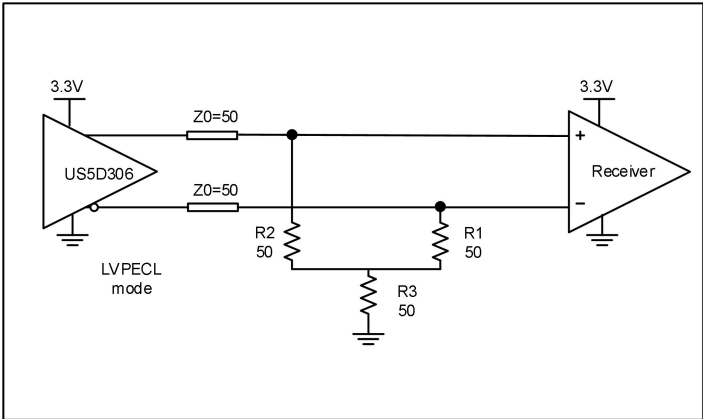


Figure 17: 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 18 and Figure 19 show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{DDO} - 2V$. For $V_{DDO} = 2.5V$, the $V_{DDO} - 2V$ is very close to ground

level. The R3 in Figure 19 can be eliminated and the termination is shown in Figure 20.

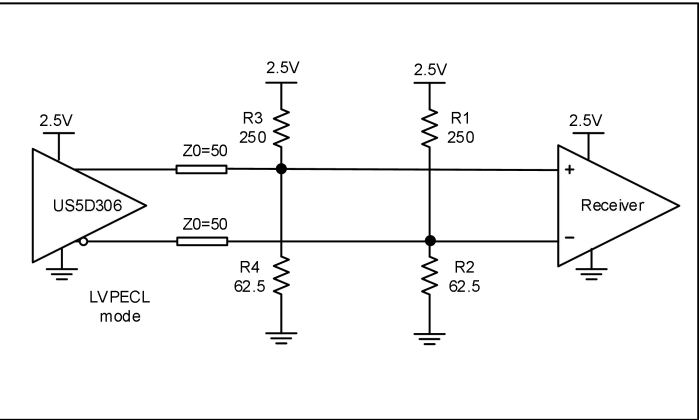


Figure 18: 2.5V LVPECL Driver Termination Example

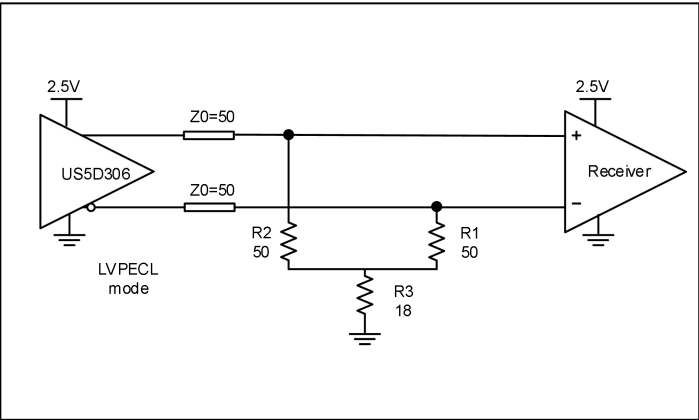


Figure 20: 2.5V LVPECL Driver Termination Example

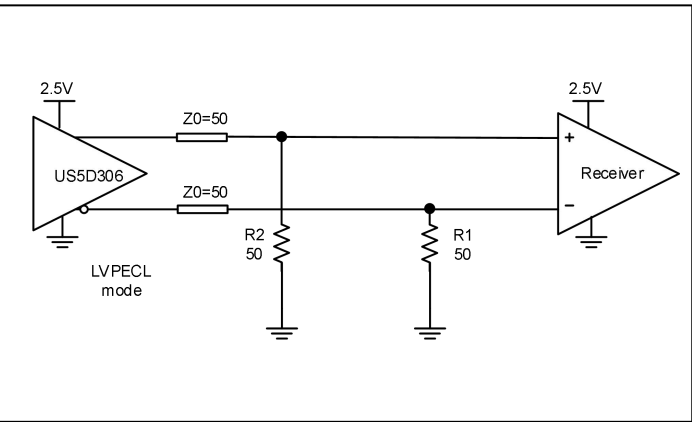


Figure 19: 2.5V LVPECL Driver Termination Example

Recommended Termination

Figure 21 is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output

types. All traces should be 50Ω impedance single-ended or 100Ω differential.

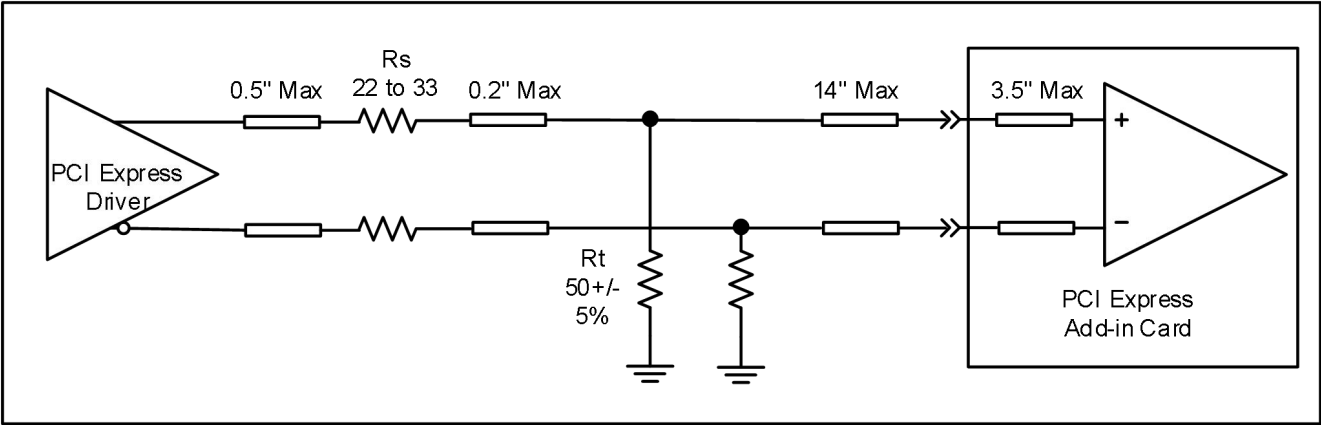


Figure 21: Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 22 is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will

be minimized. In addition, a series resistor (R_s) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

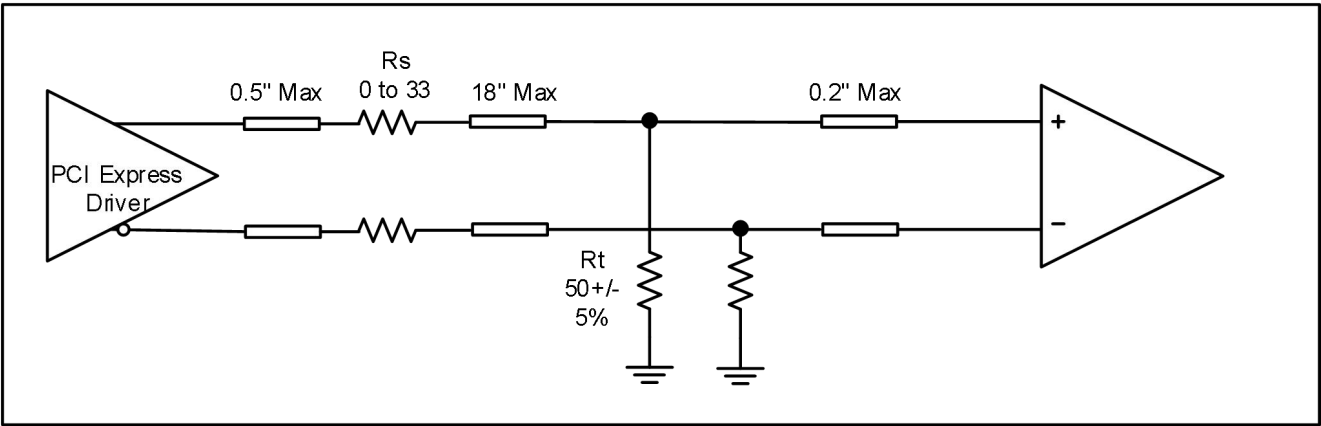


Figure 22: Recommended Termination (where a point-to-point connection can be used)

WQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 23*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only.

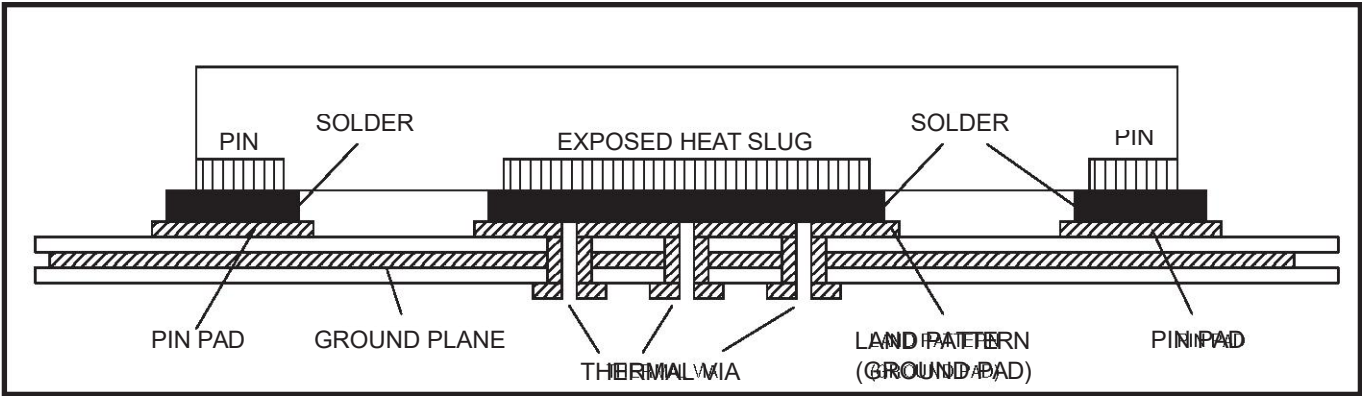
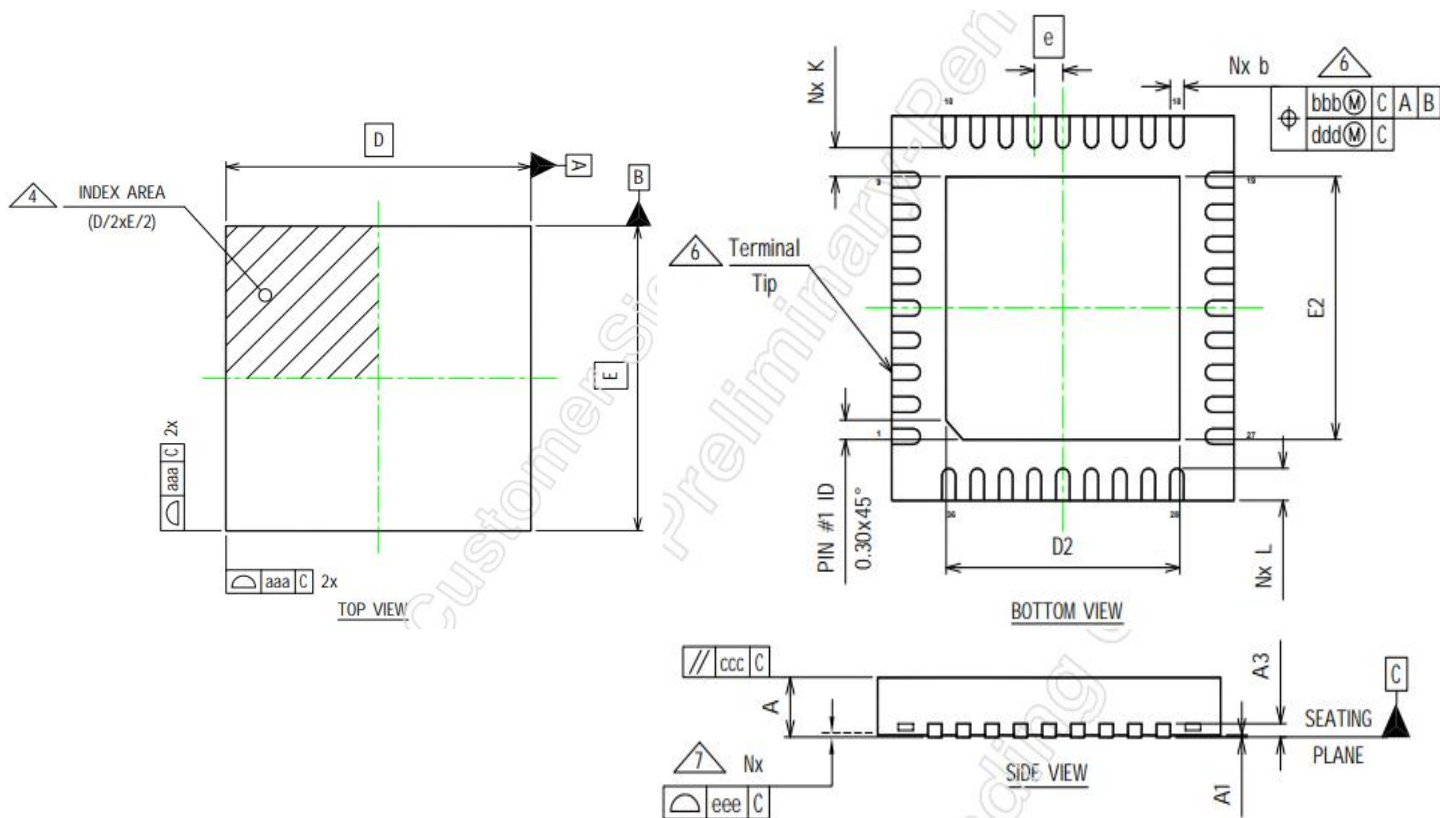


Figure 23: P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

PACKAGE DIMENSIONS



Dimension Table

| | MINIMUM | NOMINAL | MAXIMUM | NOTE |
|----|---------|----------|---------|------|
| A | 0.70 | 0.75 | 0.80 | |
| A1 | 0.00 | 0.02 | 0.05 | |
| A3 | --- | 0.203Ref | --- | |
| b | 0.19 | 0.24 | 0.29 | 6 |
| D | 6.00BSC | | | |
| E | 6.00BSC | | | |
| e | 0.50BSC | | | |
| D2 | 3.95 | 4.10 | 4.20 | |
| E2 | 3.95 | 4.10 | 4.20 | |
| K | 0.20 | --- | --- | |
| L | 0.40 | 0.50 | 0.60 | |

| | | |
|-------------|----------------|---|
| aaa | 0.05 | |
| bbb | 0.10 | |
| ccc | 0.10 | |
| ddd | 0.05 | |
| eee | 0.08 | |
| N | 36 | 3 |
| ND | 9 | 5 |
| NE | 9 | 5 |
| NOTES | 1,2 | |
| LF PART NO. | 443233 | |
| LF DWG. NO. | CARSEM-HT-107A | |

Note:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals on D and E side respectively.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Colararity applies to the terminals and all other bottom surface metallization.

Reflow profile

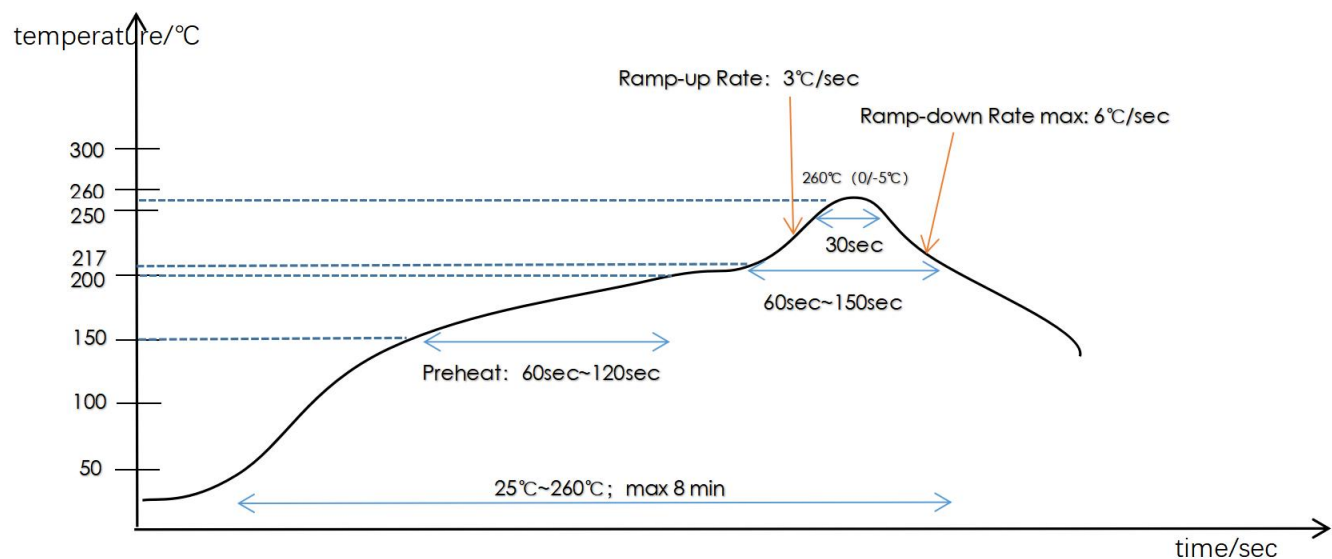


Figure: Recommended Temperature(PB-Free)

| Reflow Condition | Convection or IR/Convection |
|--|-----------------------------|
| Average ramp-up rate(217°C to Peak) | 3 °C/second max |
| Preheat temperature 175(±25)°C | 60~120 seconds |
| Temperature maintained above 217°C | 60~150 seconds |
| Time within 5°C of actual peak temperature | 30 seconds |
| Peak temperature range | 260 +0/-5 °C |
| Ramp-down rate | 6 °C/second max |
| Time 25°C to peak temperature | 8 minutes max |
| Maximum number of reflow cycles | ≤3 |

Revision History

| Date | Description of Change | Revision |
|------------|-----------------------|----------|
| 2022.05.05 | First Draft. | 1.0 |
| 2022.09.02 | Add PCI-E 5.0。 | 2.0 |