SQ76103C1

High-Efficiency 18V Input 3A Step-Down Converter Power Module with Integrated Inductor

General Description

SQ76103C1 is a high efficiency synchronous step-down DC-DC module capable of delivering 3A continuous current. It operates over an input voltage range from 4.7V to 18V and integrates the main switch, synchronous switch and inductor into a compact 2.8×3×1.5mm package.

Applications

- Server and data center
- Telecomm Boards
- General purpose POL

Features

- 4.7-18V input voltage range
- 0.8V to 5.4V adjustable output voltage
- 3A load current capability
- FCCM for small output voltage ripple
- Power Good indicator
- External programmable soft-start time to limit the inrush current
- Output over current protection with auto recovery
- Input UVLO
- Over temperature protection
- Compact Package: MQFN 2.8×3-8
- Height: 1.5mm max

Typical Application

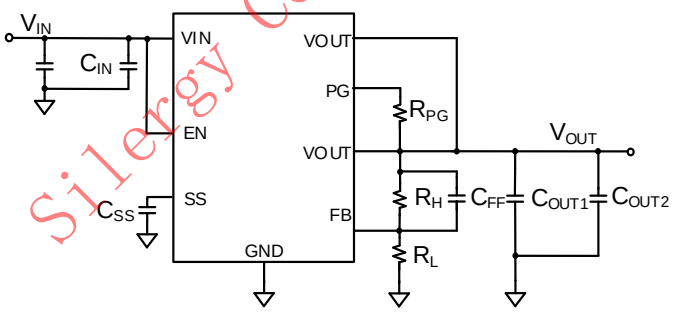


Figure 1. Application Circuit

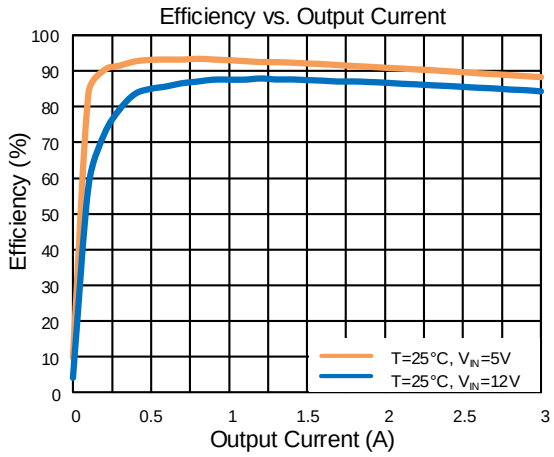
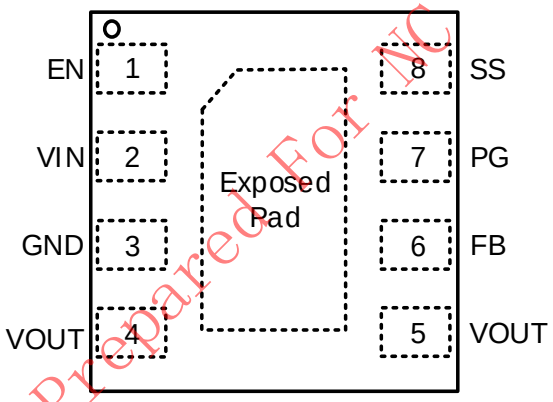


Figure 2. V_{OUT}=3.3V Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SQ76103C1ACE	QFN2.8×3-8 RoHS-Compliant and Halogen-Free	NA

Pinout (top view)



Pin No	Pin Name	Pin Description
1	EN	Enable control pin. Pull high to turn on the device. Integrated with 400kΩ pull down resistor. This resistor is only active when V_{IN} is available.
2	VIN	Input pin.
3	GND	Ground pin.
4, 5	VOUT	Output pin. Decouple this pin to GND pin with at least 22μF*2 ceramic cap.
6	FB	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.8\times(1+R_H/R_L)$.
7	PG	Power good indicator. Open drain output at PG OK status. Recommended pull-up resistor is 10kΩ-100kΩ
8	SS	Soft-start programming pin. Connect a capacitor from this pin to ground to program the soft-start time. If this pin is floating, soft-start time is about 370μs.
	Exposed Pad	This pad must be connected to GND.

Block Diagram

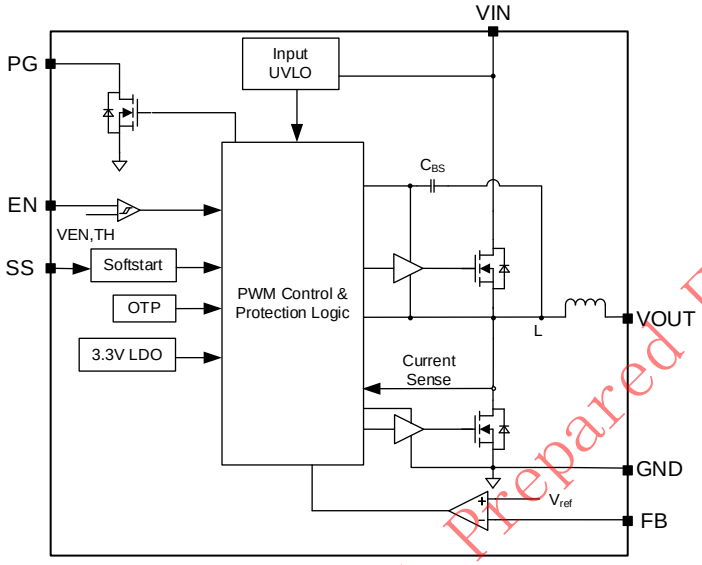


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN	-0.3	19	V
EN, PG, SS	-0.3	V_{IN} + 0.3	
FB,VOUT	-0.3	6	
Junction Temperature, Operating	-40	125	°C
Lead Temperature (Soldering,10sec.)		260	
Storage Temperature	-55	125	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	30	°C/W
Ψ_{JB} Junction-to-Board Thermal Resistance	17.1	
P_D Power Dissipation T_A = 25°C	3.33	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Input Voltage	4.7	18	V
Output Voltage	0.8	5.4	
Output Current	0	3	A

Electrical Characteristics

(V_{IN} = 12V, V_O = 3.3V, I_O = 3A, C_O = 2×22μF, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Specifications	Input Voltage Range	V_{IN}		4.7		18	V
	Input UVLO Rising Threshold			4.3	4.5	4.7	V
	Input UVLO falling Threshold			3.9	4.1	4.3	V
	Input Current with No Load		EN=high, T_A=-40°C to 85°C	18	22	27	mA
	Shutdown current		EN=low		2	5	μA
Output Specifications	Feedback reference voltage	V_{FB}		0.785	0.8	0.815	V
			T_J= 0°C to 85°C	0.788	0.8	0.812	V
	Load Regulation (Note4)		V_{IN}=12V,T_A=-40°C to 85°C, I_O=0 to 3A			±1	%
	Line Regulation (Note 4)		V_{IN}=5-18V,T_A=-40°C to 85°C, I_O=1.5A			±1	%
	Temperature Regulation (Note 4)		V_{IN}=12V,T_A=-40°C to 85°C, I_O=1.5A			±2	%
	Bottom FET Current Limit	$I_{LIM,BOT}$		3.0			A
	Rise time	T_{rise}	From 10% to 90% of Output Set-Point, C_{SS}=Open		370	500	μs
General Specifications	Switching Frequency	F_{sw}		1.7	2	2.3	MHz
	Thermal Shutdown Temperature		OTP Mode: Auto Recovery		150		°C
	Thermal Shutdown Hysteresis				15		°C
	Maximum Duty Cycle (Note 4)	D_{max}		85			%
	Min on time (Note 4)	$T_{on,min}$			50		ns
Control and Indicator Signals	EN pin logic high threshold (rising)			0.9			V
	EN pin logic low threshold (falling)					0.3	V
	EN Pull Down Resistance	R_{EN}	V_{IN}=12V, V_{EN}=0.2V.	300	420	500	kΩ
	Power Good Asserts Threshold		V_{FB} rising, PG from low to high	91	95	99	%V_{REF}
	Power Good Hysteresis				5		%V_{REF}
	PG low output voltage	$V_{PG,OL}$	I_{sink}=2mA			0.3	V
	PG Input Leakage Current	$I_{PG,LKG}$	V_{PG}=1.8V			0.4	μA

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} and Ψ_{JB} are evaluated based on a four-layer 8cm×8cm Silergy Evaluation Board under natural convection conditions at T_A = 25°C. PCB thickness: 1.6mm, copper thickness: 2oz. Junction temperature (T_J) refers to the hottest device temperature which is the inductor temperature. It is also considered equal to T_C (Case temperature) as the inductor top surface is exposed. Ambient temperature (T_A) refers to the air temperature 0.5 inch above the module. Board temperature(T_B) refers to the PCB Temperature 1mm away from the hottest module pin on the PCB top layer.

Note 3: The device is not guaranteed to function outside its operating conditions.

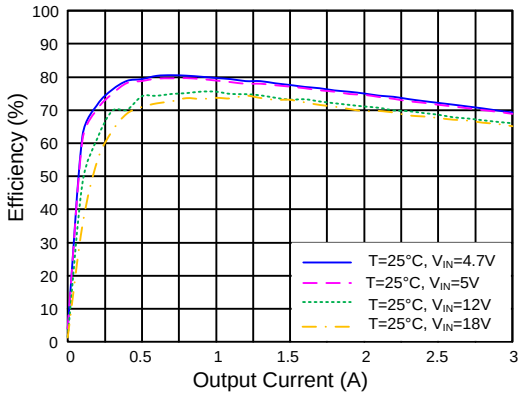
Note 4: The values are guaranteed by design, statistical correlation, not production tested.

Typical Performance Characteristics

(C_{OUT} = 2×22μF, C_{SS}=3.3nF, T_A = 25°C, resistor tolerance is ±1%, unless otherwise specified.)

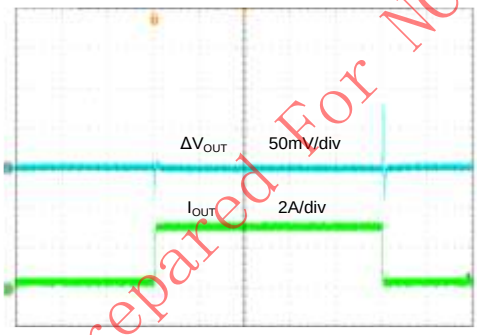
V_{OUT}=0.8V

Efficiency vs. Output Current



Load Transient

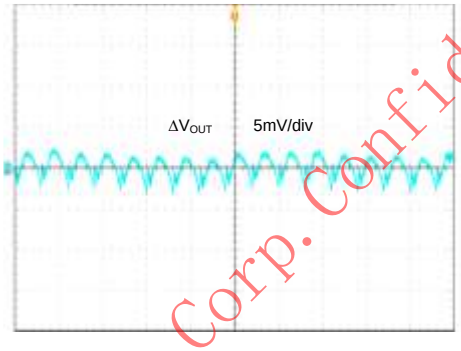
(V_{IN}=12V, V_{OUT}=0.8V, I_{LOAD}=0.3A~3A)



Time (200μs/div)

Output Ripple

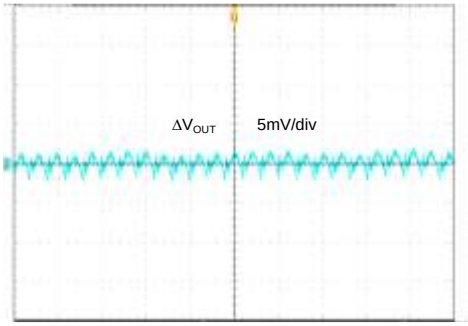
(V_{IN}=12V, V_{OUT}=0.8V, I_{OUT}=0A)



Time (2μs/div)

Output Ripple

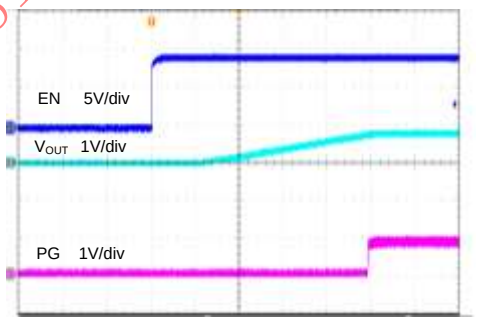
(V_{IN}=12V, V_{OUT}=0.8V, I_{OUT}=3A)



Time (2μs/div)

Startup from EN

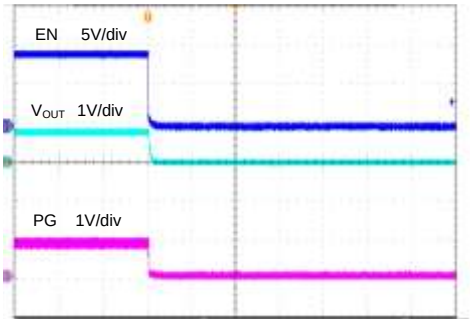
(V_{IN}=12V, V_{OUT}=0.8V, I_{OUT}=3A)



Time (400μs/div)

Shutdown from EN

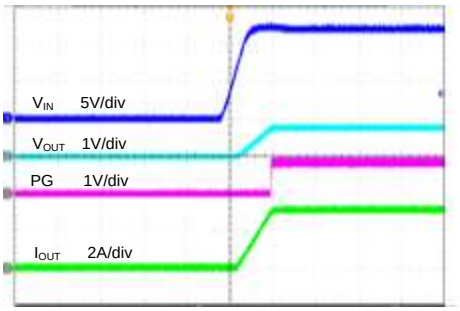
(V_{IN}=12V, V_{OUT}=0.8V, I_{OUT}=3A)



Time (400μs/div)

Startup from V_{IN}

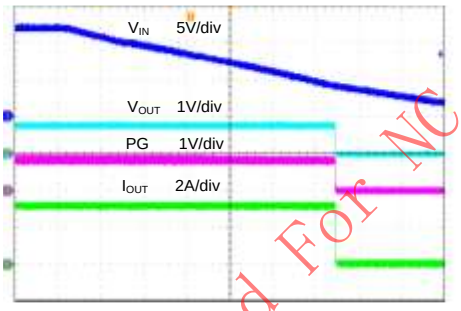
(V_{IN}=12V, V_{OUT}=0.8V, I_{OUT}=3A)



Time (2ms/div)

Shutdown from V_{IN}

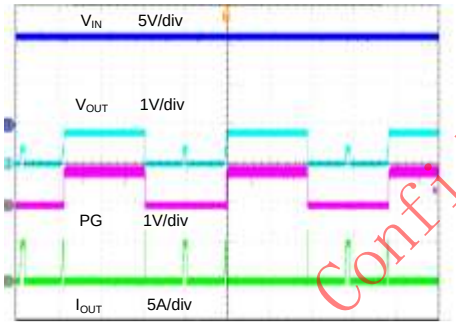
(V_{IN}=12V, V_{OUT}=0.8V, I_{OUT}=3A)



Time (2ms/div)

Short Circuit Protection

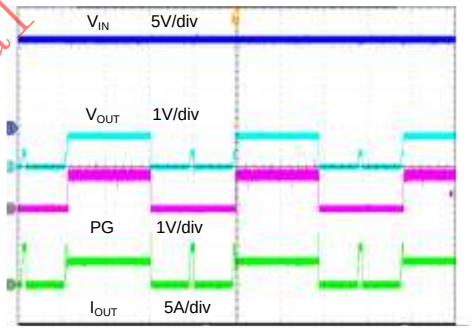
(V_{IN}=12V, V_{OUT}=0.8V, I_{OUT}=0A-Short)



Time (20ms/div)

Short Circuit Protection

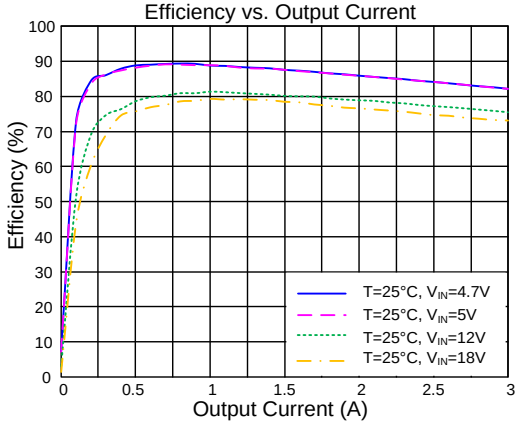
(V_{IN}=12V, V_{OUT}=0.8V, I_{OUT}=3A-Short)



Time (20ms/div)

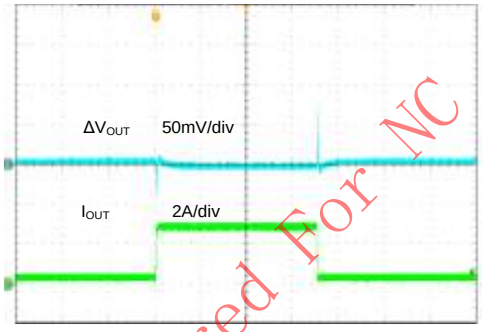
V_{OUT}=1.8V

Efficiency vs. Output Current



Load Transient

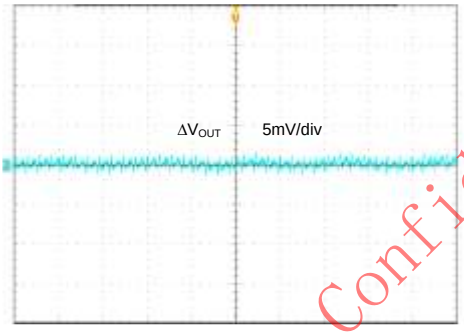
(V_{IN}=12V, V_{OUT}=1.8V, I_{LOAD}=0.3A~3A)



Time (200μs/div)

Output Ripple

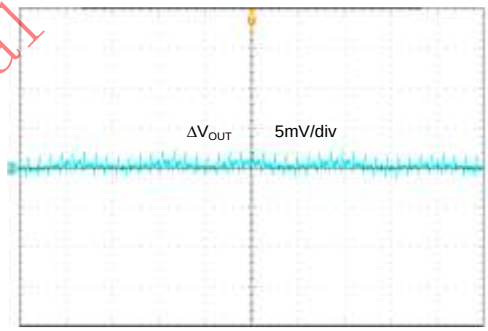
(V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=0A)



Time (2μs/div)

Output Ripple

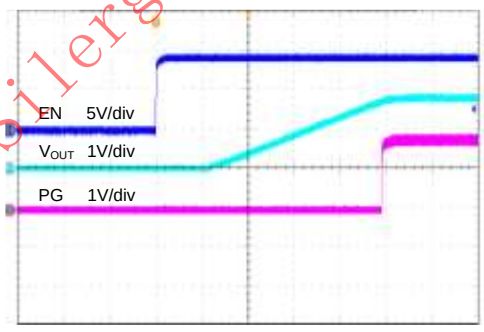
(V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=3A)



Time (2μs/div)

Startup from EN

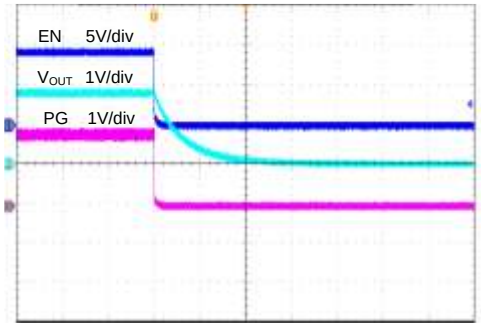
(V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=3A)



Time (400μs/div)

Shutdown from EN

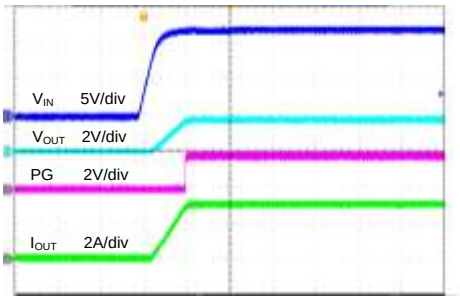
(V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=3A)



Time (400μs/div)

Startup from V_{IN}

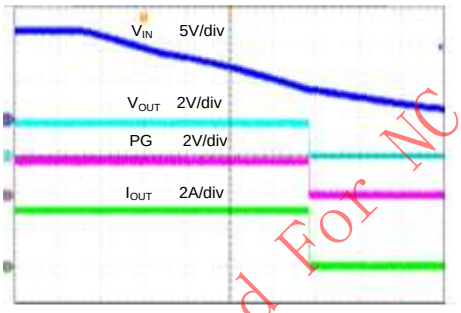
(V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=3A)



Time (2ms/div)

Shutdown from V_{IN}

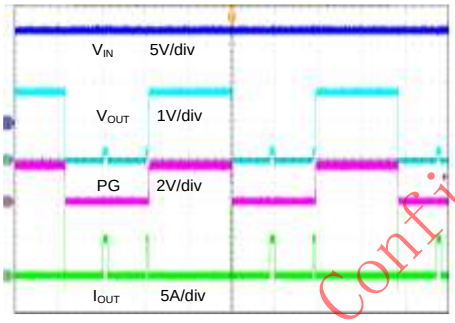
(V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=3A)



Time (2ms/div)

Short Circuit Protection

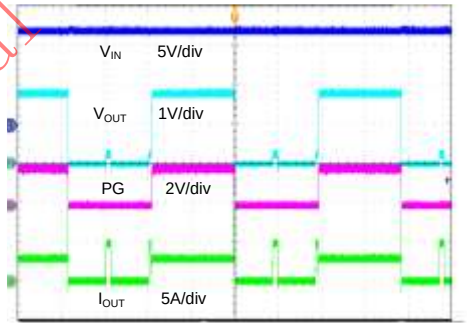
(V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=0A-Short)



Time (20ms/div)

Short Circuit Protection

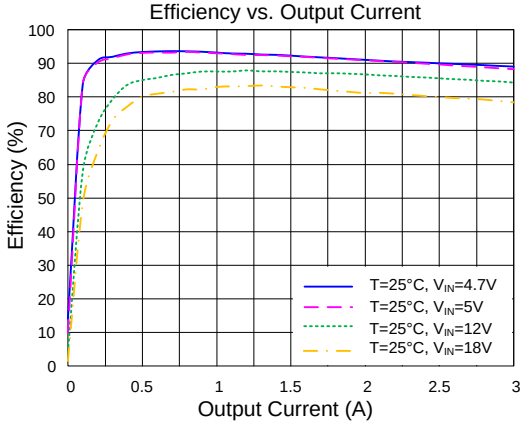
(V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=3A-Short)



Time (20ms/div)

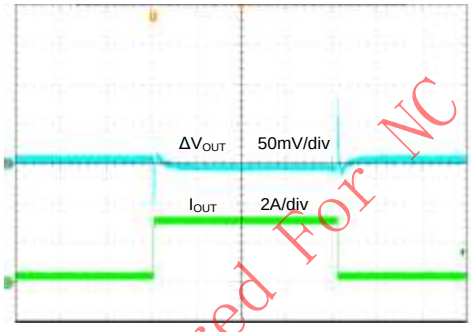
V_{OUT}=3.3V

Efficiency vs. Output Current



Load Transient

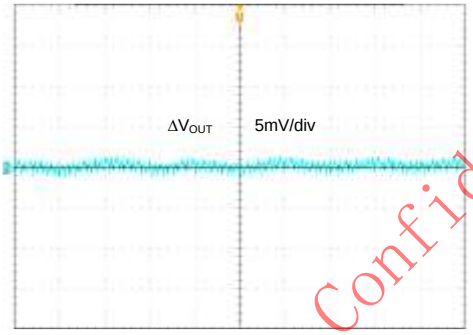
(V_{IN}=12V, V_{OUT}=3.3V, I_{LOAD}=0.3A~3A)



Time (200μs/div)

Output Ripple

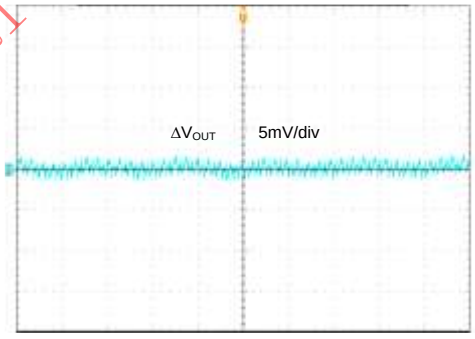
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A)



Time (2μs/div)

Output Ripple

(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A)



Time (2μs/div)

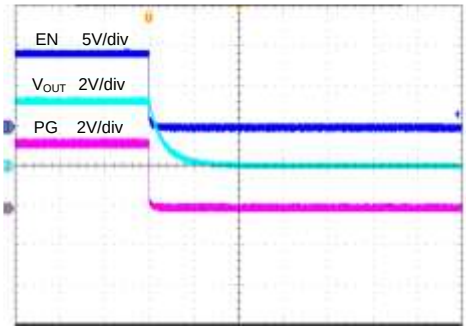
Startup from EN

(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A)

Time (400μs/div)

Shutdown from EN

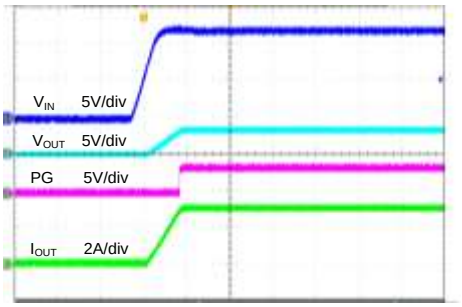
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A)



Time (400μs/div)

Startup from V_{IN}

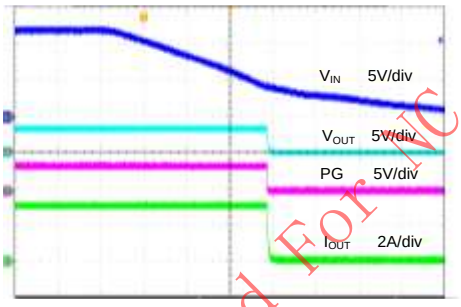
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A)



Time (2ms/div)

Shutdown from V_{IN}

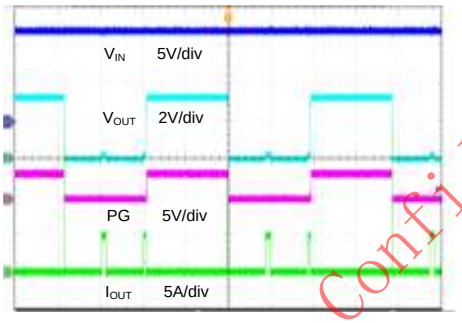
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A)



Time (2ms/div)

Short Circuit Protection

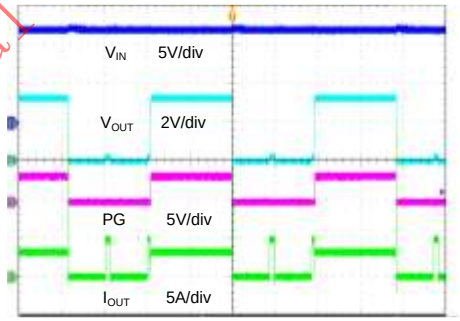
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A-Short)



Time (20ms/div)

Short Circuit Protection

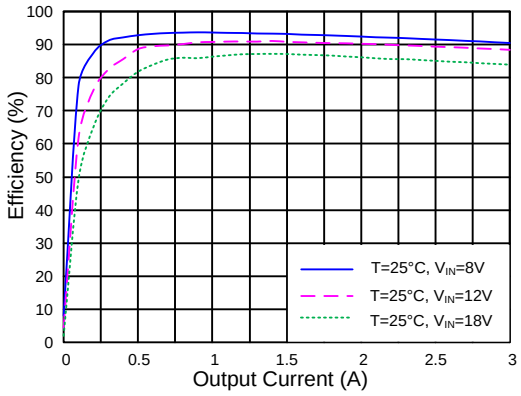
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A-Short)



Time (20ms/div)

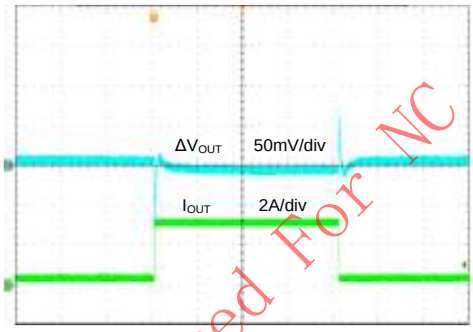
VOUT=5V

Efficiency vs. Output Current



Load Transient

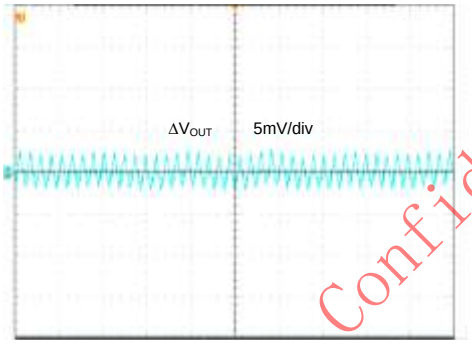
(V_{IN}=12V, V_{OUT}=5V, I_{LOAD}=0.3A~3A)



Time (200μs/div)

Output Ripple

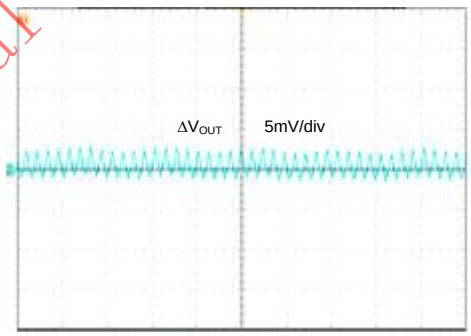
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (2μs/div)

Output Ripple

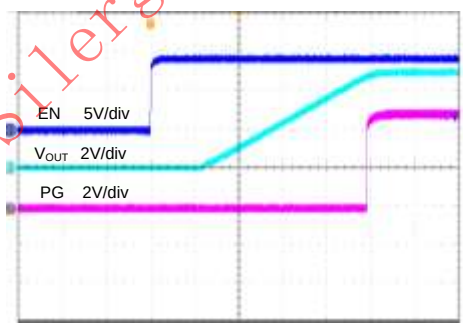
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)



Time (2μs/div)

Startup from EN

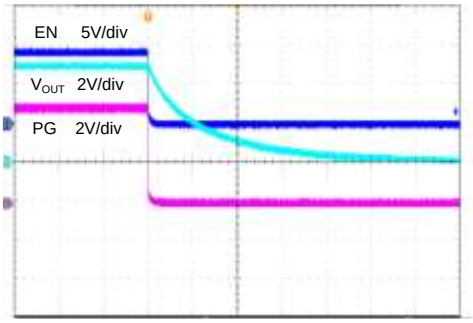
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)



Time (400μs/div)

Shutdown from EN

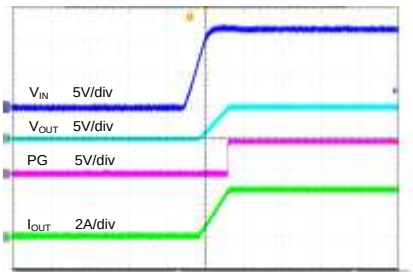
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)



Time (400μs/div)

Startup from V_{IN}

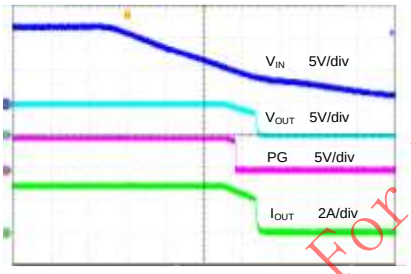
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)



Time (2ms/div)

Shutdown from V_{IN}

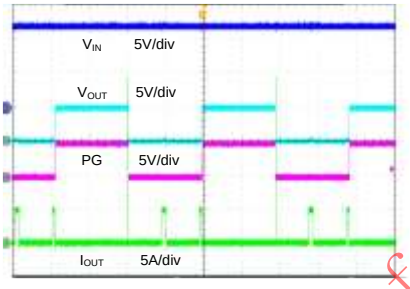
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A)



Time (2ms/div)

Short Circuit Protection

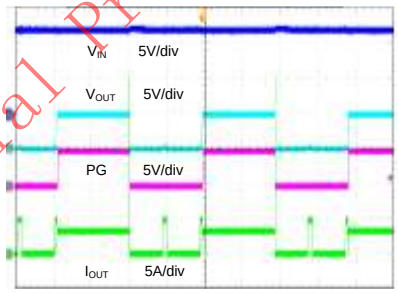
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A-Short)



Time (20ms/div)

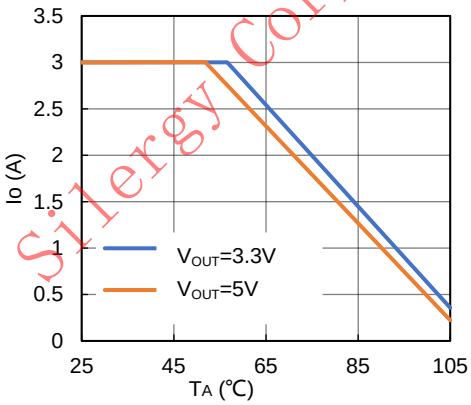
Short Circuit Protection

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A-Short)



Time (20ms/div)

Thermal Derating V_{IN}=12V



Note:

1) T_A: Air temperature, measured at 0.5 inch above IC.
2) Based on a four-layer 80mm*80mm Silergy Evaluation Board in the natural convection.
3) The inductor is exposed and the IC case is the Inductor top surface.
4) The thermal derating test limits IC case temperature under 115°C.

Applications Information

Feedback Resistor Dividers R_H and R_L

Choose R_H and R_L to program the proper output voltage. A value of between 10kΩ and 100kΩ is highly recommended for both resistors. R_L can be calculated to be:

$$R_L = \frac{0.8V \times R_H}{(V_{OUT} - 0.8V)}$$

A feed forward capacitor C_{FF} could be placed paralleling to R_H to get better transient performance. Please refer to the recommended R_H, R_L, C_{FF} value in the external BOM section of the EVB document.

Programmable Soft-start Time

The soft-start time can be programmed by the SS pin. Connect one capacitor between the SS pin and the GND pin to program the soft-start time. The typical value of the SS charging current I_{SS} is 1.7μA. The rise time can be calculated by equation below:

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}}{I_{SS}(\mu A)}$$

To guarantee the programmable soft-start time is not too short when using smaller SS capacitor, there is one minimum soft-start time limitation, the minimum soft-start time is 0.37ms.

Table 1. C_{SS} capacitance VS. measured rise time

Capacitor from SS pin to GND (nF)	Soft start time form 10% to 90% V_{OUT} setpoint(ms)
Open	0.37
3.3	1.36
22	9.64
47	19.5
100	43.1
470	196
1000	482

Input Capacitor C_{IN}

To minimize the potential noise problem, place a typical X7R or better grade ceramic capacitor and greater than 10μF capacitance. Place this ceramic capacitor really close to the VIN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and VIN/GND pins.

To reduce input voltage overshot and ringing in case where the input source is far away from module VIN pin, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}}$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications, one 10uF X7R capacitor is sufficient.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor.

For the best performance, it is recommended to use X7R or better grade ceramic capacitor and greater than 22μF*2 capacitance. Place this ceramic capacitor really

close to the VOUT and GND pins to minimize the loop area formed by C_{OUT}, and the VOUT/GND pins.

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 1.2A using two 22μF ceramic capacitors, each with an ESR of approximately 3mΩ for a parallel total of 44μF and 1.5mΩ ESR.

$$V_{RIPPLE,ESR} = 1.2A \times 1.5m\Omega = 1.8mV$$

$$V_{RIPPLE,CAP} = \frac{1.2A}{8 \times 44\mu F \times 2MHz} = 1.7mV$$

Total ripple = 3.5mV. The actual capacitive ripple may be higher than the calculated value because the capacitance decreases with the voltage on the capacitor.

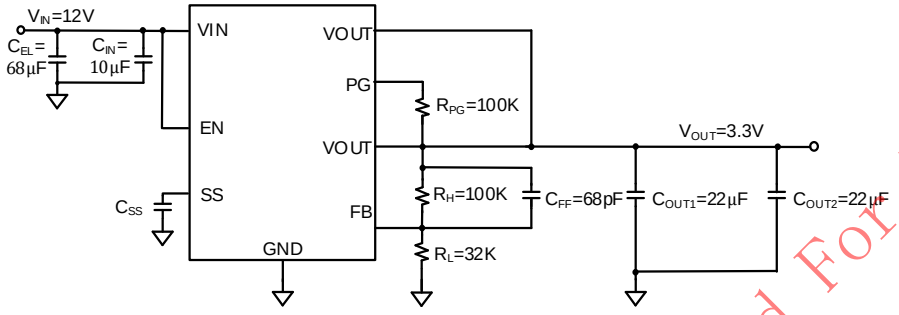
Table 2. External Capacitor Recommendation

	Description	Vendor	PN
C_{IN}	10μF/25V X7R/1206	Murata	GRM31CR71E106MA12#
C_{OUT}	22μF/10V X7R/0805	Murata	GRM21BZ71A226ME15#
C_{OUT}	47μF/6.3V X7U/1206	Murata	GXM31CE70J476ME10#
C_{OUT}	100μF/6.3V X7S/1210	Murata	GRM32EC70J107ME15#

Table 3. Output Capacitor Recommendation

V_{OUT}	C_{OUT_MIN}	C_{OUT_MAX}
0.8V ≤ V_{OUT} ≤ 0.9V	22μF×2	300μF
0.9V < V_{OUT} ≤ 1.8V	22μF×2	400μF
1.8V < V_{OUT} ≤ 3.3V	22μF×2	600μF
3.3V < V_{OUT} ≤ 5.4V	22μF×2	1100μF

Application Schematic (V_{OUT} = 3.3V)



BOM List

Designator	Description	Part Number	Manufacturer
C_{EL}	68uF/25V Electrolytic Cap		
C_{IN}	10µF/25V/X7R, 1206	GRM31CR71E106MA12D	murata
C_{OUT1}	22uF/10V/X7R,0805	GRM21BZ71A226ME15#	murata
C_{OUT2}	22uF/10V/X7R,0805	GRM21BZ71A226ME15#	murata
C_{ff}	68pF/100V,C0G,0603	GCM1885C2A680JA16D	murata
C_{ss}	3.3n/50V,C0G, 0603	GRM1885C1H332JA01#	murata
R_H	100kΩ, 1%, 0603		
R_L	32kΩ, 1%, 0603		
R_{PG}	100kΩ, 1%, 0603		

Layout Design

To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN} and C_{OUT}.

1) C_{IN} must be close to the pins VIN and GND. The loop area formed by C_{IN} and GND must be minimized.
2) C_{OUT} must be close to the pins VOUT and GND. The loop area formed by C_{OUT} and GND must be minimized.
3) Place the FB components (R_H, R_L, C_{FF}) as close to the FB pin as possible.
4) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

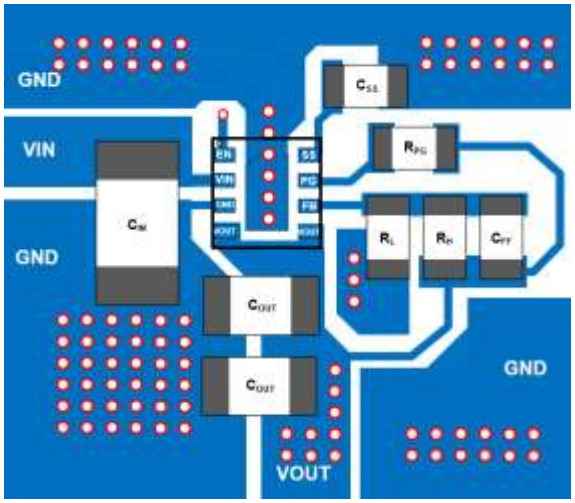
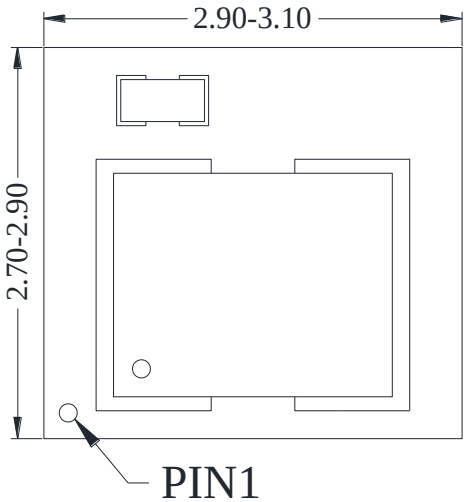
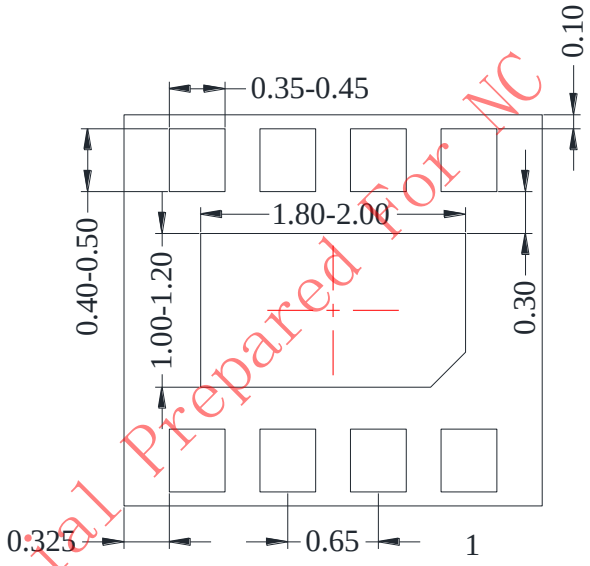


Figure 2. PCB Layout Suggestion

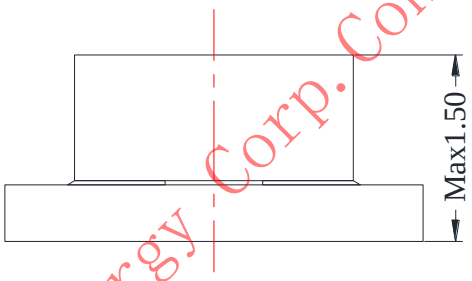
MQFN3×2.8-8 Package Outline Drawing



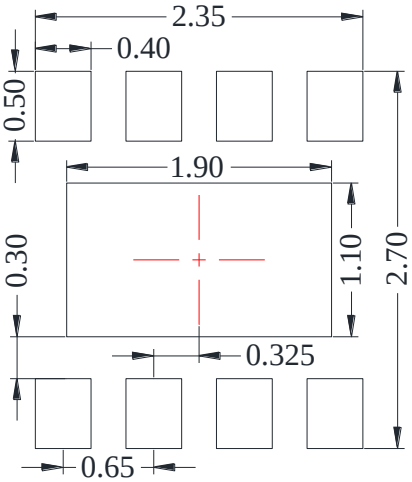
Top View



Bottom View



Front View



Recommended PCB layout
(Reference only)

Notes:

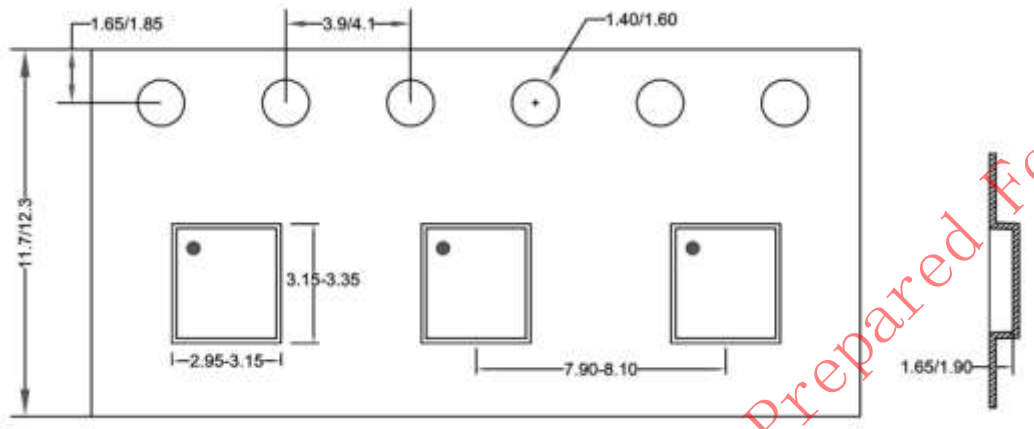
1. All dimension in millimeter and exclude mold flash & metal burr.

2. Center line on drawing refers to the chip body center.

Taping & Reel Specification

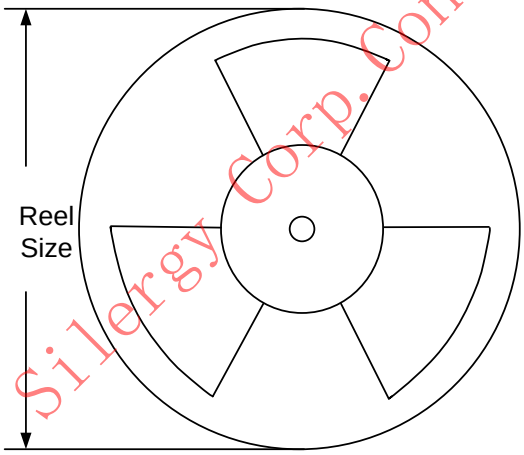
1. Taping Orientation

MQFN2.8x3



Feeding Direction →

2. Carrier Tape & Reel specification for packages



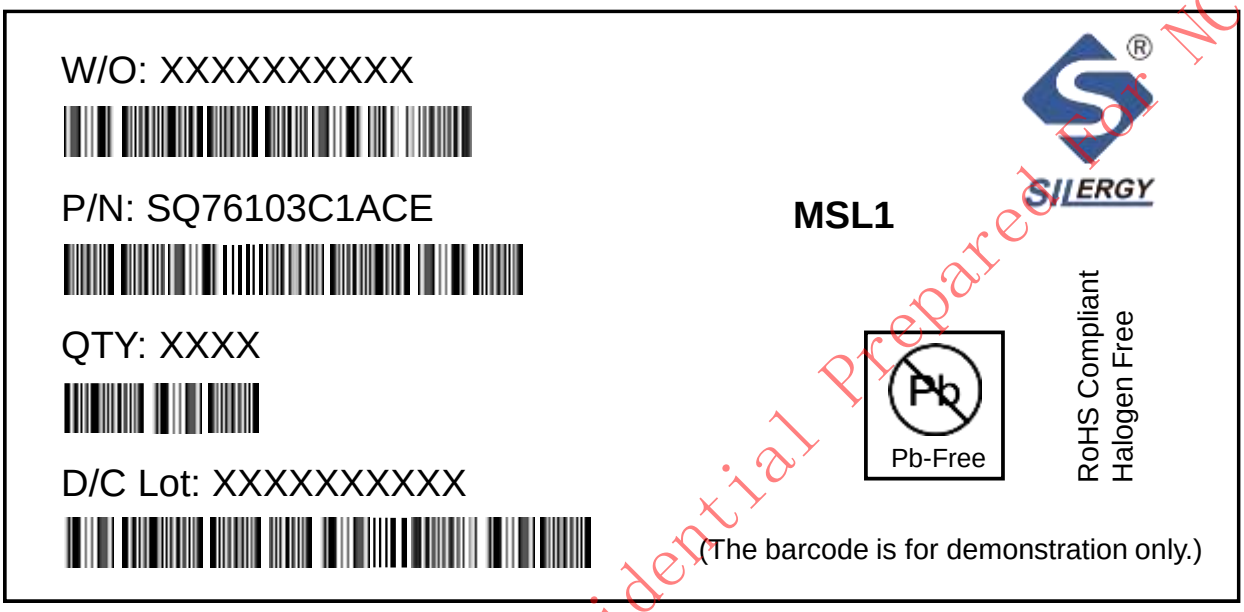
Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
MQFN2.8x3	12	8	13"	400	400	3000

Others: NA

Packaging Information

Device Code: **HAW**

Label Information



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
2023/12/06	1.0	Production Release

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