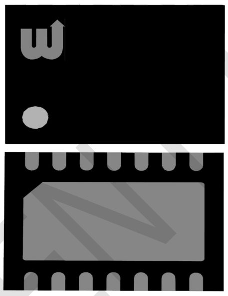
WSTQ6160AN
Smart High-Side Power Switch Quad Channel，140mΩ，DFN9×6-14L ，*AEC-Q100 qualified*

Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for loads with high inrush current, such as lamps
- Suitable for 12 V and 24 V trucks + trailer and transportation systems

Package	DFN9×6-14L
Marking	WSTQ6160AN



Basic Features

- Quad channel device
- Very low stand-by current
- 3.3 V and 5 V compatible logic inputs
- Optimized electromagnetic compatibility
- Very low electromagnetic susceptibility

Product Summary

Parameter	Symbol	Value
Max. transient supply voltage	V_S	60V
Operating voltage range	V_{NOM}	8-36V
On-state resistance (per channel，T_j = 25℃)	R_{ON}	140mΩ
Nominal load current (one channel active，T_j = 25℃)	$I_{L(NOM)1}$	2.5A
Nominal load current (All channels active，T_j = 25℃)	$I_{L(NOM)2}$	1.8A
Typical current sense ratio (I_{OUT}=1A)	K	460
Current limitation	I_{LIMH}	5A
Supply current in sleep	I_{SLEEP}	3uA

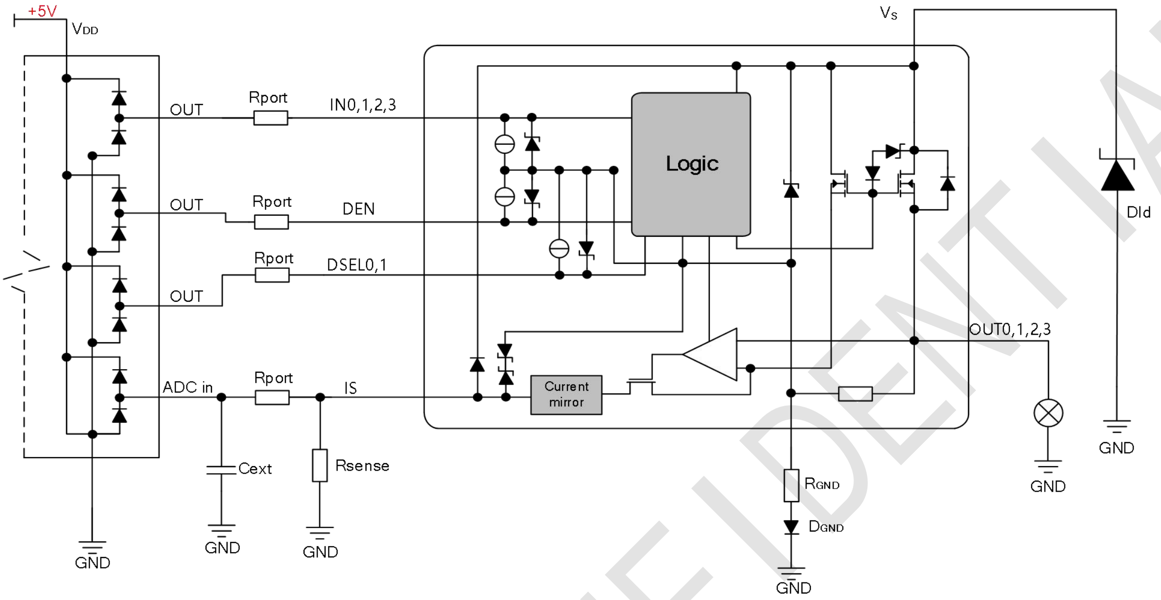
Diagnostic Functions

- Proportional load current sense
- High current sense precision for wide range currents
- Off-state open load detection
- OUT short to VS detection
- Overload and short to ground latch-off
- Thermal shutdown latch-off
- Very low current sense leakage

Protection Functions

- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of VS
- Thermal shutdown
- Electrostatic discharge protection

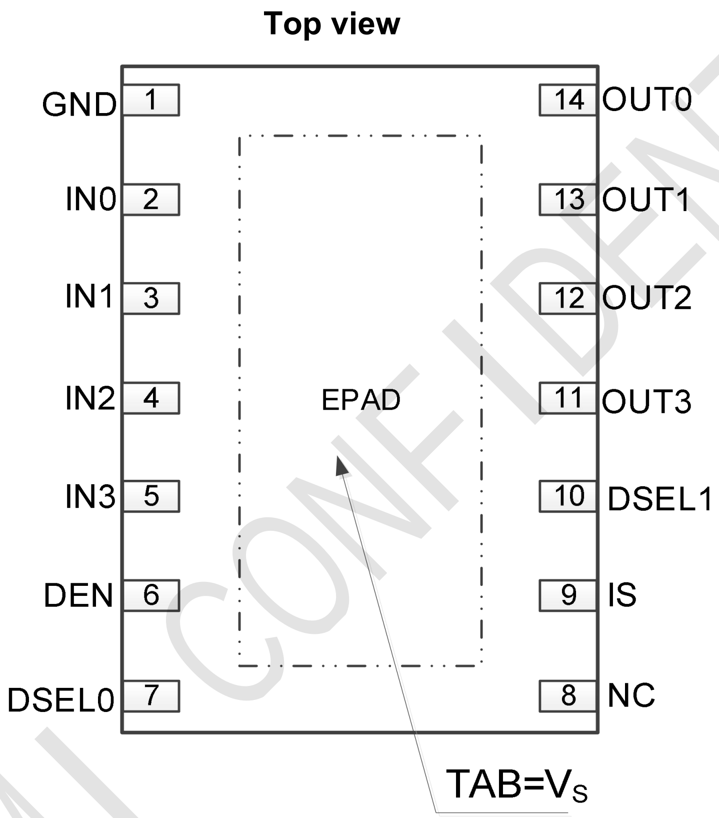
Typical Application Circuit



Ordering Information

Package	Top Mark	Part No.
DFN9×6-14L, Pb-free	WSTQ6160AN XXYMXX	WSTQ6160AN

Pin Configuration



Pin Description

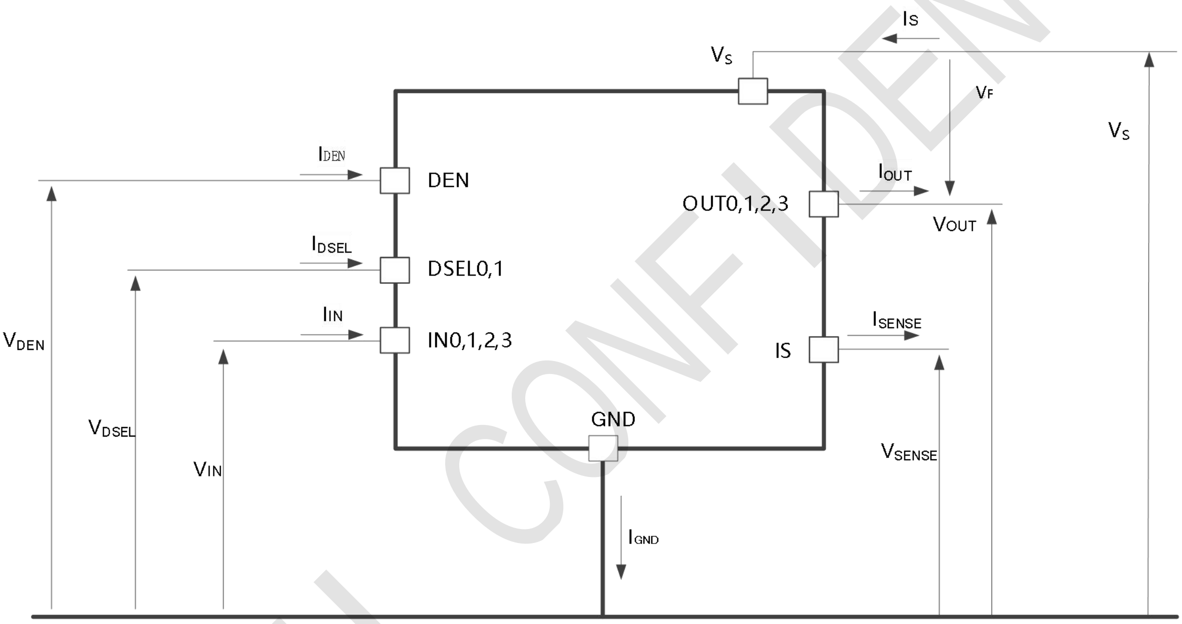
Pin Name	Pin NO.	Pin Description
GND	1	Ground connection. Must be reverse battery protected by an external diode / resistor network.
IN0/1/2/3	2/3/4/5	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
DEN	6	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the IS diagnostic pin.
DSEL0/1	7/10	Active high compatible with 3 V and 5 V CMOS outputs pin; they address the IS multiplexer.
NC	8	Not Connected
IS	9	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load
OUT0/1/2/3	11/12/13/14	Power outputs.
V_S	EPAD	Battery connection.

Table 1. Suggested connections for unused and not connected pins

Connection / pin	IS	OUT	IN0,1,2,3	DEN, DSEL0,1
Floating	Not allowed	X(1)	X	X
To ground	Through 1.0K resistor	Not allowed	Through 15K resistor	Through 15K resistor

Note1：X do not care.

Current and Voltage Conventions



Note2: $V_F = V_{OUT} - V_S$ during reverse battery condition.

Absolute Maximum Ratings (Note3)

Symbol	Parameter	Value	Unit
V_s	DC supply voltage	60	V
$-V_s$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUT0,1 DC output current	Internally limited	A
V_{IN}, V_{DEN}, V_{DSEL}	IN0,1,2,3, DEN, DSEL0,1 DC input voltage	-0.3 to 6.0	V
I_{IS}	IS pin DC output current	20	mA
	IS pin DC output current in reverse	-20	
T_j	Junction operating temperature	-40 to 150	℃
T_{stg}	Storage temperature	-55 to 150	

Note3：Stressing the device above the rating listed in Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Thermal Resistance (Note4)

Symbol	Parameter	Value	Unit
T_{JC}	Thermal Resistance Junction-to-Case	1.3	℃/W
T_{JA}	Junction-to-Ambient Thermal Resistance	30	℃/W

Note4：According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

ESD Susceptibility (Note5)

Symbol	Parameter	Values	Unit
$V_{ESD(HBM)}$3)	ESD Susceptibility all Pins (HBM)	±2	kV
$V_{ESD(HBM)\_OUT}$	ESD Susceptibility OUT vs GND and V_S connected (HBM)	±4	kV
$V_{ESD(CDM)}$4)	ESD Susceptibility all Pins (CDM)	±500	V
$V_{ESD(CDM)\_CRN}$	ESD Susceptibility Corner Pins (CDM) (pins 1, 7, 8, 14)	±750	V

Note5：

1) Not subject to production test - specified by design.

2) Maximum digital input voltage to be considered for Latch-Up tests: 5.5 V.

3) ESD susceptibility, Human Body Model “HBM”, according to AEC Q100-002.

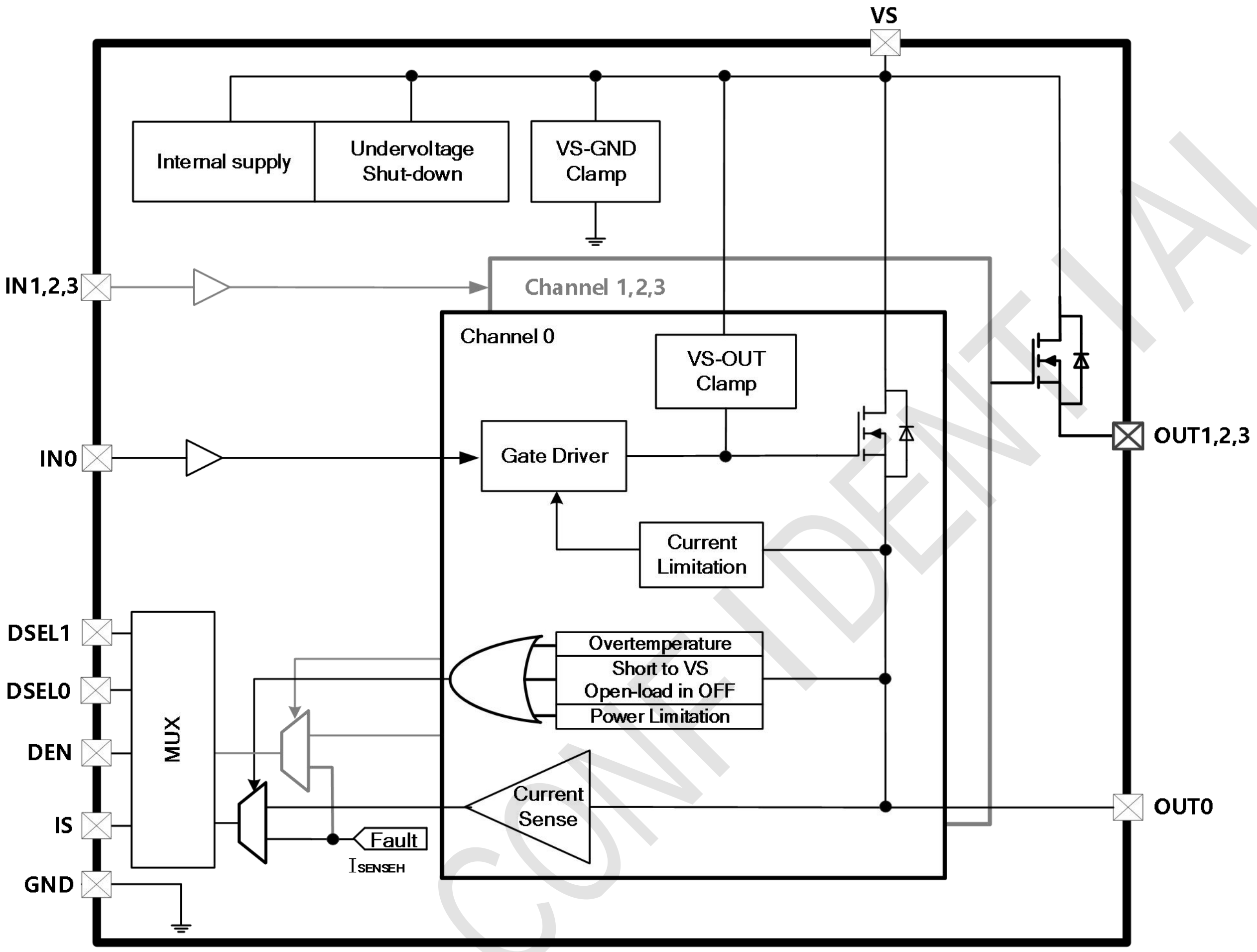
4) ESD susceptibility, Charged Device Model “CDM”, according to AEC Q100-011.

EAS Susceptibility (Note6)

Symbol	Parameter	Values			Unit	Note or Test Conditon
		Min.	Typ.	Max.		
E_{AS}	Maximum Energy Dissipation Single Pulse (one channel)			70	mJ	I_{OUT} =2.5A $T_{J(0)}$ = 150 °C V_S = 28 V

Note6:：Not subject to production test - specified by design.

Functional Block



Electrical Characteristics (Note7), 8V<V_S < 36 V; -40°C < Tj < 150°C, unless otherwise specified

Power section

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Nominal operating voltage	V_{NOM}		8	24	36	V
Extended operating voltage	V_{OP}		5		58	V
Under voltage shutdown	V_{USD}			3.5	5.0	V
Under voltage shutdown hysteresis	$V_{USDhyst}$			0.3		V
On-state resistance	R_{ON}	I_{OUT}=1A, T_j = 25℃		140		mΩ
		I_{OUT}=1A,T_j =150℃			280	
		I_{OUT}=1A,V_S =5V, T_j = 25℃			210	
Nominal load current (One Channel Active)	$I_{L(NOM)1}$	T_A=25℃		2.5		A
Nominal load current at T_A=85℃ (One Channel Active)	$I_{L(NOM)1\_85}$	T_A=85℃, T_j < 150℃		2.0		A
Nominal load current (All Channels Active)	$I_{L(NOM)2}$	T_A=25℃		1.8		A
Nominal load current at T_A=85℃ (All Channels Active)	$I_{L(NOM)2\_85}$	T_A=85℃, T_j < 150℃		1.5		A
Inverse Current Capability	$I_{L(INV)}$	V_S<V_{OUT}, V_{IN}=5V, T_A=25℃		2.5		A
V_S clamp voltage	V_{CLAMP}	I_S=20 mA	60	64	71	V
Supply current in sleep	I_{SLEEP}	V_S=36V, V_{IN}=V_{OUT}=V_{DEN}=0V V_{DSEL}=0V, T_j =25℃		3.0	6.0	µA
		V_S =36V, V_{IN}=V_{OUT}=V_{DEN} =0V, V_{DSEL}=0V, T_j= 125℃			20	µA
Sleepy mode blanking time	t_{D_SLEEP}	V_S=36V, V_{IN}=V_{OUT}=V_{DSEL}=0V V_{DEN}=5V to 0V	150	400	800	us
Supply current in active	$I_{S(ACTIVE)}$	V_S=36V, V_{DEN}=5V, $V_{IN0,1,2,3}$=0V,		1.2	2.5	mA
Control stage current consumption in ON state	$I_{GND(ON)}$	V_S=36V, V_{DEN}=5V, V_{DSEL}=0V $V_{IN0,1,2,3}$=5V		8.0	16	mA
Off-state output current	$I_{L(off)}$	V_{IN} =V_{OUT}=0V, V_S=36V, T_j =25℃	0	0.1	3	µA
		V_{IN} =V_{OUT}=0V, V_S=36V, T_j =125℃	0		6	µA
OUT - V_S diode voltage	V_F	I_{OUT} =-2A, T_j =150℃			0.9	V

Switching

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Turn-on delay time at T_j = 25℃	$T_{d\ (on)}$	V_S=28V,V_{DEN}=5V,R_L=28Ω	-	25	90	us
Turn-off delay time at T_j = 25℃	$T_{d\ (off)}$		-	35	100	us
Turn-on voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{on}$	V_S=28V,V_{DEN}=5V,R_L=28Ω	0.2	0.6	1.2	V/us
Turn-off voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{off}$		1.3	2.3	3.3	
Differential pulse skew(t_{PHL} - t_{PLH})	t_{SKEW}	V_S=28V,V_{DEN}=5V,R_L=28Ω	-50	-	50	us

Logic input (IN0,1,2,3, DSEL0,1, DEN)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic input low level voltage	V_{LOW}				0.9	V
Low level logic input current	I_{LOW}	V_{LOW}=0.9V	2	11	35	uA
Logic input high level voltage	V_{HIGH}		2.1		6.0	V
High level logic input current	I_{HIGH}	V_{HIGH}=2.0V	1	10	30	uA
Logic input hysteresis voltage	$V_{(hyst)}$		-	0.2	-	V

Protections

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
DC short circuit current	I_{LIMH}	5V < V_{CC}< 36V ,V_{DS}=6V	4	5	6.5	A
		V_{DS}=32V		3		
Short circuit current during thermal cycling	I_{LIML}	V_S=24V, V_{DEN}=5V, T_R<T_j<$T_{TSD,}$		2		
Maximum number of Short mode latch				5		cycles
Shutdown temperature	T_{TSD}		150	175	200	℃
Thermal hysteresis	T_{HYST}			20		℃
Dynamic temperature	ΔT_{J_SD}	T_j = -40℃		60		℃
Current limit thermal hysteresis	T_R			40		℃
Turn-off output voltage clamp	V_{DEMAG}	I_{OUT}=2A, V_{DEN}=5V, L= 6mH, T_j =-40℃ to 150℃	V_S-60	V_S-64	V_S-71	V

Current sense characteristics

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
I_{OUT}/I_{IS}	K_0	I_{OUT}=50mA, V_{DEN}=5V	-5%	380	+5%	
I_{OUT}/I_{IS}	K_1	I_{OUT}=0.1A, V_{DEN}=5V	-3%	425	+3%	
I_{OUT}/I_{IS}	K_2	I_{OUT}=0.5A, V_{DEN}=5V	-2.5%	455	+2.5%	
I_{OUT}/I_{IS}	K_3	I_{OUT}=1A, V_{DEN}=5V	-2.5%	460	+2.5%	
I_{OUT}/I_{IS}	K_4	I_{OUT}=2A, V_{DEN}=5V	-2.5%	465	+2.5%	
Current sense leakage current	I_{IS0}	CS disabled: V_{DEN} =0V	0		1	uA
		CS enabled: V_{DEN} = 5V, All channels ON, I_{OUTX} = 0A, :		25		
Output voltage for IS shutdown	V_{OUT_MSD}	V_{DEN}=5V, R_{SENSE}=3.9K, V_{IN0}=5V; V_{DSEL}=0V, I_{OUT0}=2A		5		V
Max analog sense output voltage	V_{IS}	V_S=28V, V_{IS} =5V	4.5			V
Current sense output current in fault condition	I_{ISH}	V_S=28V, V_{IS} =5V	10	20	30	mA
Current sense output voltage in fault condition	V_{ISH}	V_S=28V, V_{IS} =5V	5.4	6	6.6	V

OFF-state diagnostic

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
OFF-state open load voltage detection threshold（VS-OUT）	V_{OL}	V_{DEN}=5V, V_{IN}=0V, V_{DSEL}=0V	4	5	6	V
OFF-state output sink current	$I_{L(off2)}$	V_S=28V,V_{IN} = 0V, V_{OUT}=28V-V_{OL}, T_j = -40℃ to 150℃	-450	-350	-250	uA
OFF-state diagnostic delay time from falling edge of IN	t_{DSTKON}	V_{DEN}=5V, V_{IN0}= 5V to 0V, V_{DSEL}=0V, V_{OUT0} =V_S,	150	400	800	us
Settling time for valid OFF-state open load diagnostic indication from rising edge of DEN	$t_{D\_OL\_V}$	V_{IN0}=0V,V_{DSEL}=0V,V_{OUT0}=V_S, V_{DEN}=0V to 5V			150	us
OFF-state diagnostic delay time from rising edge of V_{OUT}	t_{D_VOL}	V_{DEN}=5V,V_{IN0}=0V,V_{DSEL}=0V, V_{OUT0}=V_S-6V to V_S		5	30	us

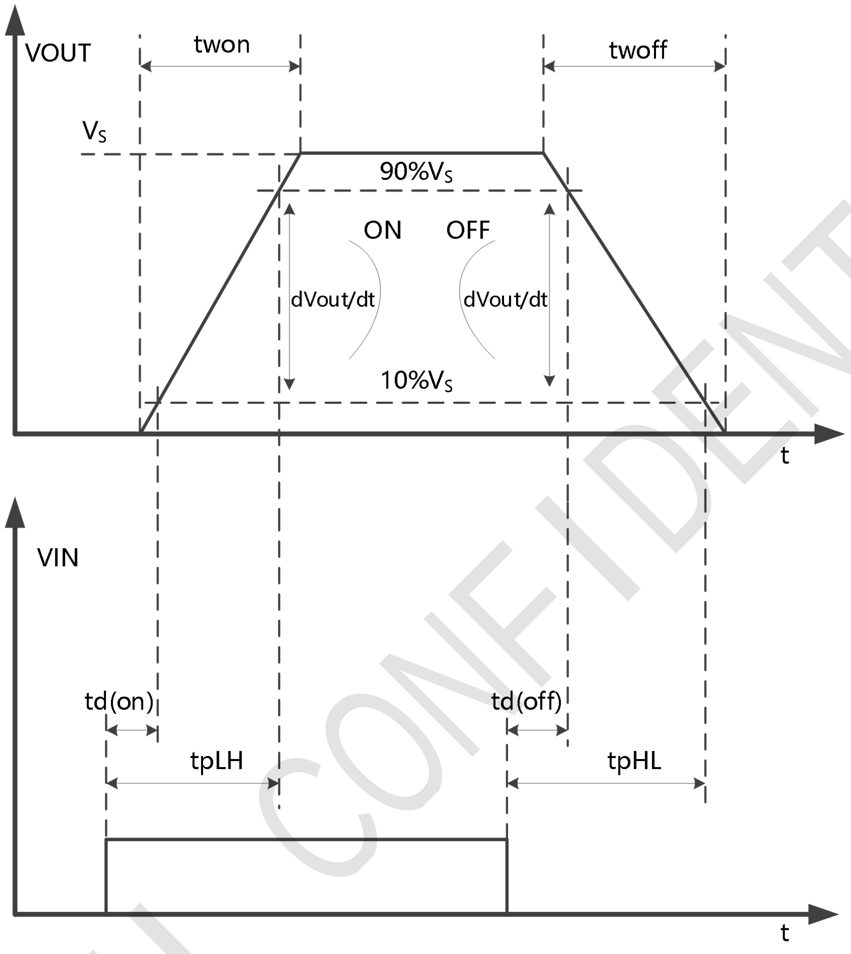
Current sense timings

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Current sense settling time from rising edge of DEN	$t_{DSENSE1H}$	V_{IN}=5V, V_{DEN}=0V to 5V, R_{SENSE}=1K, R_L=28Ω			100	us
Current sense disable delay time from falling edge of DEN	$t_{DSENSE1L}$	V_{IN}=5V, V_{DEN}=5V to 0V, R_{SENSE}=1K, R_L=28Ω		5	20	us
Current sense settling time from rising edge of IN	$t_{DSENSE2H}$	V_{IN}=0V to 5V, V_{DEN}=5 V, R_{SENSE} =1K, R_L=28Ω		80	250	us
Current sense settling time from rising edge of I_{OUT}(dynamic response to a step change of I_{OUT})	$\Delta t_{DSENSE2H}$	V_{IN}=5V, V_{DEN}=5V, R_{SENSE}=1K, I_{IS}=90% of I_{IS_MAX}, I_{OUT} = 90% of I_{OUTMAX} R_L=28Ω			150	us
Current sense turn-off delay time from falling edge of IN	$t_{DSENSE2L}$	V_{IN}=5V to 0V, V_{DEN}=5V, R_{SENSE}=1K, R_L=28Ω		80	250	us

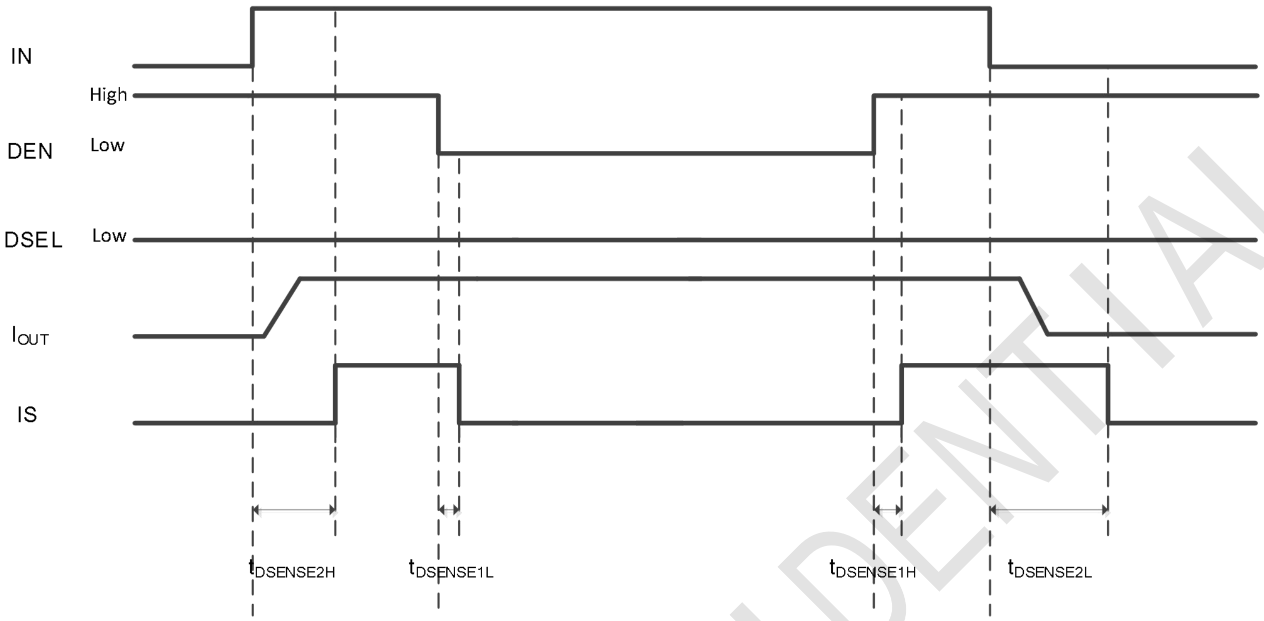
Note7: Except for the special test instructions, all electrical parameters are tested under T_A= +25℃. The minimum and maximum specification range of the specifications is guaranteed by the test, and the typical values are guaranteed by the design, test, or statistical analysis.

Switching Status and Timing Relationship

Switching time and pulse skew



Current sense timings (current sense mode)



T_{DSTKON}

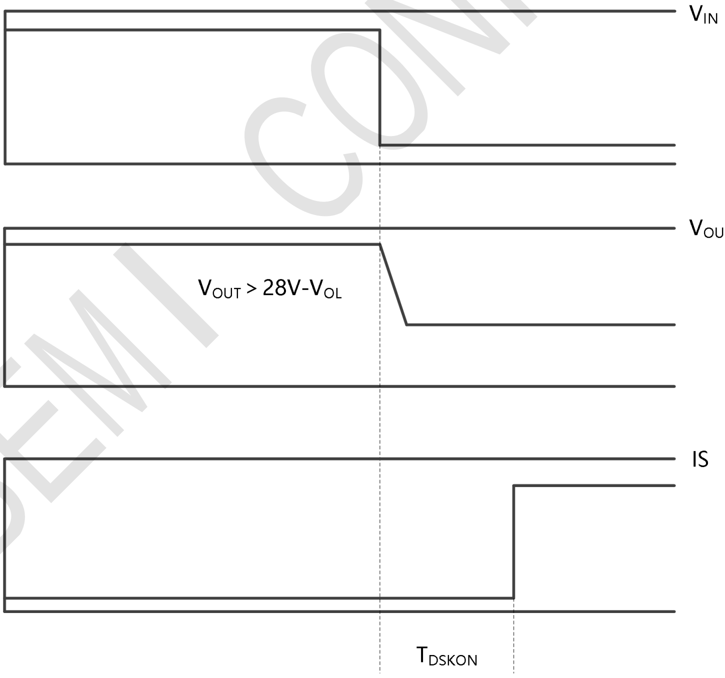


Table 2. Truth table

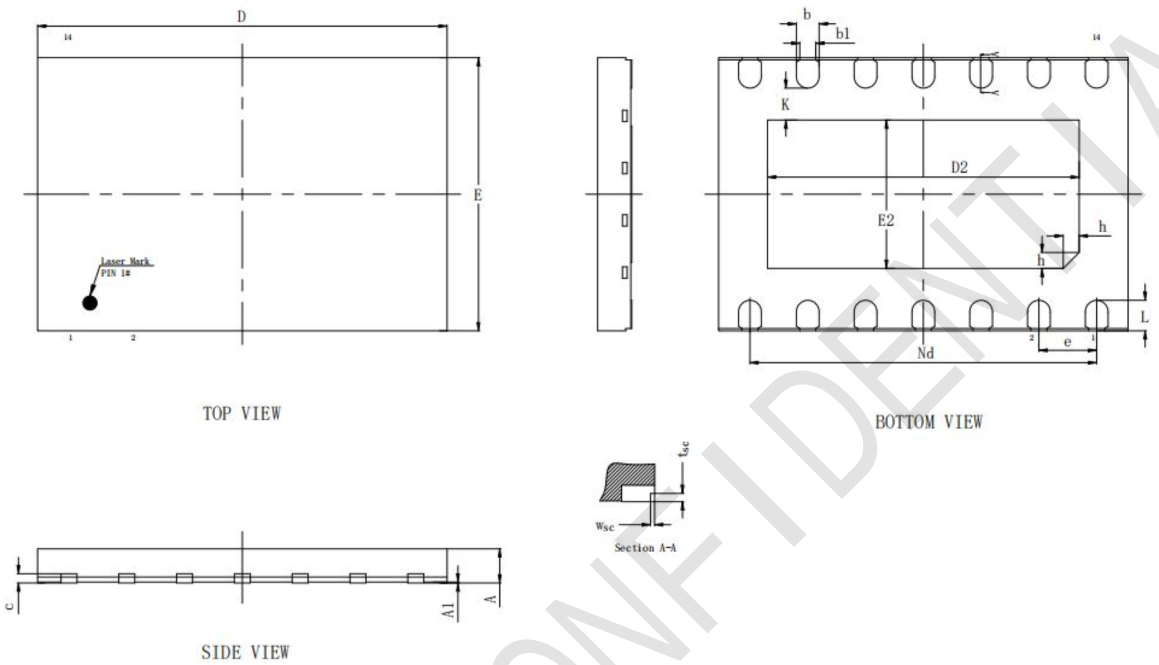
Conditions	IN_X	DEN	OUT_X	IS
Standby	L	L	L	0
Normal	L	H	L	0
	H	H	H	$I_{IS} = I_{OUT}/K$
Overload	H	H	H	I_{ISH}
OverTemperature	L	H	L	0
	H	H	H	I_{ISH}
Undervoltage	X	X	L	0
Short to V_S	L	H	H	I_{ISH}
	H	H	H	<Normal
Open-Load	L	H	H	I_{ISH}
Short circuit to GND	H	H	L	I_{ISH}

Table 3. Current sense output

DEN	DSEL1	DSEL0	MUX Channel	Current sense output			
				Normal	Overload	OFF-state	Negative output
L	X	X		Hi-Z			
H	L	L	Channel 0 diagnostic	$I_{IS} = I_{OUT0}/K$	$I_{IS} = I_{ISH}$	$I_{IS} = I_{ISH}$	Hi-Z
H	L	H	Channel 1 diagnostic	$I_{IS} = I_{OUT1}/K$	$I_{IS} = I_{ISH}$	$I_{IS} = I_{ISH}$	Hi-Z
H	H	L	Channel 2 diagnostic	$I_{IS} = I_{OUT2}/K$	$I_{IS} = I_{ISH}$	$I_{IS} = I_{ISH}$	Hi-Z
H	H	H	Channel 3 diagnostic	$I_{IS} = I_{OUT3}/K$	$I_{IS} = I_{ISH}$	$I_{IS} = I_{ISH}$	Hi-Z

Package Outline

DFN9×6-14L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.45	0.50	0.55
b1	0.35REF		
c	0.203REF		
D	8.90	9.00	9.10
D2	6.75	6.85	6.95
e	1.27BSC		
Nd	7.62BSC		
E	5.90	6.00	6.10
E2	3.16	3.26	3.36
L	0.62	0.67	0.72
h	0.30	0.35	0.40
K	0.70REF		
W_{SC}	0.01	-	0.09
t_{SC}	0.08	-	0.18

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