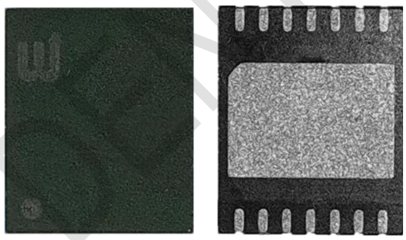
WS7020AF

Smart High-Side Power Switch Single Channel，23mΩ，DFN5×6-14L ，*AEC-Q100 qualified*

Application

- Suitable for resistive, inductive and capacitive loads
- Specially intended for automotive signal lamps
- Replaces electromechanical relays, fuses and discrete circuits

Package Information	
Package	DFN5×6-14L
Marking	WS7020AF



Basic Features

- Single channel device
- Standby current <1.0μA
- 3.3 V and 5 V compatible logic inputs
- RoHS compliant and lead free
- AEC-Q100 qualified

Product Summary

Parameter	Symbol	Value
Max. DC supply voltage	V_S	35V
Operating voltage range	V_{NOM}	4.5-28V
On-state resistance (per channel, Typ.)	R_{ON}	23mohm
Nominal load current	$I_{L(NOM)}$	7.5A
Typical current sense ratio (I_L=3A)	K	3160
Current limitation (typ.)	I_{LIMH}	24A
Supply current in standby mode	I_{STBY}	<1.0μA

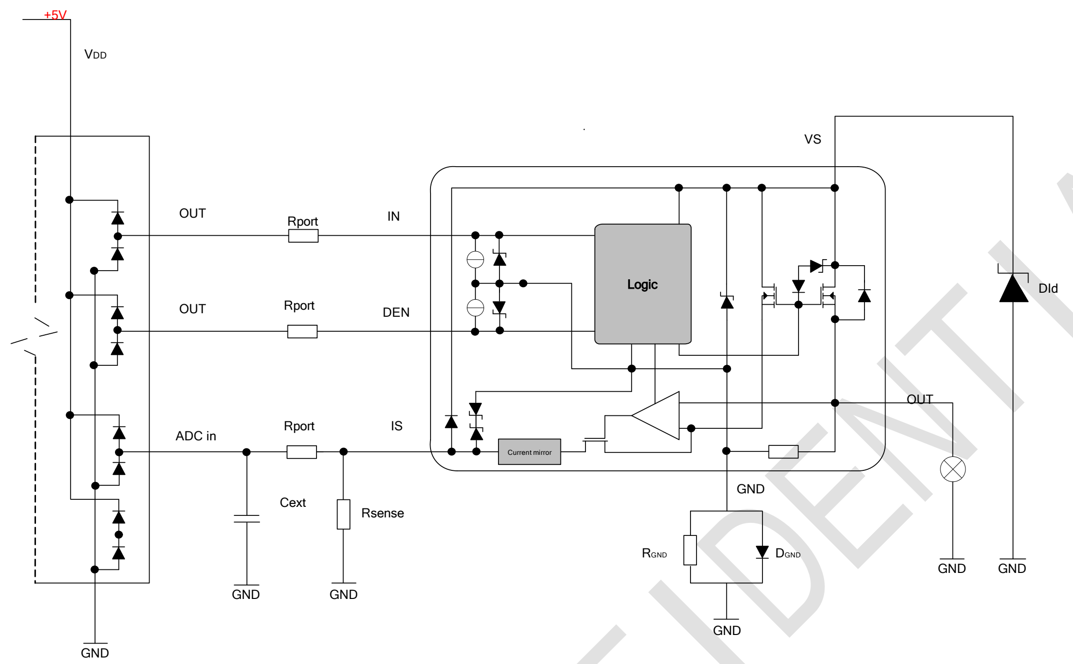
Diagnostic Functions

- Multiplexed analog feedback of load current with high precision proportional current mirror
- Off-state open load detection
- Output short to V_S detection

Protection Functions

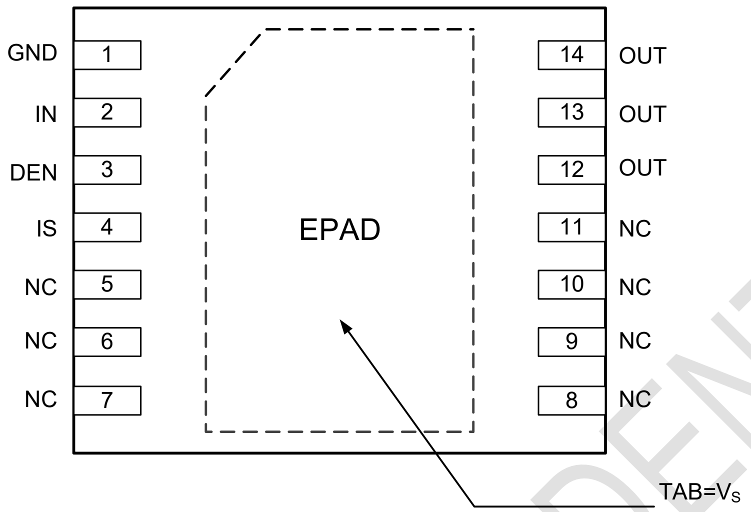
- Undervoltage shutdown
- Overvoltage clamp
- Load current limitation
- Output short-circuit protection
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of V_S
- Thermal shutdown indication
- Electrostatic discharge protection

Typical Application Circuit



Pin Configuration

Top view



DFN5×6-14L

Pin Description

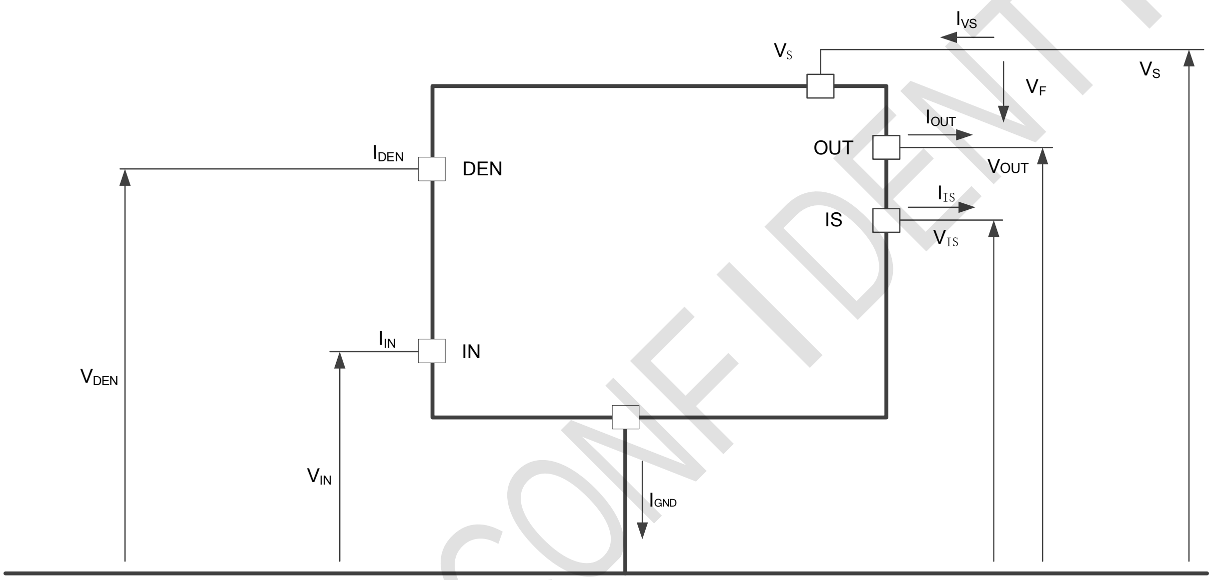
Pin Name	Pin NO.	Pin Description
GND	1	Ground connection. Must be reverse battery protected by an external diode / resistor network.
IN	2	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
DEN	3	Active high compatible with 3 V and 5 V CMOS outputs pin, it enables the IS diagnostic pin.
IS	4	Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic:
NC	5/6/7/8/9/10/11	No connect.
OUT	12/13/14	Power outputs.
V_S	EPAD	Battery connection.

Table 1. Suggested connections for unused and not connected pins

Connection / pin	IS	NC	OUT	IN	DEN
Floating	Not allowed	X(1)	X	X	X
To ground	Through 1K resistor	X	Not allowed	Through 15K resistor	Through 15K resistor

Note1：X do not care.

Current and Voltage Conventions



Note2: $V_F = V_{OUT} - V_S$ during reverse battery condition.

Absolute Maximum Ratings (Note3)

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	35	V
$-V_S$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUT DC output current	Internally limited	A
V_{IN}, V_{DEN}	IN, DEN DC input voltage	-0.3 to 6.0	V
I_{IS}	IS pin DC output current	20	mA
	IS pin DC output current in reverse	-20	
T_j	Junction operating temperature	-40 to 150	℃
T_{stg}	Storage temperature	-55 to 150	

Note3：Stressing the device above the rating listed in Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Thermal Resistance (Note4)

Symbol	Parameter	Value	Unit
T_{JC}	Thermal Resistance Junction-to-Case	1.3	℃/W
T_{JA}	Junction-to-Ambient Thermal Resistance	28	℃/W

Note4：According to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

ESD Susceptibility (Note5)

Symbol	Parameter	Values	Unit
$V_{ESD(HBM)}$ 3)	ESD Susceptibility all Pins (HBM)	±2	kV
$V_{ESD(HBM)\_OUT}$	ESD Susceptibility OUT vs GND and V_S connected (HBM)	±4	kV
$V_{ESD(CDM)}$ 4)	ESD Susceptibility all Pins (CDM)	±500	V
$V_{ESD(CDM)\_CRN}$	ESD Susceptibility Corner Pins (CDM) (pins 1,7,8,14)	±750	V

Note5：

1) Not subject to production test - specified by design.

2) Maximum digital input voltage to be considered for Latch-Up tests: 5.5 V.

3) ESD susceptibility, Human Body Model "HBM", according to AEC Q100-002.

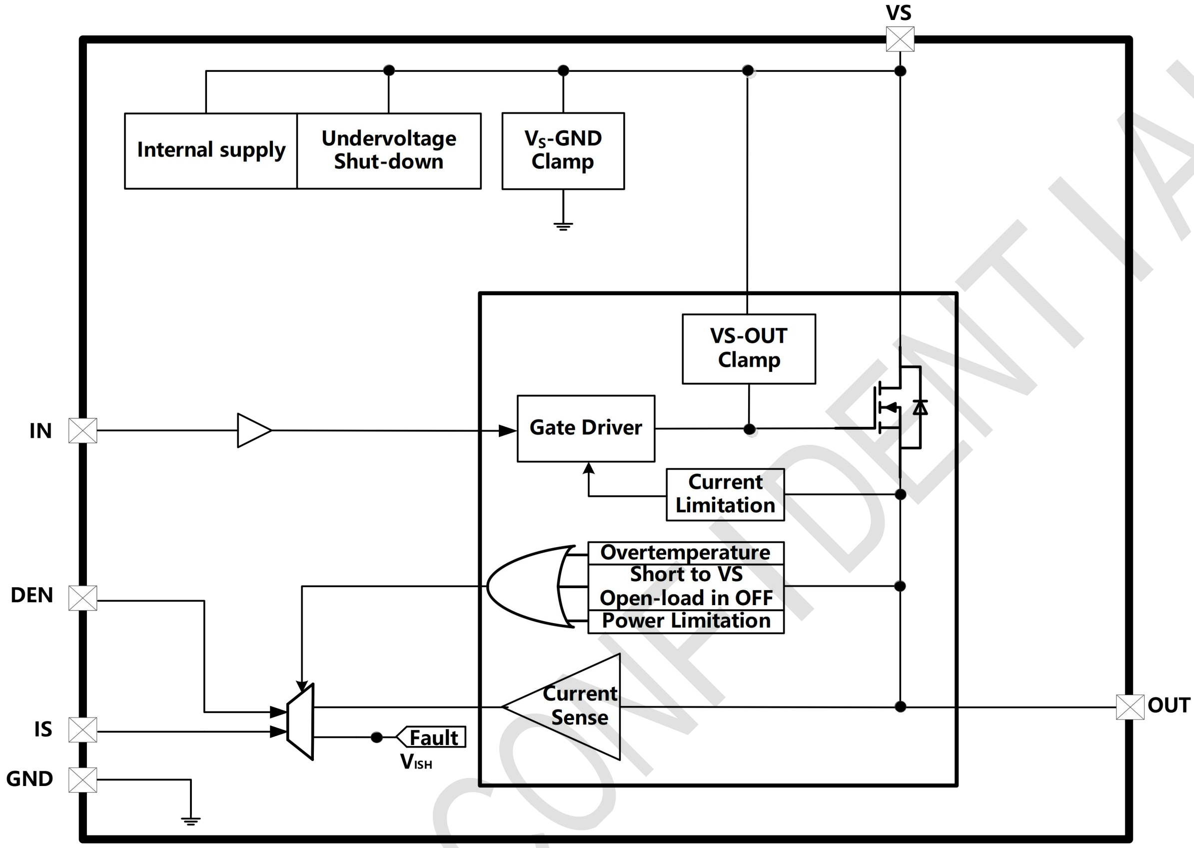
4) ESD susceptibility, Charged Device Model "CDM", according to AEC Q100-011.

EAS/EAR Susceptibility (Note6)

Symbol	Parameter	Values			Unit	Note or Test Conditon
		Min.	Typ.	Max.		
E_{AS}	Maximum Energy Dissipation Single Pulse			78	mJ	I_L = 2*$I_{L(NOM)\_85}$ $T_{J(0)}$ = 150 °C V_S = 28 V
E_{AR}	Maximum Energy Dissipation Repetitive Pulse			25	mJ	I_L = $I_{L(NOM)\_85}$ $T_{J(0)}$ = 85°C V_S = 13.5 V 1M Cycles
$\|I_L\|$	Load Current			I_{LIMH}	A	

Note6:：Not subject to production test - specified by design.

Functional Block



Electrical Characteristics (Note7)

Power section

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_S		4.5	13	28	V
Under voltage shutdown	V_{USD}				4.5	V
Under voltage shutdown reset	$V_{USDReset}$				5	V
Under voltage shutdown hysteresis	$V_{USDhyst}$			0.3		V
On-state resistance	R_{ON}	I_L=5A, T_j = 25℃		23		mΩ
		I_L=5A, T_j =150℃			50	
		I_L=5A, V_S=4.5V, T_j = 25℃			40	
Nominal load current	$I_{L(NOM)}$	T_A=25℃		7.5		A
Nominal load current at T_A=85℃	$I_{L(NOM)\_85}$	T_A=85℃, T_j < 150℃		6.0		A
Inverse Current Capability	$I_{L(INV)}$	V_S<V_{OUT}, V_{IN}=5V, T_A=25℃		7.5		A
V_S clamp voltage	V_{clamp}	I_S=20 mA, 25℃ < T_j < 150℃	35	42	48	V
		I_S=20 mA, T_j =-40℃	33			
Supply current in standby at V_S = 13 V	I_{STBY}	V_S = 13V, V_{IN}=V_{OUT}=V_{DEN}=0V, T_j =25℃			1.0	μA
		V_S =13V, V_{IN}=V_{OUT}=V_{DEN} =0V, T_j= 125℃			3.0	μA
Standby mode blanking time	t_{D_STBY}	V_S=13V, V_{IN}=V_{OUT}=0V V_{DEN}=5 V to 0 V	100	400	800	us
Supply current	$I_{S(ON)}$	V_S=13V, V_{DEN}=0V, V_{IN}=5V, I_L=0A		3	6	mA
Control stage current consumption in ON state	$I_{GND(ON)}$	V_S=13V, V_{DEN}=5V, V_{IN}=5V, I_L=5A			6	mA
Off-state output current at V_S =13V	$I_{L(off)}$	V_{IN} =V_{OUT}=0V, V_S =13V, T_j =25℃	0	0.05	0.5	μA
		V_{IN} =V_{OUT}=0V, V_S =13V, T_j =125℃	0		3.0	μA
OUT- V_S diode voltage at T_j=150℃	V_F	I_{OUT} =-0.2A, T_j =150℃			0.9	V

Switching/V_S = 13 V, -40℃ < T_j< 150℃, unless otherwise specified

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Turn-on delay time at T_j = 25℃	$T_{d\ (on)}$	R_L=2.6Ω	10	40	120	us
Turn-off delay time at T_j = 25℃	$T_{d\ (off)}$		10	75	120	us
Turn-on voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{on}$	R_L=2.6Ω	0.05	0.2	0.7	V/us
Turn-off voltage slope at T_j = 25℃	$(dV_{OUT}/dt)_{off}$		0.05	0.25	0.7	
Differential pulse skew(t_{PHL} - t_{PLH})	t_{SKEW}	R_L=2.6Ω	-90	-	60	us

Logic input (IN, DEN)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic input low level voltage	V_{LOW}				0.9	V
Low level logic input current	I_{LOW}	V_{INL}=0.9V	0.5			uA
Logic input high level voltage	V_{HIGH}		2.1		6.0	V
High level logic input current	I_{HIGH}	V_{INH}=2.1V			12	uA
Logic input hysteresis voltage	$V_{(hyst)}$		0.1	0.3	0.7	V

Protections (7 V < V_S< 18 V, -40℃ < T_j < 150℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
DC short circuit current	I_{LIMH}	V_S=13V	12	24	36	A
		4.5V < V_S< 18V			36	
Short circuit current during themal cycling	I_{LIML}	V_S=13V, T_R< T_j< T_{TSD}		9		
Shutdown temperature	T_{TSD}		150	175	200	℃
Thermal hysteresis	T_{HYST}			20		℃
Dynamic temperature	ΔT_{J_SD}	T_j = -40℃, V_S=13V		60		℃
Current limit thermal hysteresis	T_R			40		℃
Turn-off output voltage clamp	V_{DEMAG}	I_L=2A, L= 6mH, T_j = -40℃	V_S-33			V
		I_L=2A, L= 6mH, T_j =25℃ to 150℃	V_S-35	V_S-38	V_S-43	

Current sense / 7 V < V_S< 18 V, -40℃ < T_j < 150℃

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Current sense clamp voltage	V_{IS_CL}	V_{DEN}=0V, I_{IS} =1mA		-15		V
		V_{DEN}=0V, I_{IS} = -1mA		7		

Current sense characteristics

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
I_L/I_{IS}	K_1	I_L=0.5A, V_{DEN}=5V	-50%	2100	+50%	
I_L/I_{IS}	K_2	I_L=1A, V_{DEN}=5V	-30%	2680	+30%	
I_L/I_{IS}	K_3	I_L=3A, V_{DEN}=5V	-15%	3160	+15%	
I_L/I_{IS}	K_4	I_L=8A, V_{DEN}=5V	-10%	3360	+10%	
Current sense leakage current	I_{IS0}	CS disabled: V_{DEN} =0V	0		0.5	uA
		CS disabled: -1V<V_{IS}<5V	-0.5		3	
		CS enabled: V_{DEN}=5V, V_{IN}= 5V, I_L=0A	0		200	
		CS enabled: V_{DEN}=5V, V_{IN}= 0V, I_L=0A	0		2	
Output voltage for CS shutdown	V_{OUT_MSD}	V_{DEN}=5V, R_{SENSE} =2.7K, V_{IN}=5V;I_L=5A		5		V
CS saturation voltage	V_{IS_SAT}	V_S=7V, R_{SENSE}=2.7K,V_{DEN}=5V,V_{IN}=5V, I_L =16A, T_j =150 ℃	5			V
CS saturation current	I_{IS_SAT}	V_S=7V, V_{IS}=4V, V_{IN}=5V, V_{DEN}=5V, T_j =150℃	4			mA
Output saturation current	I_{OUT_SAT}	V_S=7V, V_{IS}=4V, V_{IN}=5V, V_{DEN}=5V T_j =150 ℃	20			A

OFF-state diagnostic

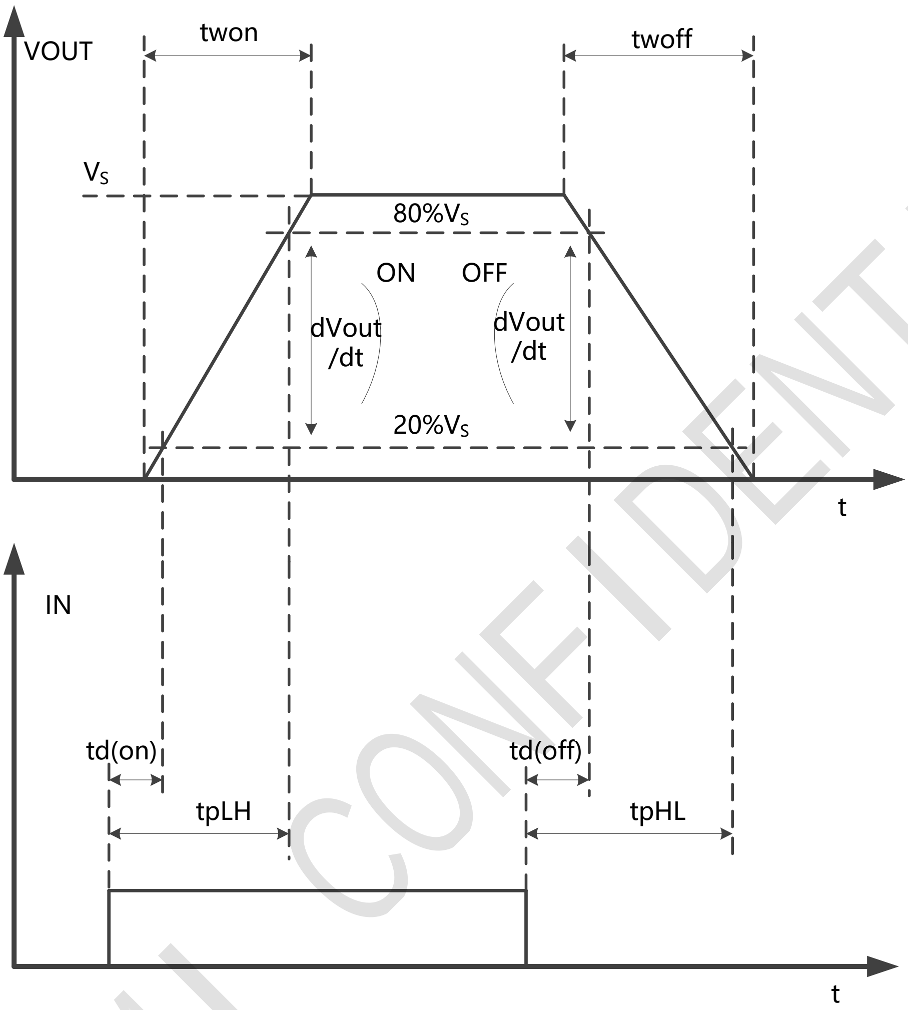
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
OFF-state open load voltage detection threshold	V_{OL}	V_{DEN}=5V, V_{IN}=0V	2	3	4	V
OFF-state output sink current	$I_{L(off2)}$	V_{IN} = 0 V, V_{OUT} = V_{OL},T_j = -40℃ to 150℃	-900	-400	-160	uA
OFF-state diagnostic delay time from falling edge of IN	t_{DSTKON}	V_{DEN}=5V, V_{IN}= 5V to 0 V, V_{OUT}=4V I_L =0A	100	350	700	us

Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn	$t_{D\_OL\_V}$	V_{IN}=0V,V_{OUT}=4V, V_{DEN} = 0V to 5V			150	us
OFF-state diagnostic delay time from rising edge of V_{OUT}	t_{D_VOL}	V_{DEN}=5V,V_{IN}=0V, V_{OUT}=0V to 4V		5	30	us
Fault diagnostic feedback						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Current sense output voltage in fault condition	V_{ISH}	V_S=13V, R_{SENSE} =1K, V_{IN}=0V, V_{DEN} = 5V, I_L=0A,V_{OUT}=4V	5.0	6.0	6.6	V
Current sense output current in fault condition	I_{ISH}	V_S=13V, V_{IS} =5V	10	20	30	mA
Current sense timings						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Current sense settling time from rising edge of DEN	$t_{DSENSE1H}$	V_{IN}=5V, V_{DEN}=0V to 5V, R_{SENSE}=1K, R_L=2.6Ω			100	us
Current sense disable delay time from falling edge of DEN	$t_{DSENSE1L}$	V_{IN}=5V, V_{DEN}=5V to 0V, R_{SENSE}=1K, R_L=2.6Ω		5	20	us
Current sense settling time from rising edge of IN	$t_{DSENSE2H}$	V_{IN}=0V to 5V, V_{DEN}=5 V, R_{SENSE} =1K, R_L=2.6Ω		80	250	us
Current sense settling time from rising edge of I_{OUT}(dynamic response to a step change of I_{OUT})	$\Delta t_{DSENSE2H}$	V_{IN}=5V,V_{DEN}=5V,R_{SENSE}=1K, I_{IS}=90% of $I_{IS,MAX}$, R_L=2.6Ω			150	us
Current sense turn-off delay time from falling edge of IN	$t_{DSENSE2L}$	V_{IN}=5V to 0V, V_{DEN}=5V, R_{SENSE}=1K, R_L=2.6Ω		80	250	us

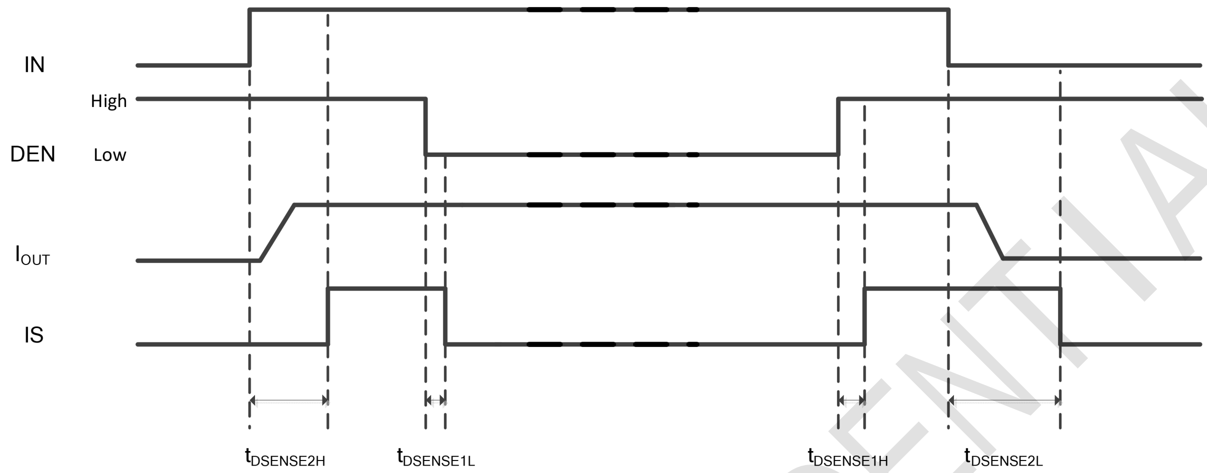
Note7: Except for the special test instructions, all electrical parameters are tested under T_A= +25℃. The minimum and maximum specification range of the specifications is guaranteed by the test, and the typical values are guaranteed by the design, test, or statistical analysis.

Switching Status and Timing Relationship

Switching time and pulse skew



Current sense timings (current sense mode)



T_{DSTKON}

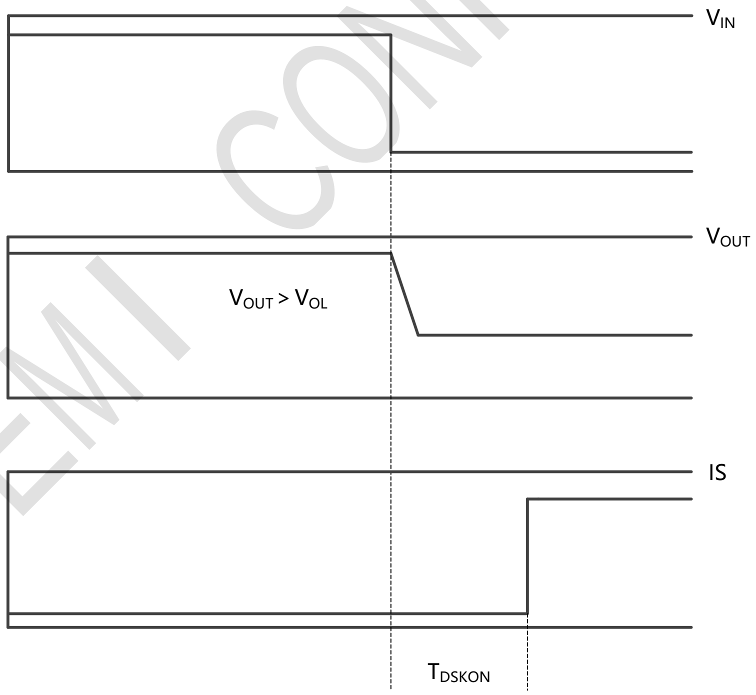


Table 2. Truth table

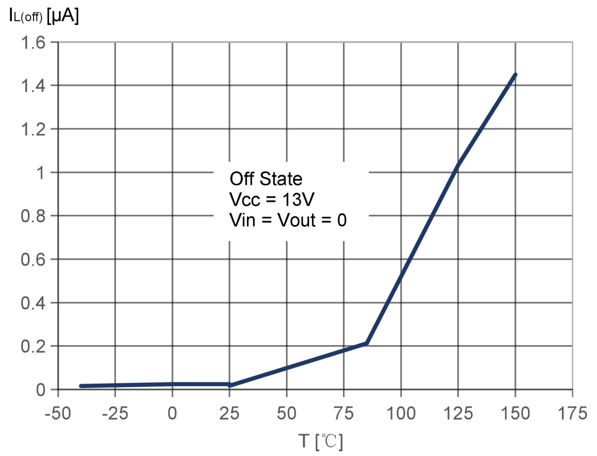
Mode	Conditions	IN	DEN	OUT	IS	Comments
Standby	All logic INs low	L	L	L	Hi-Z	Low quiescent current consumption
Normal	Nominal load connected; $T_j < 150℃$	L	See Table 3	L	See Table 3	
		H		H	See Table 3	Outputs configured for auto-restart
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j\_SD}$	L	See Table 3	L	See Table 3	
		H		H	See Table 3	Output cycles with temperature hysteresis
Undervoltage	$V_S < V_{USD}$	X	X	L	Hi-Z	Re-start when $V_S > V_{USD} + V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_S	L	See Table 3	H	See Table 3	
	Open-Load	L		H	See Table 3	External pull-up
Negative output voltage	Inductive loads turn-off	L	See Table 3	<0	See Table 3	

Table 3. Current sense output

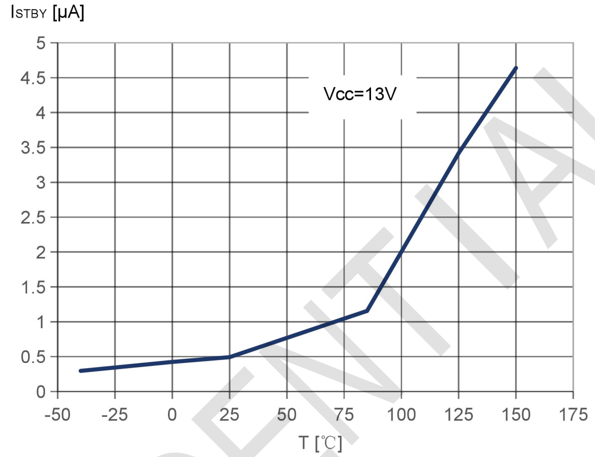
DEn	MUX Channel	Current sense output			
		Normal	Overload	OFF-state	Negative output
L		Hi-Z			
H	Channel diagnostic	$I_{IS} = I_{OUT}/K$	$V_{IS} = V_{ISH}$	$V_{IS} = V_{ISH}$	Hi-Z

Electrical Characteristics Curves

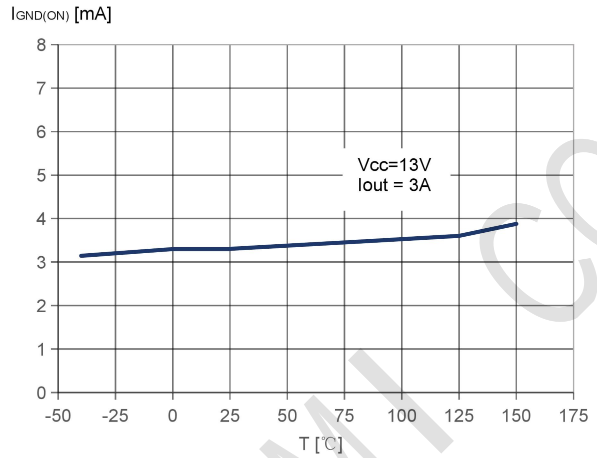
OFF-state output current



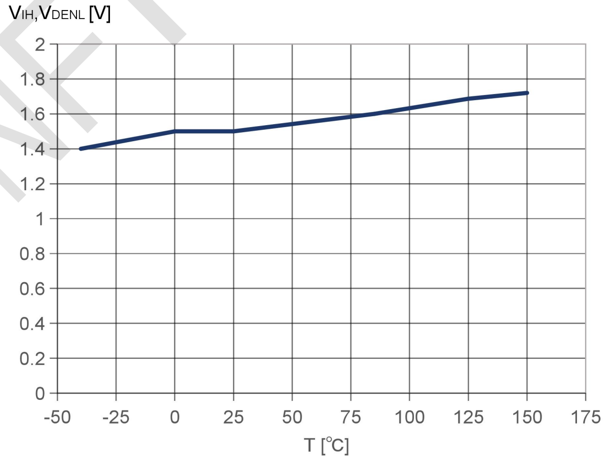
Standby current



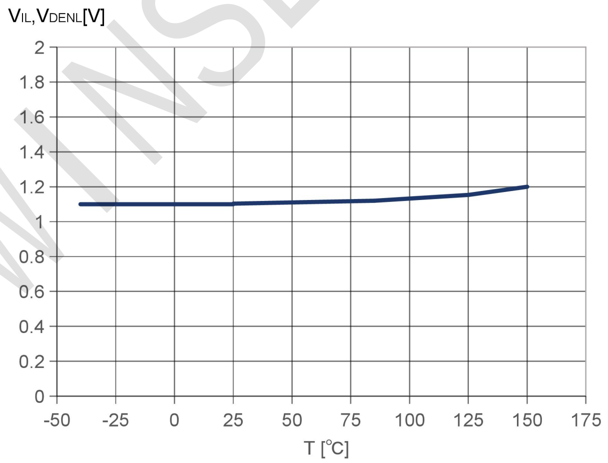
IGND(ON) vs. TA



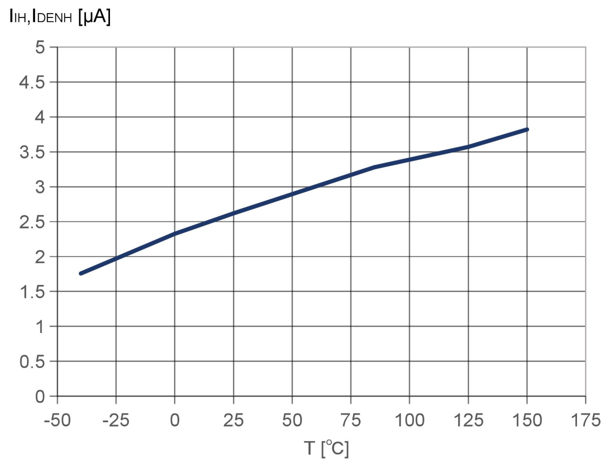
Logic Input high level voltage



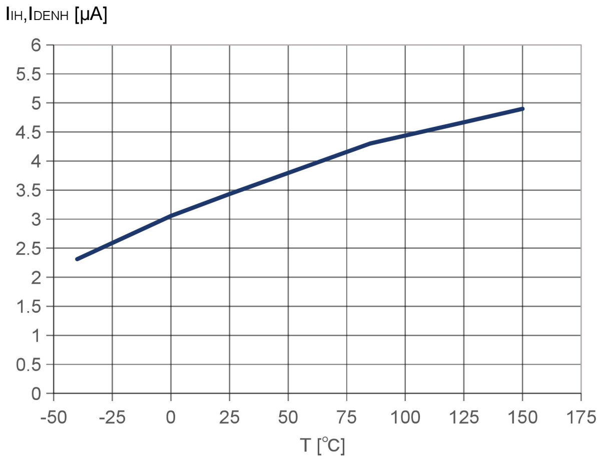
Logic Input Low level voltage



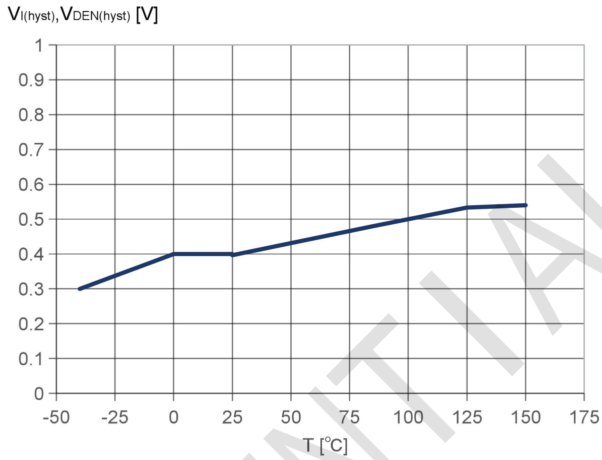
High level logic input current



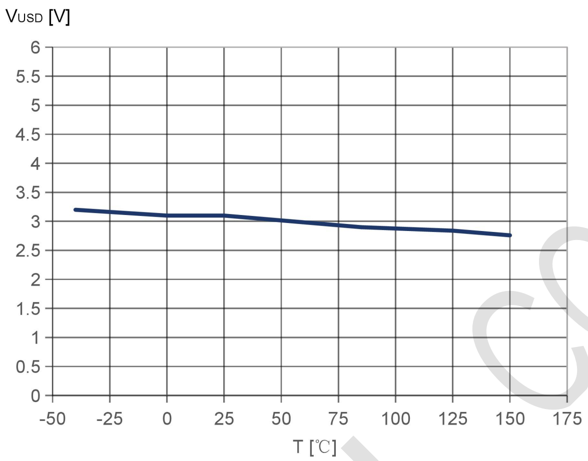
Low level logic input current



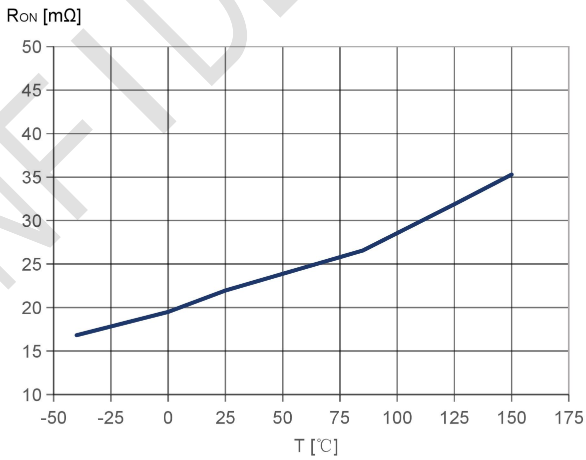
Logic Input hysteresis voltage



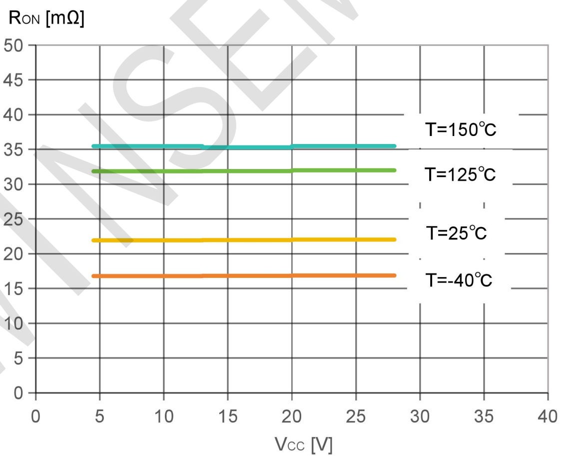
Undervoltage shutdown



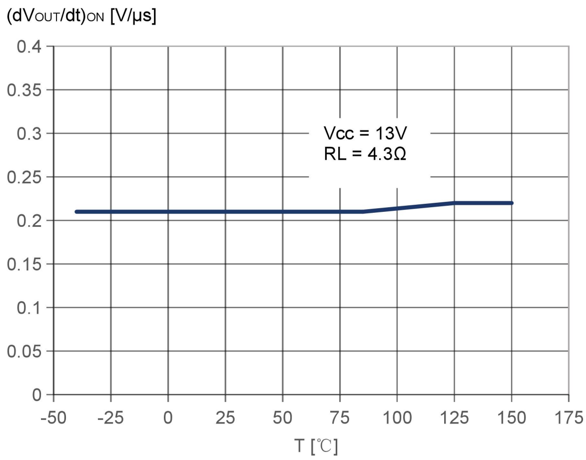
On-state resistance vs. TA



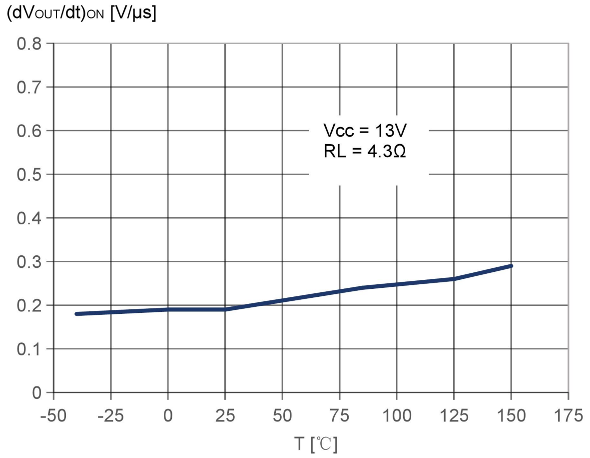
On-state resistance vs. TA



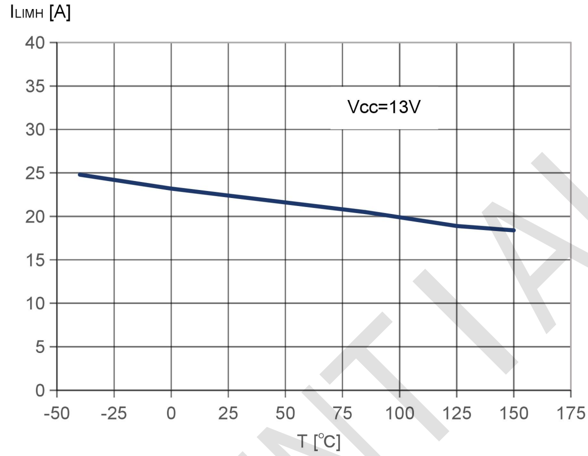
Turn-on voltage slope



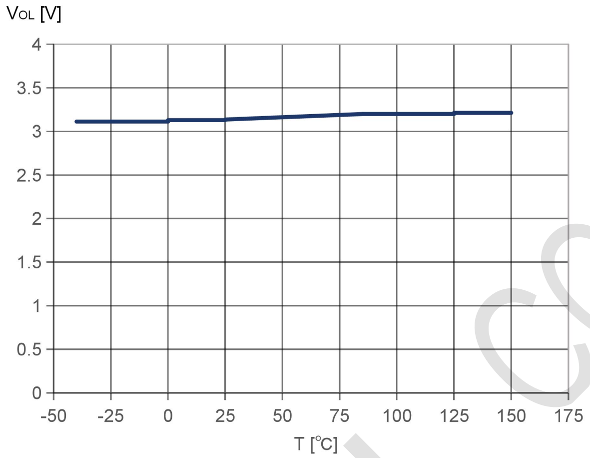
Turn-off voltage slope



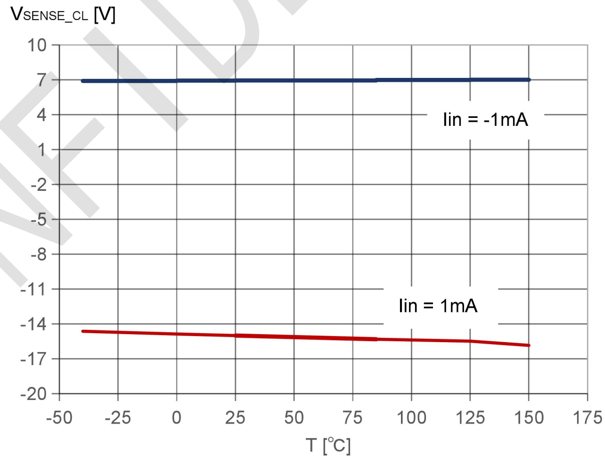
ILIMH vs. TA



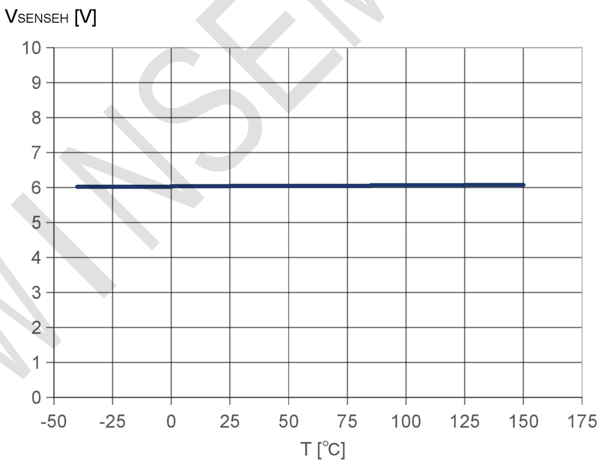
OFF-state open-load voltage detection threshold



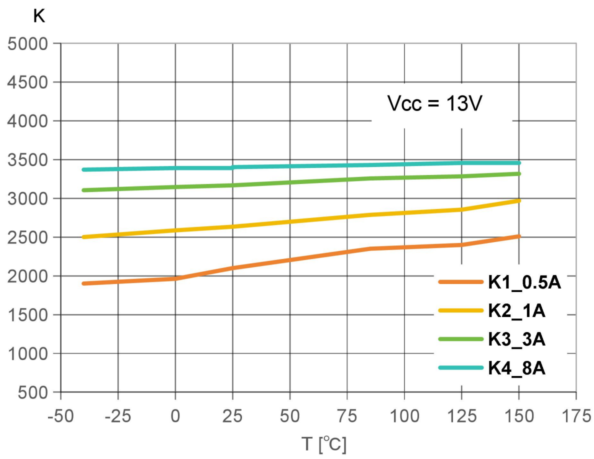
VIS_Clamp vs. TA



VISH vs. TA



IL / IIS vs. TA



Functional Description

Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_j through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_j exceeds the safety level of ΔT_{j_SD}. The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175℃), it automatically switches off and the diagnostic indication is triggered.

Current limitation

The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH}, by operating the output power MOSFET in the active region.

Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMAG}, allowing the inductor energy to be dissipated without damaging the device.

Diode (D_{GND}) in the ground line

A resistor (typ.R_{GND}=4.7K) should be inserted in parallel to D_{GND} if the device drives an inductive load. This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_S line, the control pins will be pulled negative. WS suggests to insert a resistor (R_{prot}=15K) in line both to prevent the micro-controller I/O pins from latching-up and to protect the HSD inputs. The value of these resistors is a compromise between the leakage current of micro-controller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of micro-controller I/Os.

IS - analog current sense

Diagnostic information on device and load status are provided by an analog output pin (IS) delivering the following signals:

- Current monitor: current mirror of channel output current

The signal are routed through an analog multiplexer which is configured and controlled by means of DEN pin, according to the address map in IS multiplexer addressing Table.

Current monitor

When current mode is selected in the IS, this output is capable to provide:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to known ratio named K
- Diagnostics flag in fault conditions delivering fixed voltage V_{ISH}

The current delivered by the current sense circuit, I_{IS} can be easily converted to a voltage V_{IS} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

While device is operating in normal conditions (no fault intervention), V_{IS} calculation can be done using simple equations.

Current provided by IS output: $I_{IS} = I_{OUT}/K$

Voltage on R_{SENSE}: $V_{IS} = R_{SENSE}*I_{IS} = R_{SENSE}*\ I_{OUT}/K$

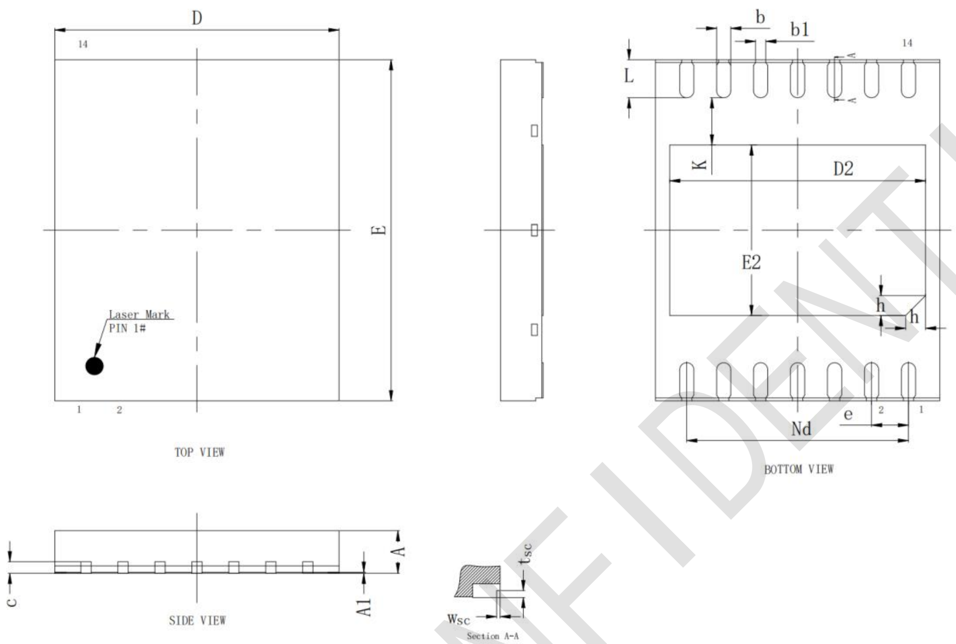
Where:

- V_{IS} is voltage measurable on R_{SENSE} resistor

I_{IS} is current provided from IS pin in current output mode

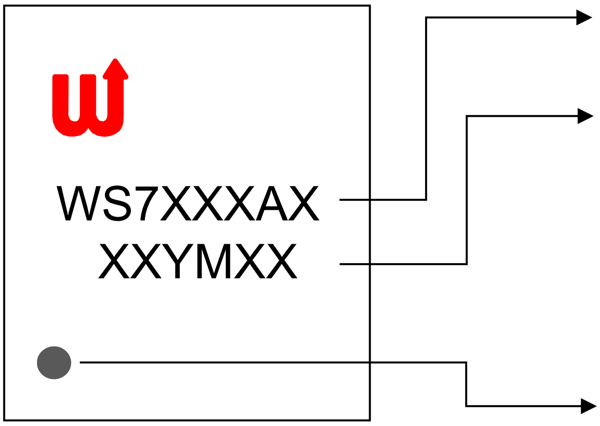
Package Outline

DFN5×6-14L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.203REF		
D	4.90	5.00	5.10
D2	4.40	4.50	4.60
e	0.65BSC		
Nd	3.90BSC		
E	5.90	6.00	6.10
E2	2.90	3.00	3.10
L	0.62	0.67	0.72
h	0.30	0.35	0.40
K	0.83REF		
W_{SC}	0.01	-	0.09
t_{SC}	0.08	-	0.18

Marking Information



Product Name

Internal control code

1）XX：Wafer Information

2）Y：The last digit of the year

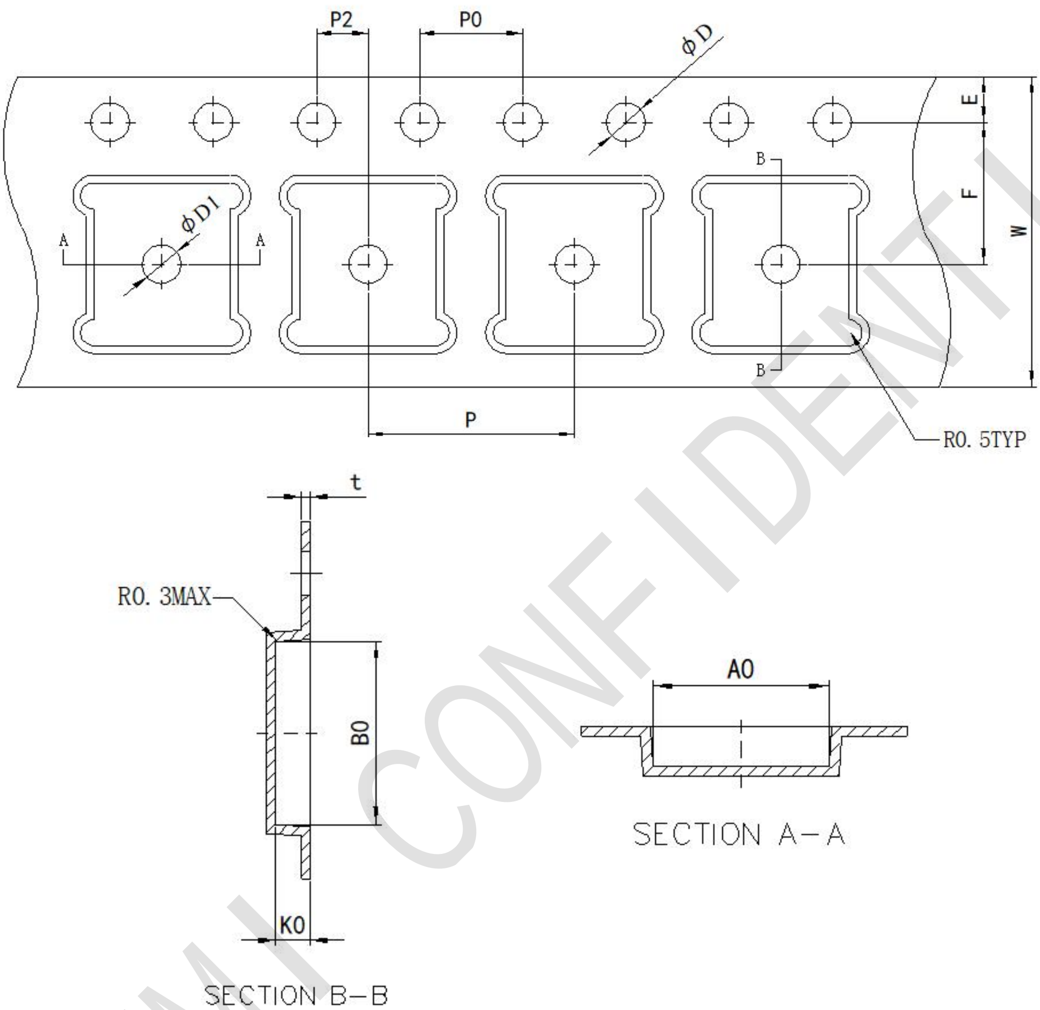
3）M：Production month，1-9/A/B/C

4）XX：Internal quality control code

The mark of PIN1

Tape and Reel Information

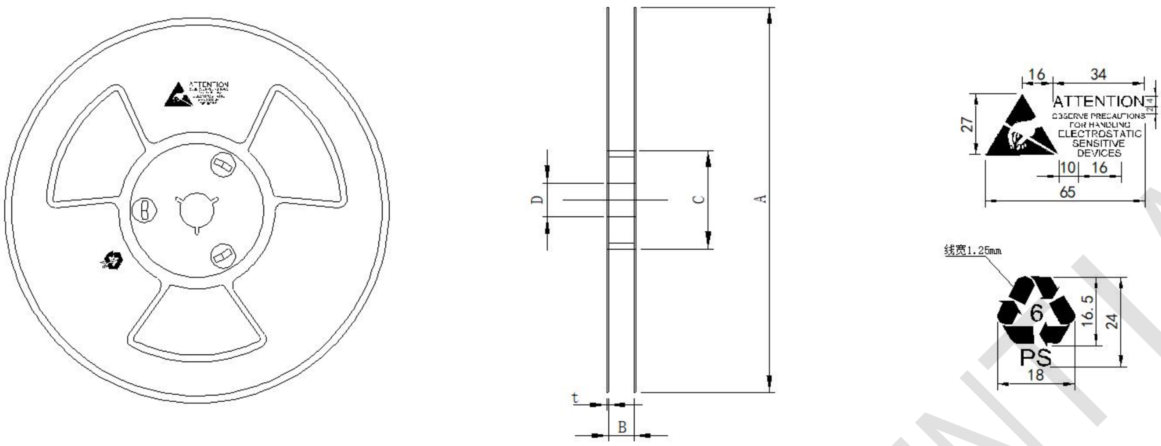
DFN5×6-14L Carrier tape



DFN5×6-14L Carrier Tape Dimensions

Description	Value（Unit：mm）
E	1.75±0.10
F	5.50±0.05
P2	2.00±0.05
D	1.50±0.1
D1	1.50 MIN
P0	4.00±0.10
W	12.00±0.1
P	8.00±0.10
A0	5.30±0.10
B0	6.30±0.10
K0	1.20±0.10

DFN5×6-14L Reel（13＂）



DFN5×6-14L Reel Dimensions

Description	Value（Unit：mm）
Carrier width	12
A	329±1
B	12.4+2
C	100±1
D	13.3±0.3
t	2.0±0.3

Tape and Reel Information

Package	Reel	QTY/Reel	Reel/Inner Box	Inner Box/Carton	QTY/Carton	Inner Box Size (mm)	Carton Size（mm）
DFN5×6-14L	13＂	3000	1	8	24000	336×336×48	420×355×365

CONTACT

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