



SWITCHMODE LEAD-ACID BATTERY CHARGER

Check for Samples: [UC2909-EP](#)

FEATURES

- Accurate and Efficient Control of Battery Charging
- Average Current Mode Control from Trickle to Overcharge
- Resistor Programmable Charge Currents
- Thermistor Interface Tracks Battery Requirements Over Temperature
- Output Status Bits Report on Four Internal Charge States
- Undervoltage Lockout Monitors VCC and VREF

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

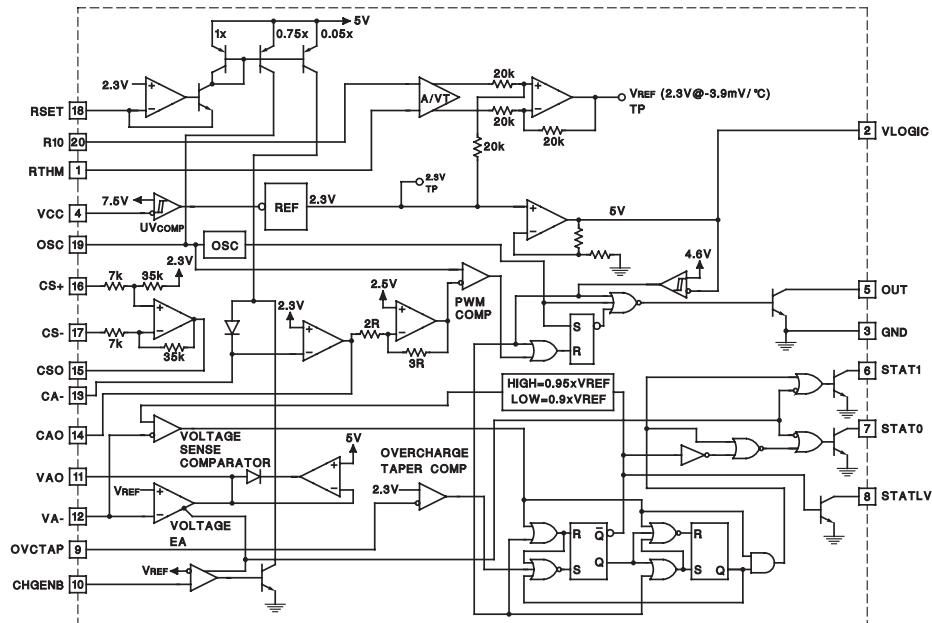
- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Military ($-55^{\circ}\text{C}/125^{\circ}\text{C}$) Temperature Range⁽¹⁾
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability
- Not to Exceed 185.35-KHz Oscillation Frequency at 125°C

(1) Additional temperature ranges available - contact factory

DESCRIPTION

The UC2909 controls lead acid battery charging with a highly efficient average current mode control loop. This chip combines charge state logic with average current PWM control circuitry. Charge state logic commands current or voltage control depending on the charge state. The chip includes undervoltage lockout circuitry to insure sufficient supply voltage is present before output switching starts. Additional circuit blocks include a differential current sense amplifier, a 1.5% voltage reference, a $-3.9\text{-mV}/^{\circ}\text{C}$ thermistor linearization circuit, voltage and current error amplifiers, a PWM oscillator, a PWM comparator, a PWM latch, charge state decode bits, and a 100-mA open collector output driver.

FUNCTION BLOCK DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	DW	UC2909MDWREP	UC2909EP

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

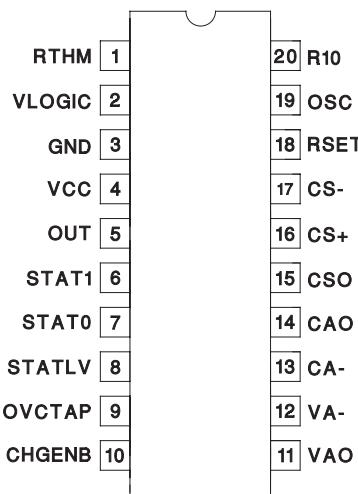
ABSOLUTE MAXIMUM RATINGS^{(1) (2)}

over operating free-air temperature range unless otherwise noted

			UNITS
VCC	Supply voltage	OUT, STAT0, STAT1	V
	Output current sink		A
CS+, CS-		-0.4 to V _{CC} ⁽³⁾	V
Remaining pin voltages		-0.3 to 9	V
T _{stg}	Storage temperature	-55 to 150	°C
T _J	Junction temperature range	-55 to 150	°C
	Lead temperature (soldering, 10 seconds)	300	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
- (2) All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.
- (3) Voltages more negative than -0.4 V can be tolerated if current is limited to 50 mA.

**DW PACKAGE
(TOP VIEW)**



ELECTRICAL CHARACTERISTICS

$T_A = -55^\circ\text{C}$ to 125°C ; $C_T = 430 \text{ pF}$, $R_{SET} = 11.5 \text{ k}\Omega$, $R_{10} = 10 \text{ k}\Omega$, $R_{THM} = 10 \text{ k}\Omega$, $V_{CC} = 15 \text{ V}$, Output no load, $R_{STAT0} = R_{STAT1} = 10 \text{ k}\Omega$, $CHGENB = OVCTAP = VLOGIC$, $T_A = T_J$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE AMPLIFIER (CSA) ($V_{ID} = CS+ - CS-$)						
DC gain		CS- = 0 V, CS+ = -50 mV; CS+ = -200 mV	4.8	5	5.7	V/V
		CS+ = 0 V, CS- = 50 mV; CS- = 250 mV	4.8	5	5.1	
V_{OFFSET}	Offset voltage ($V_{CSO} - V_{CAO}$)	CS+ = CS- = 2.3 V, CAO = CA-			45	mV
CMRR		$V_{CM} = -0.2 \text{ V}$ to $V_{CC} - 2$, $8.8 \text{ V} < V_{CC} < 14 \text{ V}$	50			dB
		$V_{CM} = -0.2 \text{ V}$ to V_{CC} , $14 \text{ V} < V_{CC} < 35 \text{ V}$	50			
V_{OL}		$V_{ID} = -550 \text{ mV}$, $-0.2 \text{ V} < V_{CM} < V_{CC} - 2$, $I_O = 500 \mu\text{A}$		0.3	0.6	V
V_{OH}		$V_{ID} = 700 \text{ mV}$, $-0.2 \text{ V} < V_{CM} < V_{CC} - 2$, $I_O = -250 \mu\text{A}$	5.2	5.7	6.2	V
Output source current		$V_{ID} = 700 \text{ mV}$, CSO = 4 V		-1	-0.5	mA
Output sink current		$V_{ID} = -550 \text{ mV}$, CSO = 1 V	3	4.5		mA
3dB bandwidth ⁽¹⁾		$V_{ID} = 90 \text{ mV}$, $V_{CM} = 0 \text{ V}$		200		KHz
CURRENT ERROR AMPLIFIER (CEA)						
I_B		$8.8 \text{ V} < V_{CC} < 35 \text{ V}$, $V_{CHGENB} = V_{LOGIC}$	0.1	0.8		μA
$V_{IO}^{(2)}$		$8.8 \text{ V} < V_{CC} < 35 \text{ V}$, CAO = CA-		10		mV
A_{VO}		$1 \text{ V} < V_{AO} < 4 \text{ V}$	60	90		dB
GBW		$T_J = 25^\circ\text{C}$, $f = 100 \text{ KHz}$	1	1.5		MHz
V_{OL}		$I_O = 250 \mu\text{A}$		0.4	0.6	V
V_{OH}		$I_O = -5 \text{ mA}$	4.5	5		V
Output source current		CAO = 4 V		-25	-12	mA
Output sink current		CAO = 1 V	2	3		mA
I_{CA-} , I_{TRCK_CONTRO} L		$V_{CHGENB} = GND$	8.5	10	11.5	μA
VOLTAGE AMPLIFIER (CEA)						
I_B		Total bias current; regulating level	0.1	1		μA
$V_{IO}^{(2)}$		$8.8 \text{ V} < V_{CC} < 35 \text{ V}$, $V_{CM} = 2.3 \text{ V}$, $V_{AO} = V_A-$		1.2		mV
A_{VO}		$1 \text{ V} < CAO < 4 \text{ V}$	60	90		dB
GBW		$T_J = 25^\circ\text{C}$, $f = 100 \text{ KHz}$	0.25	0.5		MHz
V_{OL}		$I_O = 500 \mu\text{A}$		0.4	0.6	V
V_{OH}		$I_O = -500 \mu\text{A}$	4.75	5	5.25	V
Output source current		CAO = 4 V	-2	-1		mA
Output sink current		CAO = 1 V	2	2.5		mA
VAO leakage: high impedance state		$V_{CHGENB} = GND$, $STAT0 = 0$ and $STAT1 = 0$, $V_{AO} = 2.3 \text{ V}$	-1		1	μA

(1) Not tested in production.

(2) V_{IO} is measured prior to packaging with internal probe pad.

ELECTRICAL CHARACTERISTICS (continued)

$T_A = -55^\circ\text{C}$ to 125°C ; $C_T = 430 \text{ pF}$, $R_{SET} = 11.5 \text{ K}\Omega$, $R_{10} = 10 \text{ K}\Omega$, $R_{THM} = 10 \text{ K}\Omega$, $V_{CC} = 15 \text{ V}$, Output no load, $R_{STAT0} = R_{STAT1} = 10 \text{ K}\Omega$, CHGENB = OVCTAP = VLOGIC, $T_A = T_J$ (unless otherwise noted)

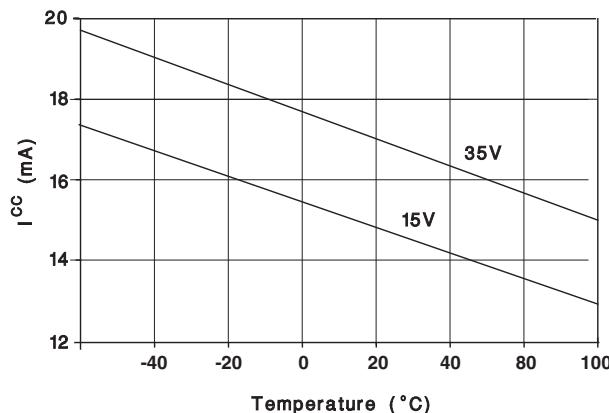
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PULSE WIDTH MODULATOR					
Maximum duty cycle	CAO = 0.6 V	90	95	100	%
Modulator gain	CAO = 2.5 V, 3.2 V	63	71	80	%/V
OSC peak			3		V
OSC valley			1		V
OSCILLATOR					
Frequency	8.8 V < V_{CC} < 35 V	151.65	168.50	185.35	KHz
THERMISTOR DERIVED ($V_{ID} = V_{RTHM} - V_{R10}$)					
Initial accuracy, V_{AO} ($R_{THM} = 10 \text{ K}\Omega$)	$V_{ID} = 0 \text{ V}$, $R_{10} = R_{THM} = 10 \text{ K}\Omega^{(3)}$	2.250	2.300	2.350	V
Line regulation	$V_{CC} = 8.8 \text{ V}$ to 35 V		3	10	mV
V_{AO}	$R_{THM} = 138 \text{ K}\Omega$, $R_{10} = 10 \text{ K}\Omega$	2.435	2.495	2.545	V
	$R_{THM} = 33.63 \text{ K}\Omega$, $R_{10} = 10 \text{ K}\Omega$	2.340	2.398	2.446	
	$R_{THM} = 1.014 \text{ K}\Omega$, $R_{10} = 10 \text{ K}\Omega$	2.015	2.066	2.107	
CHARGE ENABLE COMPARATOR (CEC)					
Threshold voltage	As a function of V_{A-}	0.99	1	1.01	V/V
Input bias current	CHGENB = 2.3 V	-0.5	-0.1		μA
VOLTAGE SENSE COMPARATOR (VSC)					
Threshold voltage	STAT0 = 0, STAT1 = 0, Function of V_{REF}	0.944	0.95	0.955	V/V
	STAT0 = 1, STAT1 = 0, Function of V_{REF}	0.895	0.9	0.905	
OVER CHARGE TAPER CURRENT COMPARATOR (OCTIC)					
Threshold voltage	Function of 2.3 V REF, CA- = CAO	0.99	1	1.01	V/V
Input bias current	OVCTAP = 2.3 V	-0.5	-0.1		μA
LOGIC 5 V (VLOGIC)					
VLOGIC	$V_{CC} = 15 \text{ V}$	4.875	5	5.125	V
Line regulation	8.8 V < V_{CC} < 35 V		3	15	mV
Load regulation	0 A < I_O < 10 mA		3	15	mV
Reference comparator turn-on threshold			4.3	4.85	V
Short circuit current	$V_{REF} = 0 \text{ V}$	30	50	80	mA
OUTPUT STAGE					
I_{SINK} continuous			50		mA
I_{PEAK}			100		mA
V_{OL}	$I_O = 50 \text{ mA}$		1	1.4	V
Leakage current	$V_{OUT} = 35 \text{ V}$			25	μA

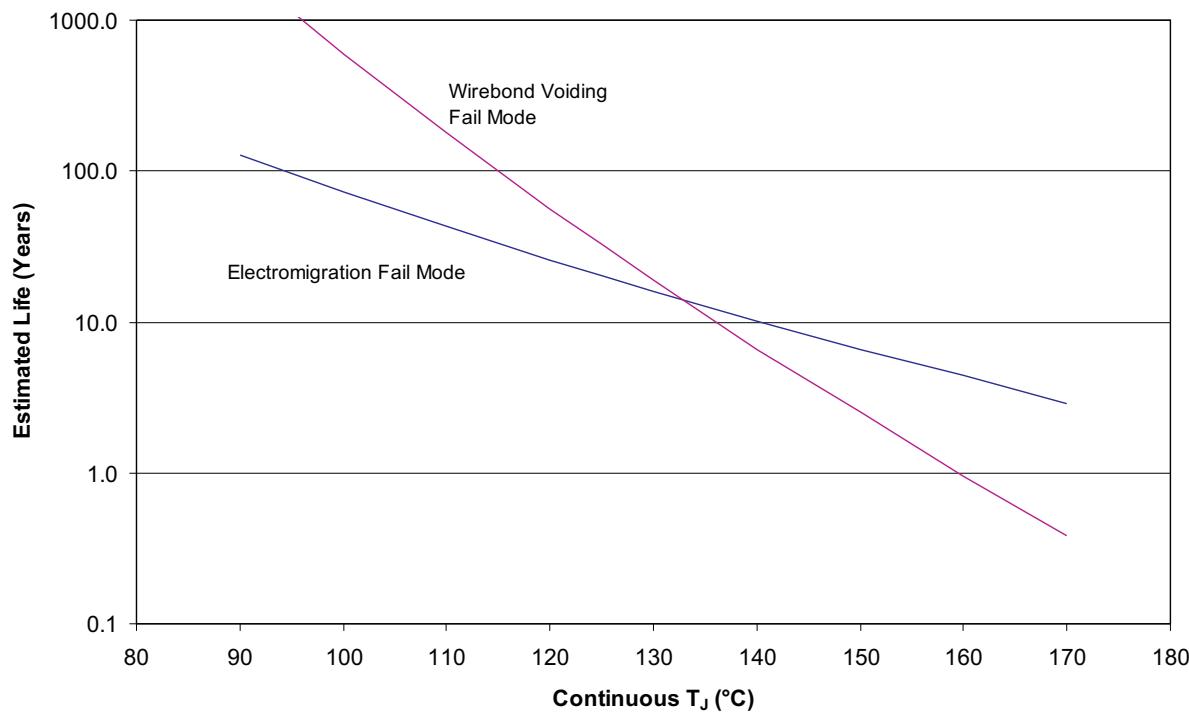
(3) Thermistor initial accuracy is measured and trimmed with respect to V_{AO} ; $V_{AO} = V_{A-}$.

ELECTRICAL CHARACTERISTICS (continued)

$T_A = -55^\circ\text{C}$ to 125°C ; $C_T = 430 \text{ pF}$, $R_{SET} = 11.5 \text{ k}\Omega$, $R_{10} = 10 \text{ k}\Omega$, $R_{THM} = 10 \text{ k}\Omega$, $V_{CC} = 15 \text{ V}$, Output no load, $R_{STAT0} = R_{STAT1} = 10 \text{ k}\Omega$, CHGENB = OVCTAP = VLOGIC, $T_A = T_J$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STAT0 AND STAT1 OPEN COLLECTOR OUTPUTS					
Maximum sink current	$V_{OUT} = 8.8 \text{ V}$	5	10		mA
Saturation voltage	$I_{OUT} = 5 \text{ mA}$		0.1	0.45	V
Leakage current	$V_{OUT} = 35 \text{ V}$			25	μA
STATLV OPEN COLLECTOR OUTPUTS					
Maximum sink current	$V_{OUT} = 5 \text{ V}$	2	5		mA
Saturation voltage	$I_{OUT} = 2 \text{ mA}$		0.1	0.45	V
Leakage current	$V_{OUT} = 5 \text{ V}$			3	μA
UVLO					
Turn-on Threshold		6.8	7.8	8.8	V
Hysteresis		100	300	500	mV
I_{CC}					
I_{CC} (run)	See Figure 1	13	19		mA
I_{CC} (off)	$V_{CC} = 6.5 \text{ V}$	2			mA


Figure 1. I_{CC} vs Temperature

**Notes:**

1. See datasheet for absolute maximum and minimum recommended operating conditions.
2. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
3. Enhanced plastic product disclaimer applies.

Figure 2. UC2909-EP Operating Life Derating Chart

DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
CA-	13	The inverting input to the current error amplifier.
CAO	14	The output of the current error amplifier which is internally clamped to approximately 4 V. It is internally connected to the inverting input of the PWM comparator.
CS-, CS+	17, 16	The inverting and non-inverting inputs to the current sense amplifier. This amplifier has a fixed gain of five and a common-mode voltage range of from -250 mV to V_{CC} .
CSO	15	The output of the current sense amplifier which is internally clamped to approximately 5.7 V.
CHGENB	10	The input to a comparator that detects when battery voltage is low and places the charger in a trickle charge state. The charge enable comparator makes the output of the voltage error amplifier a high impedance while forcing a fixed 10 mA into CA- to set the trickle charge current.
GND	3	The reference point for the internal reference, all thresholds, and the return for the remainder of the device. The output sink transistor is wired directly to this pin.
OVCTAP	9	The overcharge current taper pin detects when the output current has tapered to the float threshold in the overcharge state.
OSC	19	The oscillator ramp pin which has a capacitor (C_T) to ground. The ramp oscillates between approximately 1 V to 3 V and the frequency is approximated by: $frequency = \frac{1}{1.2 \cdot C_T \cdot R_{SET}} \quad (1)$
OUT	5	The output of the PWM driver which consists of an open collector output transistor with 100-mA sink capability.
R10	20	Input used to establish a differential voltage corresponding to the temperature of the thermistor. Connect a 10-KΩ resistor to ground from this point.
RSET	18	A resistor to ground programs the oscillator charge current and the trickle control current for the oscillator ramp. The oscillator charge current is approximately: $\frac{1.75}{R_{SET}} \quad (2)$ The trickle control current ($I_{TRCK_CONTROL}$) is approximately: $\frac{0.115}{R_{SET}} \quad (3)$
RTHM	1	A 10-KΩ thermistor is connected to ground and is thermally connected to the battery. The resistance will vary exponentially over temperature and its change is used to vary the internal 2.3-V reference by -3.9 mV/°C. The recommended thermistor for this function is part number L1005-5744-103-D1, Keystone Carbon Company, St. Marys, PA.
STAT0	7	This open collector pin is the first decode bit used to decode the charge states.
STAT1	6	This open collector pin is the second decode bit used to decode the charge states.
STATLV	8	This bit is high when the charger is in the float state.
VA-	12	The inverting input to the voltage error amplifier.
VAO	11	The output of the voltage error amplifier. The upper output clamp voltage of this amplifier is 5 V.
VCC	4	The input voltage to the chip. The chip is operational between 7.5 V and 40 V and should be bypassed with a 1-µF capacitor. A typical I_{CC} vs. temperature is shown in Figure 1 .
VLOGIC	2	The precision reference voltage. It should be bypassed with a 0.1-µF capacitor.

CHARGE STATE DECODE CHART

STAT0 and STAT1 are open collector outputs. The output is approximately 0.2 V for a logic 0.

	STAT1	STAT0
Trickle charge	0	0
Bulk charge	0	1
Over charge	1	0
Float charge	1	1

APPLICATION INFORMATION

A block diagram of the UC2909 is shown on the first page, while a typical application circuit is shown in [Figure 3](#). The circuit in [Figure 3](#) requires a DC input voltage between 12 V and 40 V.

The UC2909 uses a voltage control loop with average current limiting to precisely control the charge rate of a lead-acid battery. The small increase in complexity of average current limiting is offset by the relative simplicity of the control loop design.

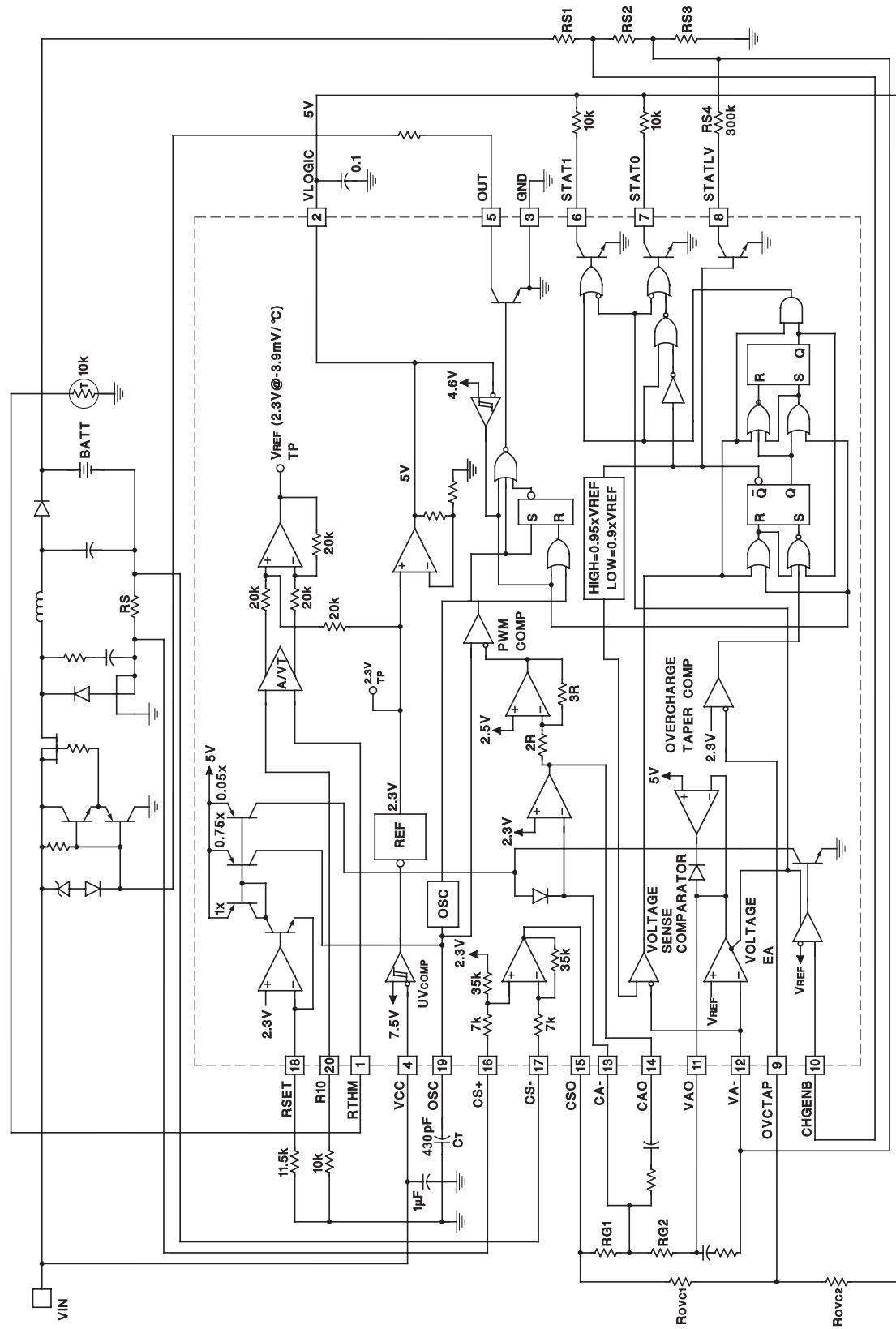


Figure 3. Typical Application Circuit

Control Loop

Current Sense Amplifier

This amplifier measures the voltage across the sense resistor RS with a fixed gain of five and an offset voltage of 2.3 V. This voltage is proportional to the battery current. The most positive voltage end of RS is connected to CSensuring the correct polarity going into the PWM comparator.

CSO = 2.3 V when there is zero battery current.

RS is chosen by dividing 350 mV by the maximum allowable load current. A smaller value for RS can be chosen to reduce power dissipation.

Maximum charge current, I_{bulk} , is set by knowing the maximum voltage error amplifier output, $V_{OH} = 5$ V, the maximum allowable drop across RS, and setting the resistors RG1 and RG2 such that:

$$\frac{RG1}{RG2} = \frac{5 \cdot V_{RS}}{VLOGIC - CA} = \frac{5 \cdot V_{RS}}{5V - 2.3V} = \frac{5 \cdot V_{RS}}{2.7V} = 1.852 \cdot I_{BULK} \cdot RS \quad (4)$$

The maximum allowable drop across RS is specified to limit the maximum swing at CSO to approximately 2 V to keep the CSO amplifier output from saturating.

No charge/load current: $V_{CSO} = 2.3$ V

Max charge/load current: $V_{max(CSO)} = 2.3$ V - 2 V = 0.3 V

Voltage Error Amplifier

The voltage error amplifier (VEA) senses the battery voltage and compares it to the 2.3-V - 3.9-mV/°C thermistor generated reference. Its output becomes the current command signal and is summed with the current sense amplifier output. A 5-V voltage error amplifier upper clamp limits maximum load current. During the trickle charge state, the voltage amplifier output is opened (high impedance output) by the charge enable comparator. A trickle bias current is summed into the CA- input which sets the maximum trickle charge current.

The VEA, $V_{OH} = 5$ V clamp saturates the voltage loop and consequently limits the charge current as stated in [Equation 4](#).

During the trickle bias state the maximum allowable charge current (ITC) is similarly determined:

$$ITC = \frac{I_{TRCK_CONTROL} \cdot RG1}{RS \cdot 5} \quad (5)$$

$I_{TRCK_CONTROL}$ is the fixed control current into CA-. $I_{TRCK_CONTROL}$ is 10 μ A when $R_{SET} = 11.5$ K Ω . See RSET pin description for equation.

Current Error Amplifier

The current error amplifier (CA) compares the output of the current sense amplifier to the output of the voltage error amplifier. The output of the CA forces a PWM duty cycle which results in the correct average battery current. With integral compensation, the CA will have a very high DC current gain, resulting in effectively no average DC current error. For stability purposes, the high frequency gain of the CA must be designed such that the magnitude of the down slope of the CA output signal is less than or equal to the magnitude of the up slope of the PWM ramp.

Charge Algorithm

Trickle Charge State

STAT0 = STAT1 = STATLV = logic 0

When CHGNB is less than VREF (2.3 V - 3.9 mV/°C), STATLV is forced low. This decreases the sense voltage divider ratio, forcing the battery to overcharge (V_{oc}).

$$V_{oc} = (V_{REF}) \cdot \frac{(RS1 + RS2 + RS3 \parallel RS4)}{(RS3 \parallel RS4)} \quad (6)$$

During the trickle charge state, the output of the voltage error amplifier is high impedance. The trickle control current is directed into the CA- pin setting the maximum trickle charge current. The trickle charge current is defined in [Equation 5](#).

Bulk Charge State

STAT1 = STATLV = logic 0, STAT0 = logic 1

As the battery charges, the UC2909 will transition from trickle to bulk charge when CHGENB becomes greater than 2.3 V. The transition equation is:

$$V_T = (V_{REF}) \cdot \frac{(RS1 + RS2 + RS3 \parallel RS4)}{(RS2 + RS3 \parallel RS4)} \quad (7)$$

STATLV is still driven low.

During the bulk charge state, the voltage error amplifier is now operational and is commanding maximum charge current (I_{BULK}) set by [Equation 4](#). The voltage loop attempts to force the battery to V_{OC} .

Overcharge State

STAT0 = STATLV = logic 0, STAT1 = logic 1

The battery voltage surpasses 95% of V_{OC} indicating the UC2909 is in its overcharge state.

During the overcharge charge state, the voltage loop becomes stable and the charge current begins to taper off. As the charge current tapers off, the voltage at CSO increases toward its null point of 2.3 V. The center connection of the two resistors between CSO and VLOGIC sets the overcurrent taper threshold (OVCTAP). Knowing the desired overcharge terminate current (I_{OCT}), the resistors R_{OVC1} and R_{OVC2} can be calculated by choosing a value of R_{OVC2} and using the following equation:

$$R_{OVC1} = (1.8518) \cdot I_{OCT} \cdot RS \cdot R_{OVC2} \quad (8)$$

Float State

STAT0 = STAT1 = STATLV = logic 1

The battery charge current tapers below its OVCTAP threshold, and forces STATLV high increasing the voltage sense divider ratio. The voltage loop now forces the battery charger to regulate at its float state voltage (V_F).

$$V_F = (V_{REF}) \cdot \frac{(RS1 + RS2 + RS3)}{RS3} \quad (9)$$

If the load drains the battery to less than 90% of V_F , the charger goes back to the bulk charge state, STATE 1.

Off Line Applications

For off line charge applications, either [Figure 4](#) or [Figure 5](#) can be used as a baseline. [Figure 4](#) has the advantage of high frequency operation resulting in a small isolation transformer. [Figure 5](#) is a simpler design, but at the expense of larger magnetics.

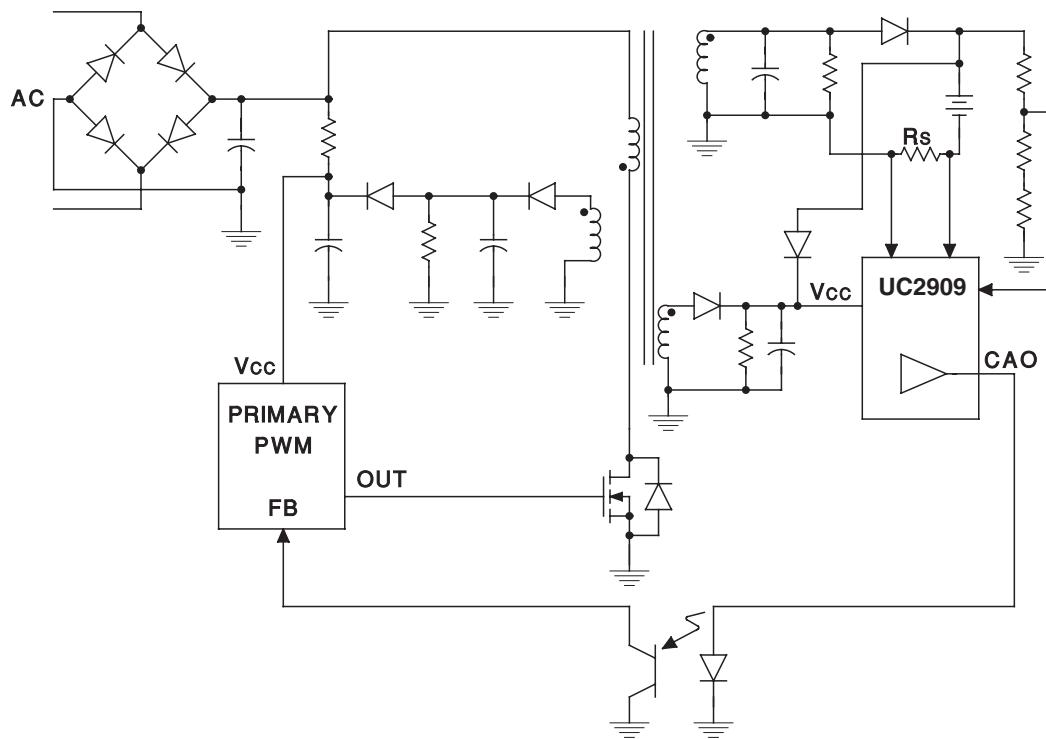


Figure 4. Off Line Charger With Primary Side PWM

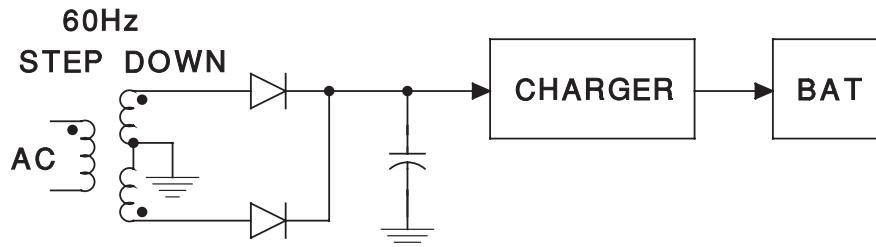


Figure 5. Isolated Off Line Charger

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC2909MDWREP	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	UC2909EP
UC2909MDWREP.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	UC2909EP
V62/10616-01XE	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	UC2909EP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

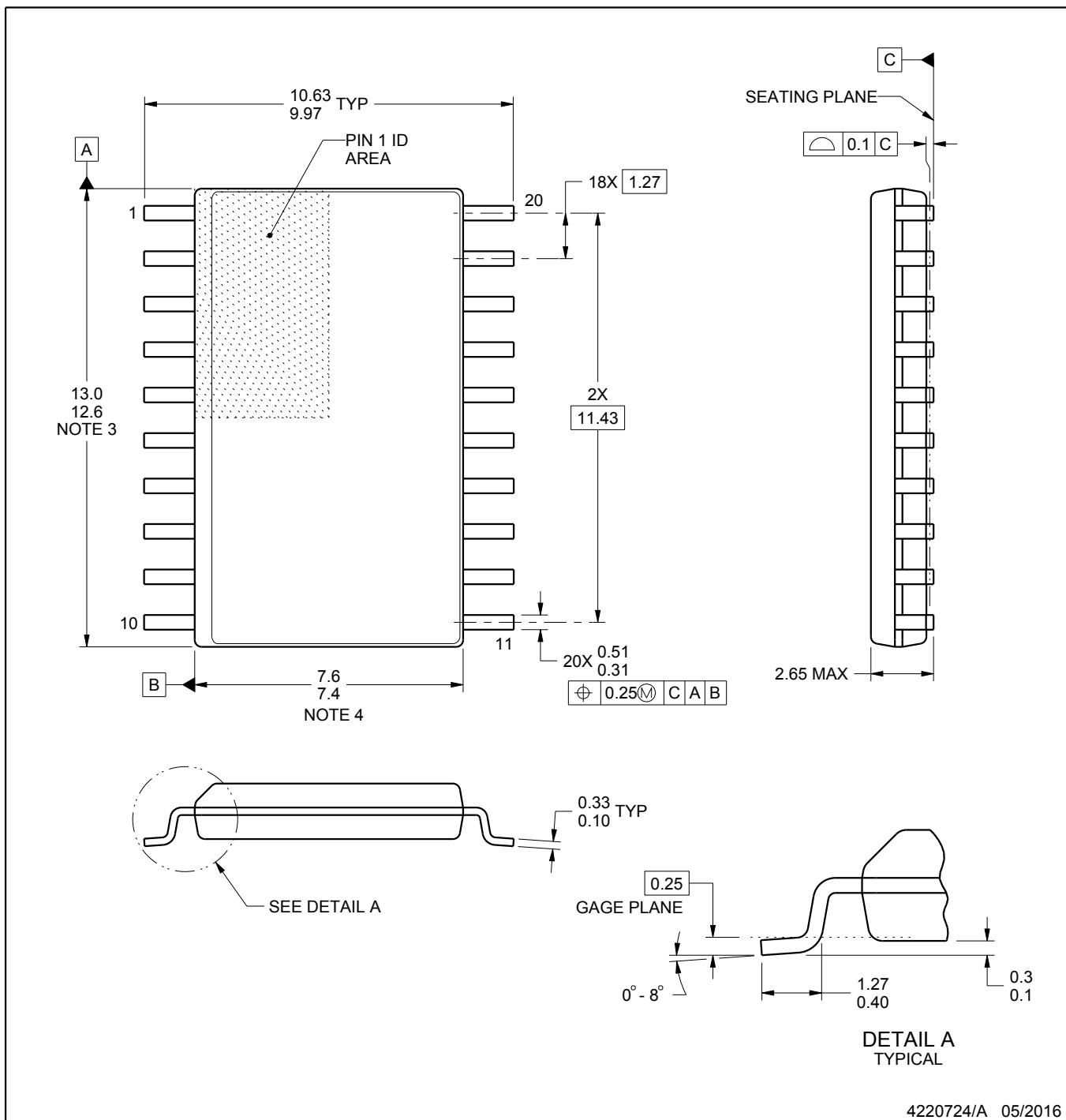
PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



NOTES:

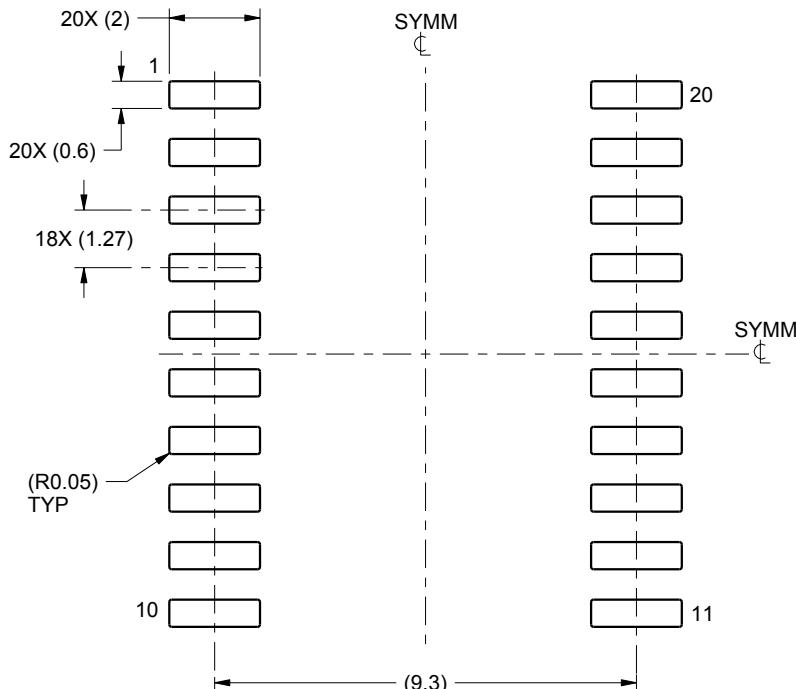
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

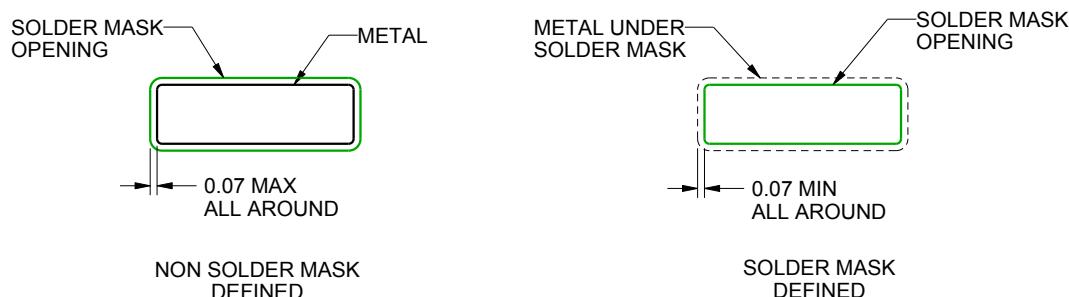
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

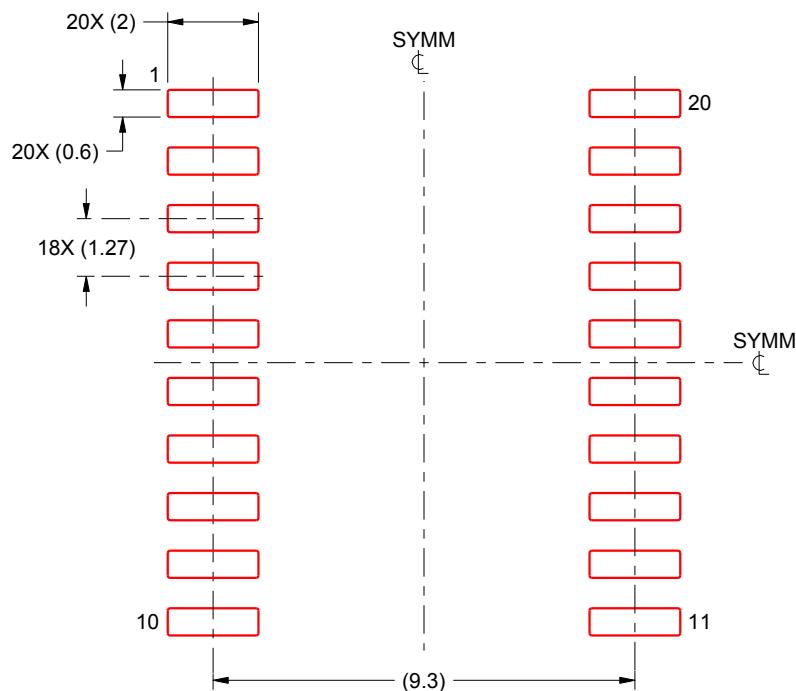
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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