

MICROPOWER SUPPLY VOLTAGE SUPERVISORS

Check for Samples: [TLC7701-EP](#), [TLC7705-EP](#), [TLC7733-EP](#)

FEATURES

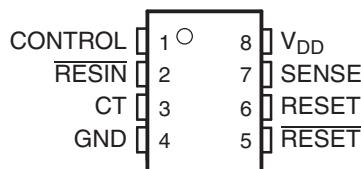
- Power-On Reset Generator
- Automatic Reset Generation After Voltage Drop
- Precision Voltage Sensor
- Temperature-Compensated Voltage Reference
- Programmable Delay Time by External Capacitor
- Supply Voltage Range . . . 2 V to 6 V
- Defined RESET Output from $V_{DD} \geq 1$ V
- Power-Down Control Support for Static RAM With Battery Backup
- Maximum Supply Current of 16 mA
- Power Saving Totem-Pole Outputs

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available in Extended (-40°C/125°C and -55°C/125°C), Temperature Ranges⁽¹⁾
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

(1) Additional temperature ranges available - contact factory

D OR PW PACKAGE
(TOP VIEW)



DESCRIPTION

The TLC77xx family of micropower supply voltage supervisors provide reset control, primarily in microcomputer and microprocessor systems.

During power-on, RESET is asserted when V_{DD} reaches 1 V. After minimum $V_{DD} (\geq 2$ V) is established, the circuit monitors SENSE voltage and keeps the reset outputs active as long as SENSE voltage ($V_{I(SENSE)}$) remains below the threshold voltage. An internal timer delays return of the output to the inactive state to ensure proper system reset. The delay time (t_d) is determined by an external capacitor:

$$t_d = 2.1 \times 10^4 \times C_T \quad (1)$$

Where

C_T is in farads

t_d is in seconds

Except for the TLC7701, which can be customized with two external resistors, each supervisor has a fixed sense threshold voltage set by an internal voltage divider. When SENSE voltage drops below the threshold voltage, the outputs become active and stay in that state until SENSE voltage returns above threshold voltage and the delay time (t_d) has expired.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

In addition to the power-on reset and undervoltage-supervisor function, the TLC77xx adds power-down control support for static RAM. When CONTROL is tied to GND, RESET will act as active high. The voltage monitor contains additional logic intended for control of static memories with battery backup during power failure. By driving the chip select (\overline{CS}) of the memory circuit with the RESET output of the TLC77xx and with the CONTROL driven by the memory bank select signal (CSH1) of the microprocessor (see [Figure 11](#)), the memory circuit is automatically disabled during a power loss. (In this application the TLC77xx power has to be supplied by the battery.)

ORDERING INFORMATION

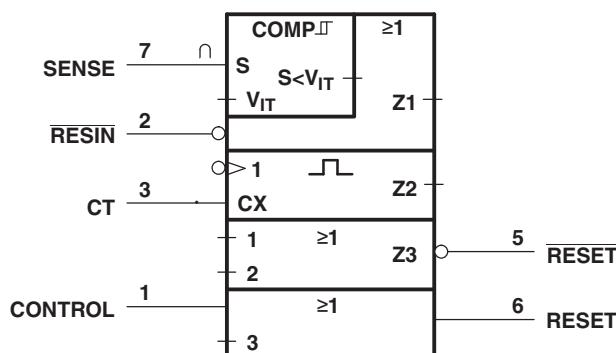
T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
-40°C to 125°C	TSSOP - PW	Tape and reel	TLC7701QPWREP	7701QE	V62/04604 - 01XE
			TLC7705QPWREP	7705QE	V62/04604 - 02XE
			TLC7733QPWREP	7733QE	V62/04604 - 03XE
-55°C to 125°C	TSSOP - PW	Tape and reel	TLC7701MPWREP	7701ME	V62/04604 - 04XE
			TLC7733MPWREP	7733ME	V62/04604 - 06XE
	SOIC - D	Tape and reel	TLC7701MDREP	7701ME	V62/04604 - 04YE

(1) The PW package is only available left-end taped and reeled (indicated by the R suffix on the device type; e.g., TLC7701QPWREP).

Table 1. FUNCTION TABLE

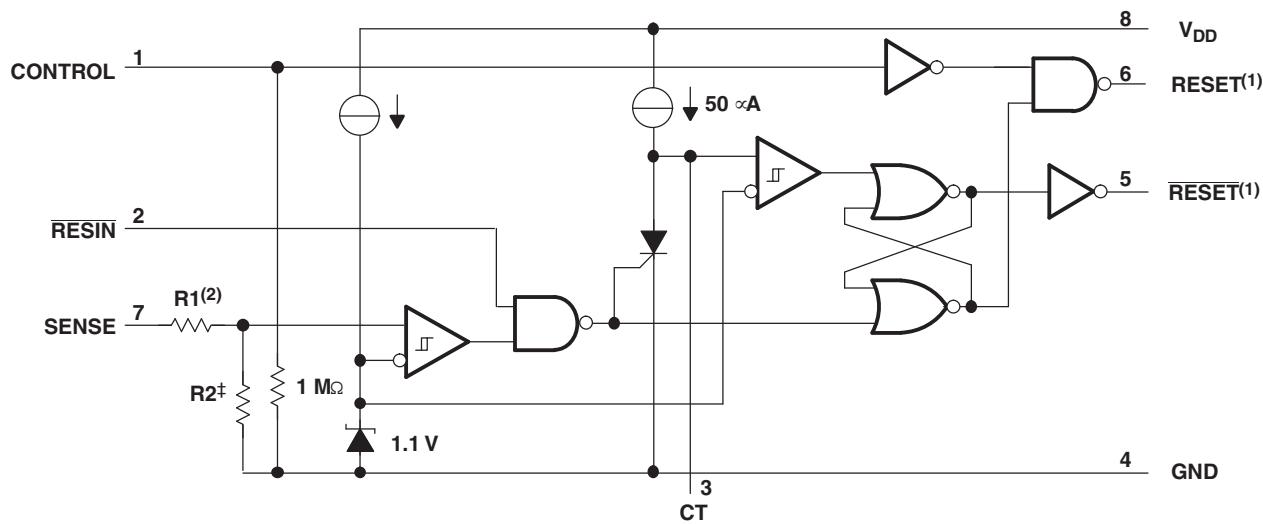
CONTROL	RESIN	$V_{I(SENSE)} > V_{IT+}$	RESET	$\overline{\text{RESET}}$
L	L	False	H	L
L	L	True	H	L
L	H	False	H	L
L	H	True	L ⁽¹⁾	H ⁽¹⁾
H	L	False	H	L
H	L	True	H	L
H	H	False	H	L
H	H	True	H	H ⁽¹⁾

(1) RESET and $\overline{\text{RESET}}$ states shown are valid for $t > t_d$.



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

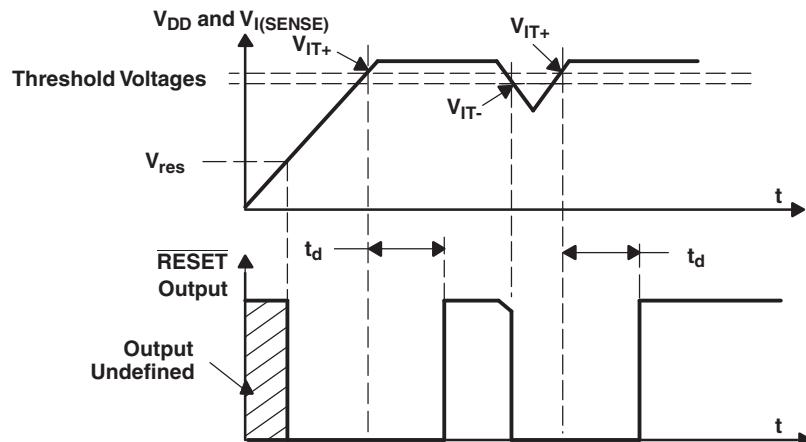
Figure 1. Logic Symbol

FUNCTIONAL BLOCK DIAGRAM


(1) Outputs are totem-pole configuration. External pullup or pulldown resistors are not required.

(2) Nominal values:

	R1 (Typ)	R2 (Typ)
TLC7701	0	∞
TLC7705	910 k Ω	290 k Ω
TLC7733	750 k Ω	450 k Ω

TIMING DIAGRAM


ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		VALUE	UNIT
V_{DD}	Supply voltage ⁽²⁾	7	V
	Input voltage range, CONTROL, RESIN, SENSE ⁽²⁾	-0.3 to 7	V
I_{OL}	Maximum low output current	10	mA
I_{OH}	Maximum high output current	10	mA
I_{IK}	Input clamp current, ($V_I < 0$ or $V_I > V_{DD}$)	± 10	mA
I_{OK}	Output clamp current, ($V_O < 0$ or $V_O > V_{DD}$)	± 10	mA
T_A	Operating free-air temperature range	TL77xxQ TL77xxM	-40 to 125 -55 to 125
T_{stg}	Storage temperature range		-65 to 150

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾	TLC77xx-EP	TLC77xx-EP	UNITS
	D	PW	
	8 PINS	8 PINS	
θ_{JA}	97.1	168	
θ_{JC}	39.4	38.9	
θ_{JB}	-	96.6	°C/W
Ψ_{JT}	-	1.5	
Ψ_{JB}	-	94.7	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	2	6		V
V_I	Input voltage	0		V_{DD}	V
V_{IH}	High-level input voltage at RESIN and CONTROL ⁽²⁾	0.7 $\times V_{DD}$			V
V_{IL}	Low-level input voltage at RESIN and CONTROL		0.2 $\times V_{DD}$		V
I_{OH}	High-level output current, $V_{DD} \geq 2.7$ V			-2	mA
I_{OL}	Low-level output current, $V_{DD} \geq 2.7$ V			2	mA
$\Delta t/\Delta V$	Input transition rise and fall rate at RESIN and CONTROL			100	ns/V
T_A	Operating free-air temperature range	Q temperature range	-40	125	°C
		M temperature range	-55	125	

(1) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

(2) To ensure a low supply current, V_{IL} should be kept < 0.3 V and $V_{IH} > -0.3$ V.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions⁽¹⁾ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = -40°C to 125°C			T _A = -55°C to 125°C			UNIT
			MIN	TYP ⁽²⁾	MAX	MIN	TYP ⁽²⁾	MAX	
V _{OH}	High-level output voltage	I _{OH} = - 20 µA	V _{DD} = 2 V	1.8		1.8			V
			V _{DD} = 2.7 V	2.5		2.5			
			V _{DD} = 4.5 V	4.3		4.3			
		I _{OH} = - 20 mA	V _{DD} = 4.5 V	3.7		3.7			
V _{OL}	Low-level output voltage	I _{OH} = - 20 µA	V _{DD} = 2 V		0.2		0.2		V
			V _{DD} = 2.7 V		0.2		0.2		
			V _{DD} = 4.5 V		0.2		0.2		
		I _{OH} = - 20 mA	V _{DD} = 4.5 V		0.5		0.5		
V _{IT-}	Negative-going input threshold voltage, SENSE ⁽³⁾	TLC7701	V _{DD} = 2 V to 6 V	1.04	1.1	1.16			V
		TLC7705		4.43	4.5	4.63			
		TLC7733		2.855	2.93	3.03	2.8	2.93	
V _{hys}	Hysteresis voltage, SENSE	TLC7701	V _{DD} = 2 V to 6 V	30					mV
		TLC7705		70					
		TLC7733		70		70			
V _{res}	Power-up reset voltage ⁽⁴⁾	I _{OL} = 20 µA			1			1	V
I _I	Input current	RESIN	V _I = 0 V to V _{DD}		2		2		µA
		CONTROL	V _I = V _{DD}	7	15	7	15		
		SENSE	V _I = 5 V		5	10	5	10	
		SENSE, TLC7701 only	V _I = 5 V		2				
I _{DD}	Supply current	RESIN = V _{DD} , SENSE = V _{DD} ≥ V _{ITmax} + 0.2 V CONTROL = 0 V, Outputs open		9	16	9	18	µA	
I _{DD(d)}	Supply current during t _d	V _{DD} = 5 V, V _{CT} = 0 , RESIN = V _{DD} , SENSE = V _{DD} CONTROL = 0 V, Outputs open		120	150	120	150	µA	
C _I	Input capacitance, SENSE	V _I = 0 V to V _{DD}		50		50		pF	

(1) All characteristics are measured with C_T = 0.1 µF.

(2) Typical values apply at T_A = 25°C.

(3) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be connected near the supply terminals.

(4) The lowest supply voltage at which RESET becomes active. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology. Rise time of VDD ≥ 15 ms/V.

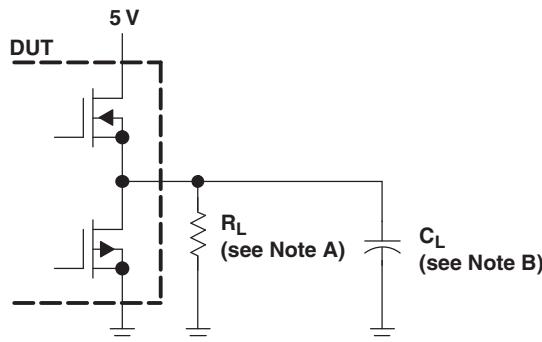
SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MEASURED		TEST CONDITIONS	TA = -40°C to 125°C			TA = -55°C to 125°C			UNIT
		FROM (INPUT)	TO (OUTPUT)		MIN	TYP	MAX	MIN	TYP	MAX	
t _d	Delay time			RESIN = 0.7 × V _{DD} , CONTROL = 0.2 × V _{DD,CT} = 100 nF, T _A = Full range, See timing diagram	1.1	2.1	4.2		2.1		ms
t _{PLH}	Propagation delay time, low-to-high level output	SENSE	RESET	V _{IH} = V _{IT+max} + 0.2 V, V _{IL} = V _{IT-min} - 0.2 V, RESIN = 0.7 × V _{DD,SENSE} = 0.2 × V _{DD} , C _T = NC ⁽¹⁾		20			20		μs
t _{PLH}	Propagation delay time, high-to-low level output					5			5		
t _{PLH}	Propagation delay time, low-to-high level output					5			5		
t _{PLH}	Propagation delay time, high-to-low level output					20			20		
t _{PLH}	Propagation delay time, low-to-high level output	RESIN	RESET	V _{IH} = 0.7 × V _{DD} , V _{IL} = 0.2 × V _{DD,SENSE} = V _{IT+max} + 0.2 V, CONTROL = 0.2 × V _{DD} , C _T = NC ⁽¹⁾		20			20		μs
t _{PLH}	Propagation delay time, high-to-low level output					60			60		ns
t _{PLH}	Propagation delay time, low-to-high level output					65			65		
t _{PLH}	Propagation delay time, high-to-low level output					20			20		μs
t _{PLH}	Propagation delay time, low-to-high level output	CONTROL	RESET	V _{IH} = 0.7 × V _{DD} , V _{IL} = 0.2 × V _{DD,SENSE} = V _{IT+max} + 0.2 V, RESIN = 0.7 × V _{DD} , C _T = NC ⁽¹⁾		58			58		ns
t _{PLH}	Propagation delay time, high-to-low level output					58			58		ns
	Low-level minimum pulse duration to switch RESET and RESET	SENSE		V _{IH} = V _{IT+max} + 0.2 V, V _{IL} = V _{IT-min} - 0.2 V		3		4			μs
				V _{IL} = 0.2 × V _{DD} , V _{IH} = 0.7 × V _{DD}		1		1			
t _r	Rise time		RESET and RESET	10% to 90%		8		8			ns/V
t _f	Fall time			90% to 10%		4		4			

(1) NC = No capacitor, and includes up to 100-pF probe and jig capacitance.

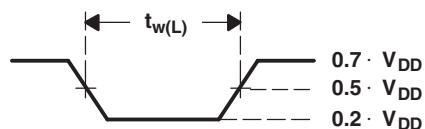
PARAMETER MEASUREMENT INFORMATION



- A. For switching characteristics, $R_L = 2\text{ k}\Omega$
- B. $C_L = 50\text{ pF}$ includes jig and probe capacitance

Figure 2. RESET AND $\overline{\text{RESET}}$ Output Configurations

I, Q, and Y suffixed devices



M suffixed devices

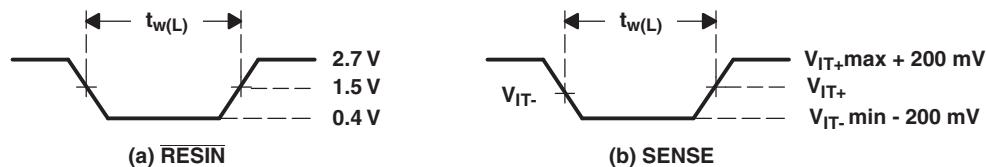


Figure 3. Input Pulse Definition Waveforms

TYPICAL CHARACTERISTICS

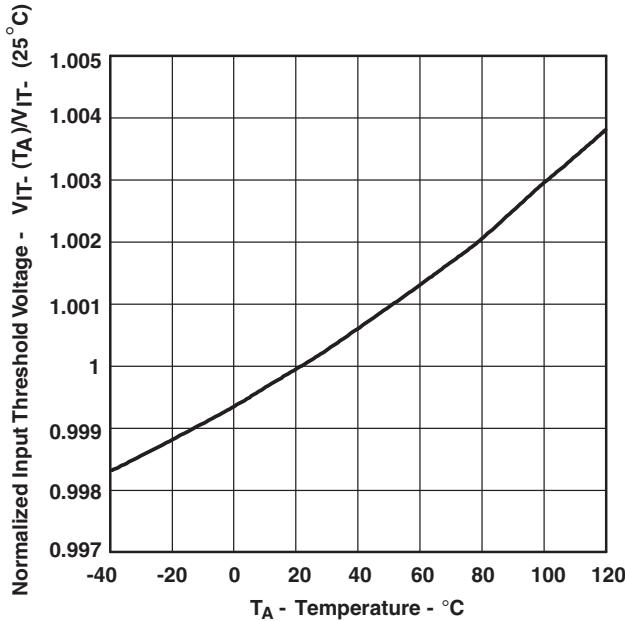
NORMALIZED INPUT THRESHOLD VOLTAGE
vs
TEMPERATURE

Figure 4.

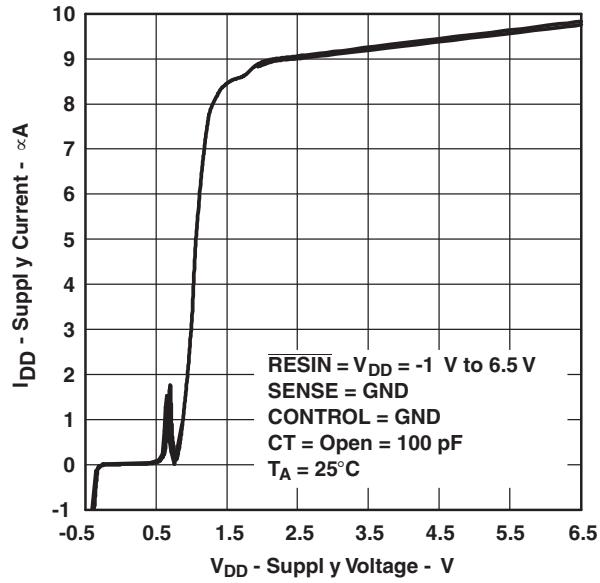
SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 5.

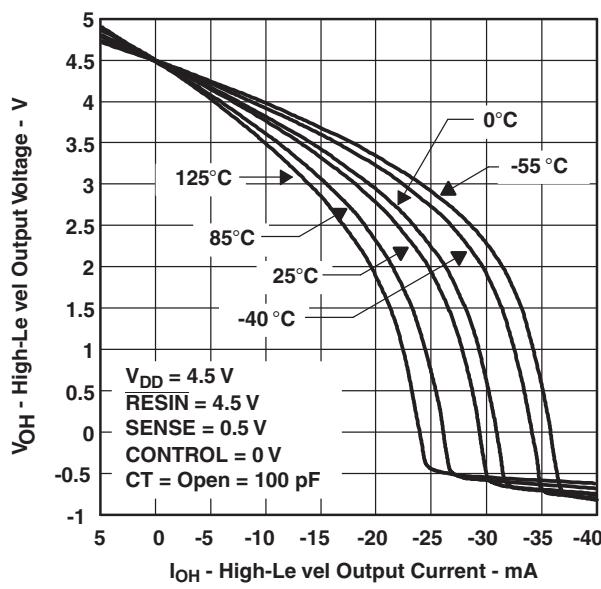
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 6.

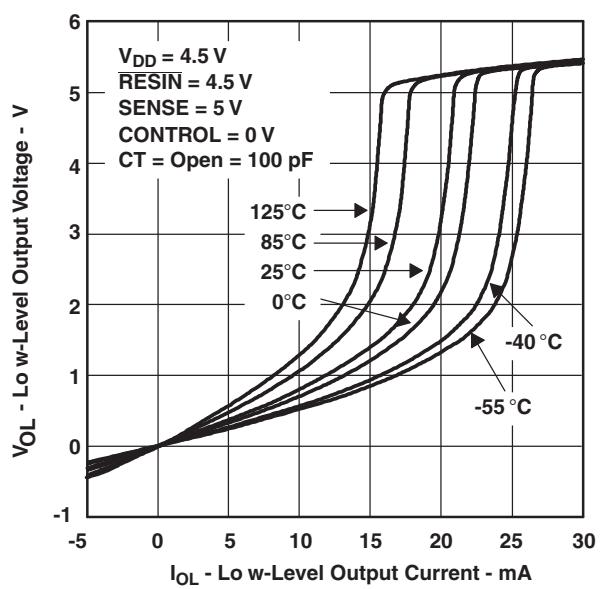
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 7.

TYPICAL CHARACTERISTICS (continued)

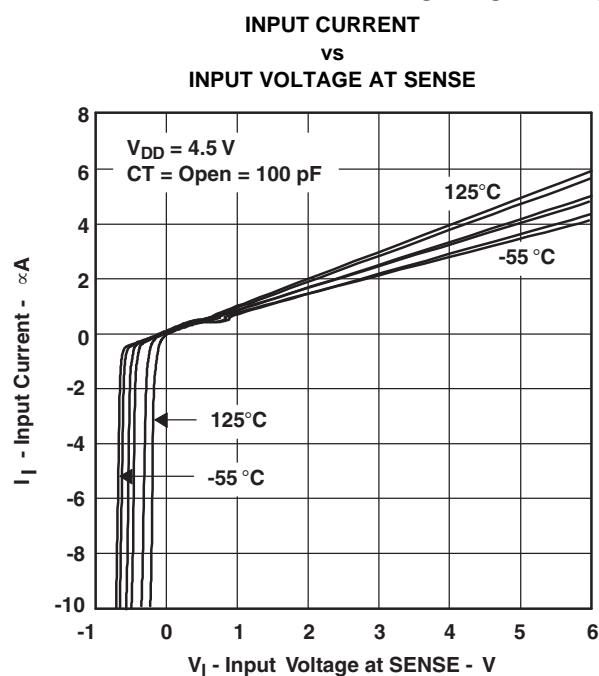


Figure 8.

**MINIMUM PULSE DURATION AT SENSE
vs
SENSE THRESHOLD OVERDRIVE**

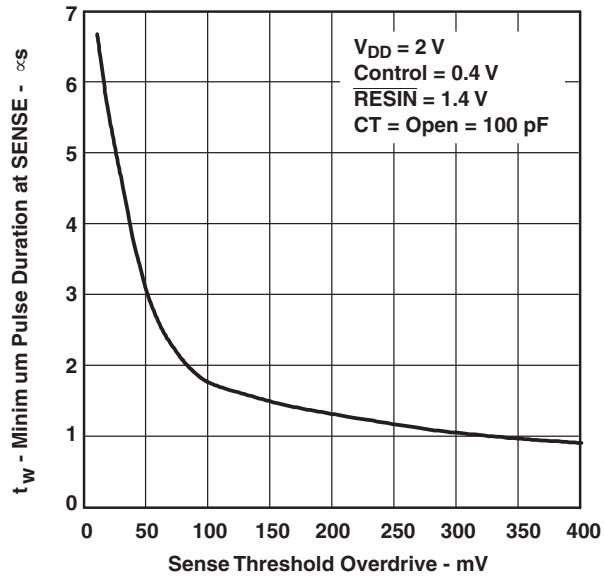


Figure 9.

APPLICATION INFORMATION

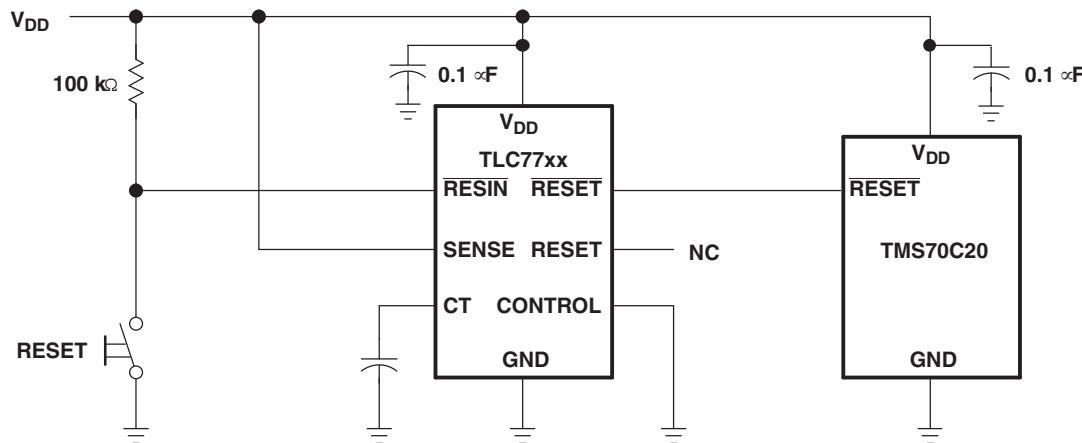


Figure 10. Reset Controller in a Microcomputer System

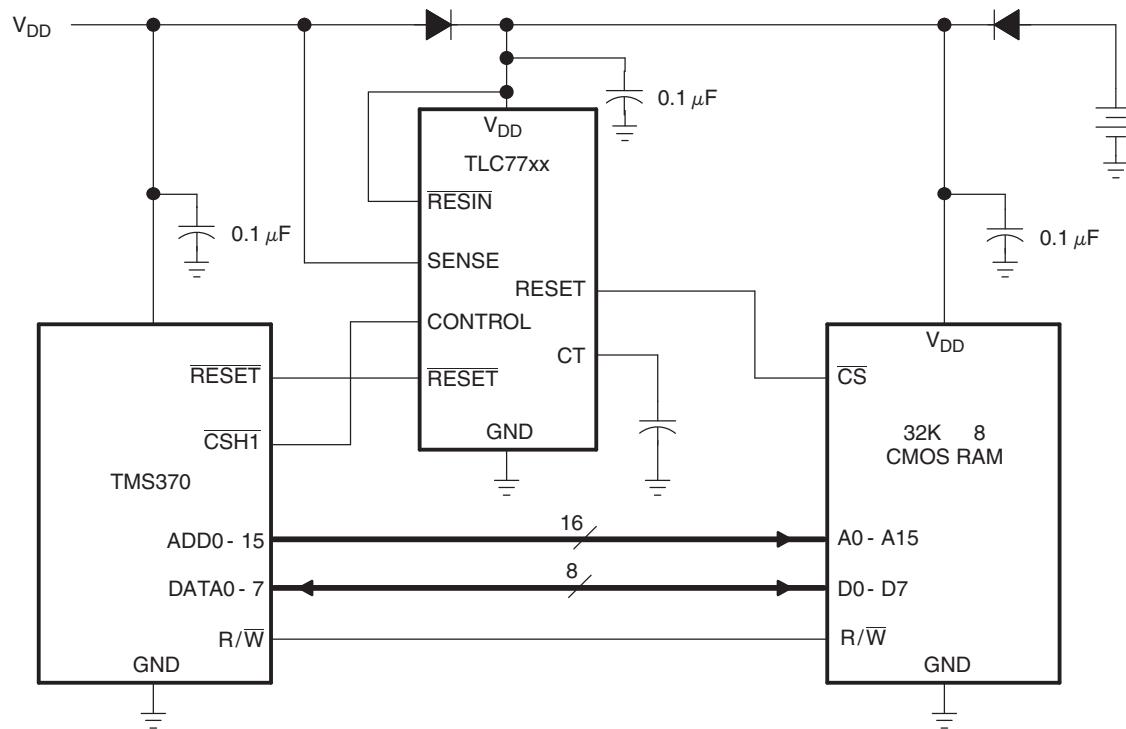


Figure 11. Data Retention During Power Down Using Static CMOS RAMs

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC7701MDREP	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME
TLC7701MDREP.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME
TLC7701MPWREP	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME
TLC7701MPWREP.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME
TLC7701QPWREP	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7701QE
TLC7701QPWREP.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7701QE
TLC7705QPWREP	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705QE
TLC7705QPWREP.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705QE
TLC7733MPWREP	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7733ME
TLC7733MPWREP.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7733ME
TLC7733QPWREP	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7733QE
TLC7733QPWREP.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7733QE
V62/04604-01XE	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7701QE
V62/04604-02XE	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7705QE
V62/04604-03XE	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7733QE
V62/04604-04YE	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7701ME
V62/04604-06XE	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7733ME

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

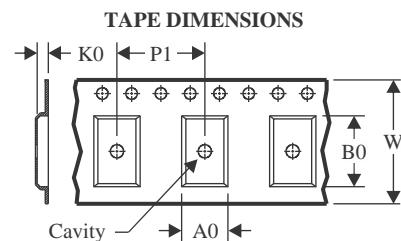
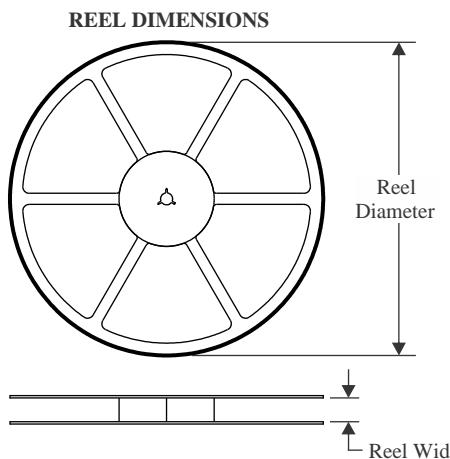
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC77-EP :

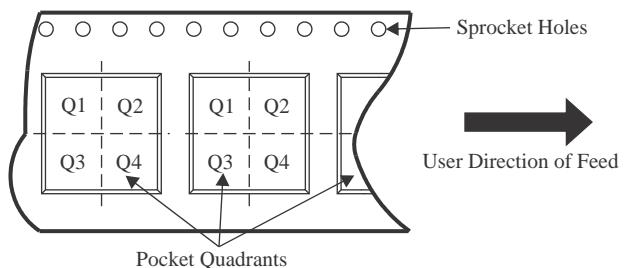
- Catalog : [TLC77](#)
- Automotive : [TLC77-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC7701MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC7701MPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7701QPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7705QPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7733MPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC7733QPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

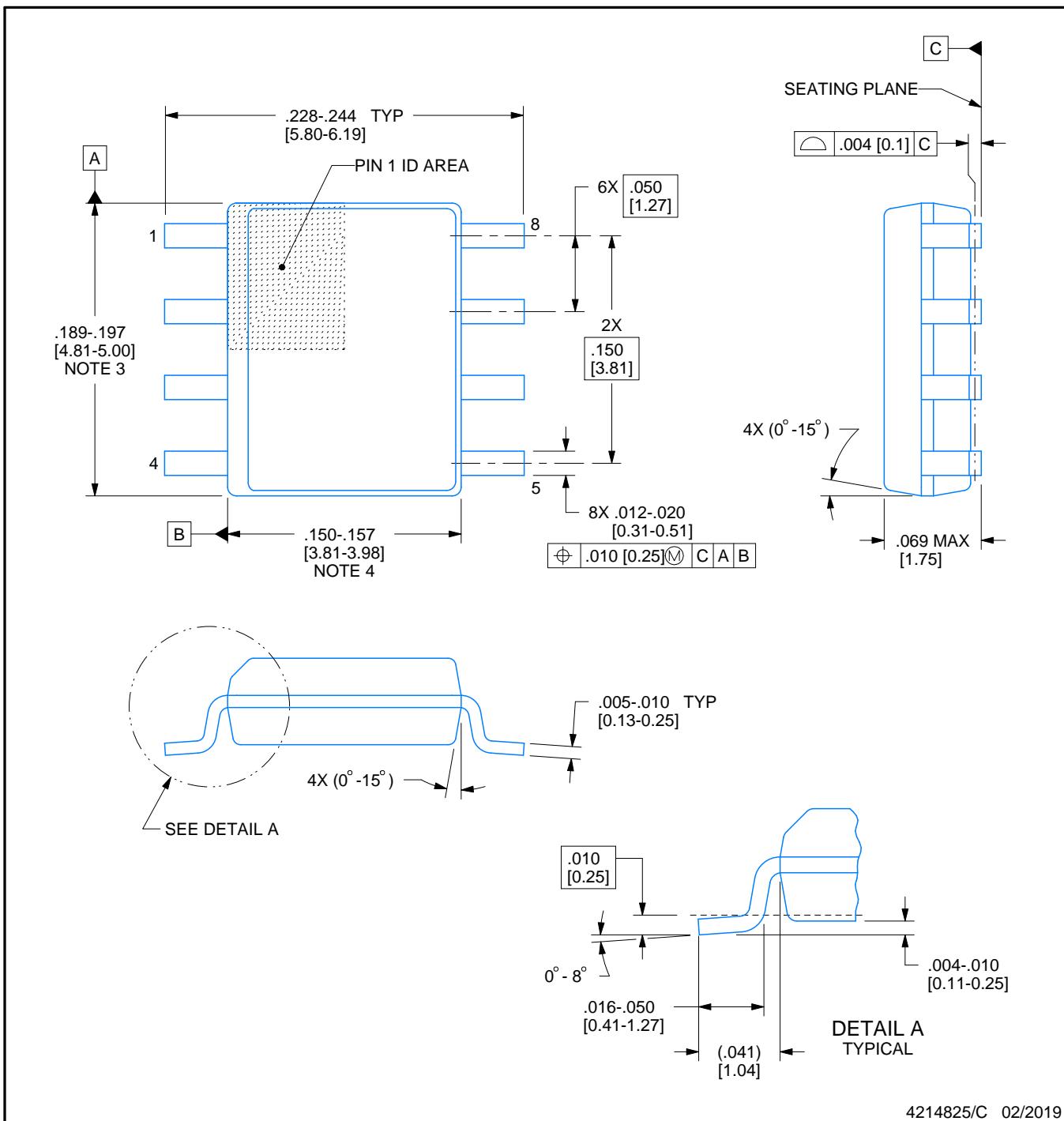
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC7701MDREP	SOIC	D	8	2500	340.5	338.1	20.6
TLC7701MPWREP	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC7701QPWREP	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC7705QPWREP	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC7733MPWREP	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC7733QPWREP	TSSOP	PW	8	2000	353.0	353.0	32.0



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

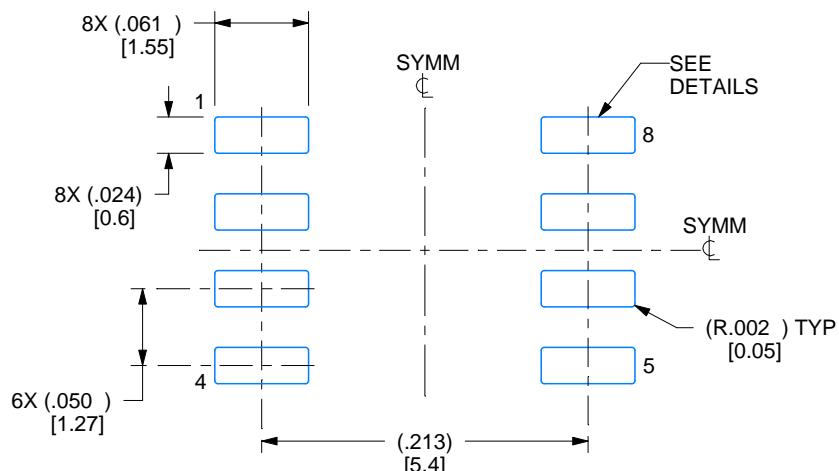
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

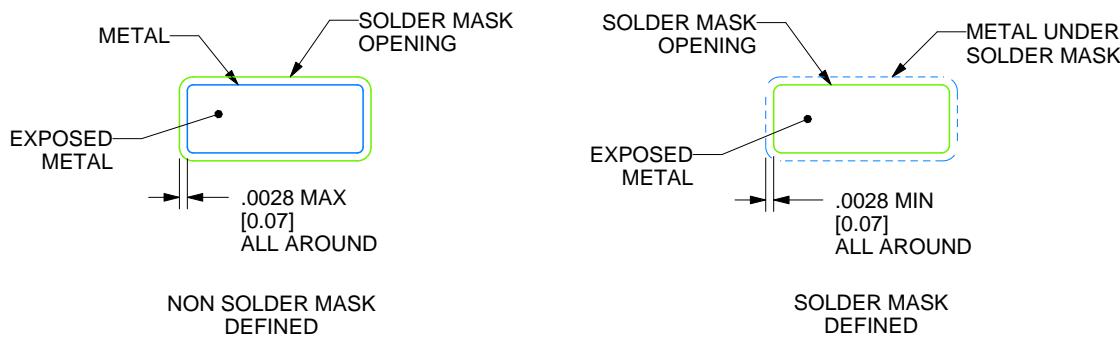
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

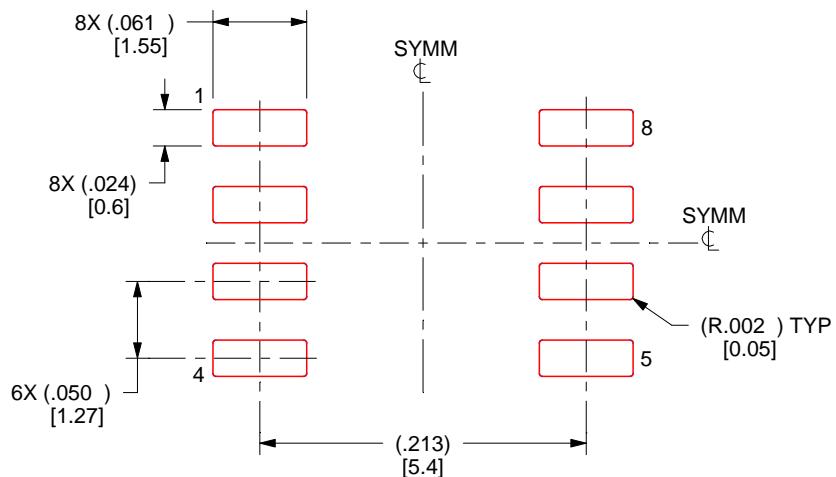
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

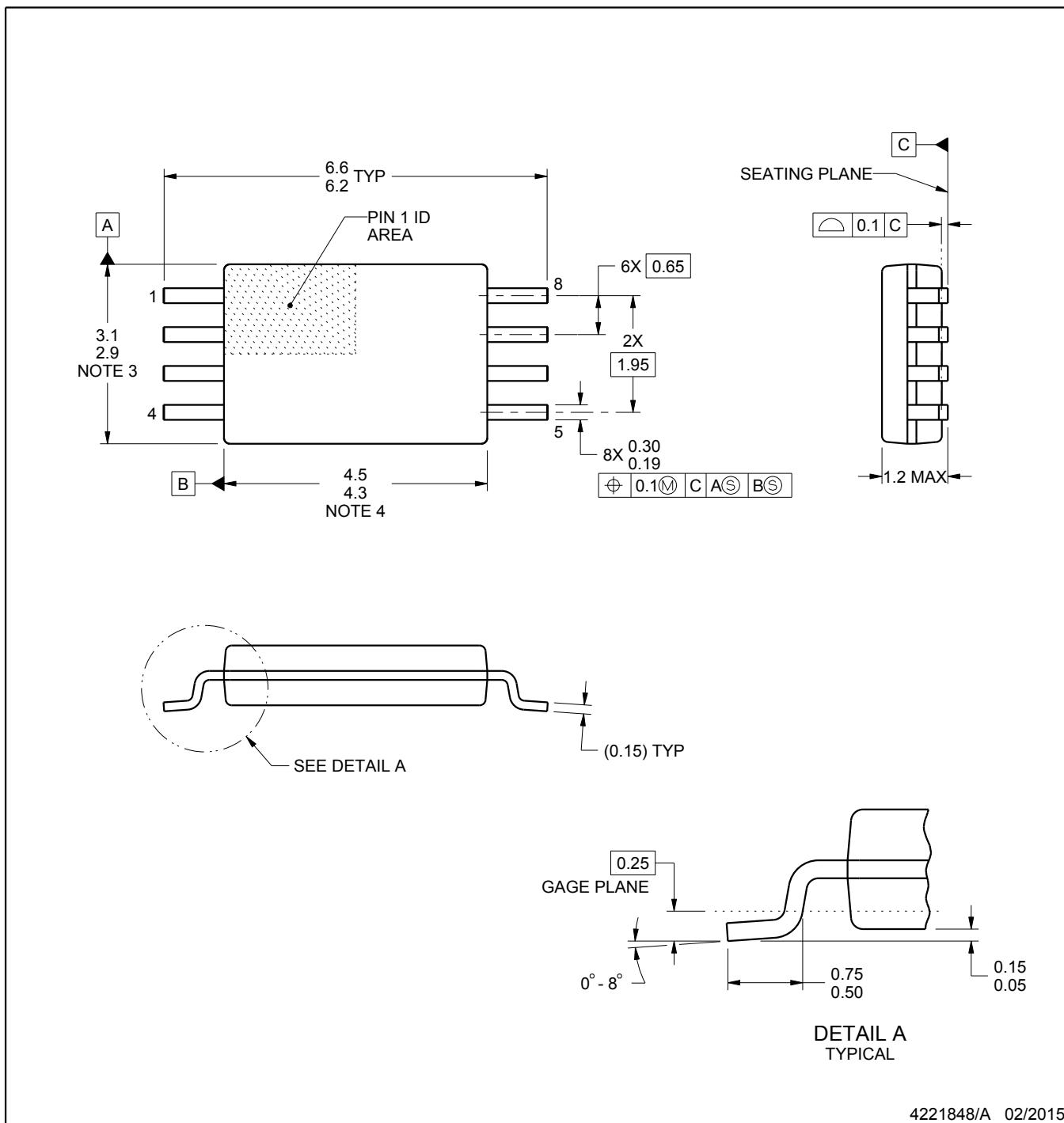
PACKAGE OUTLINE

PW0008A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

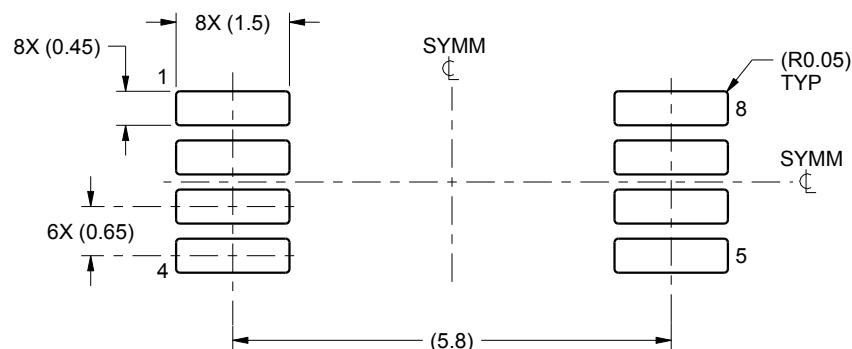
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

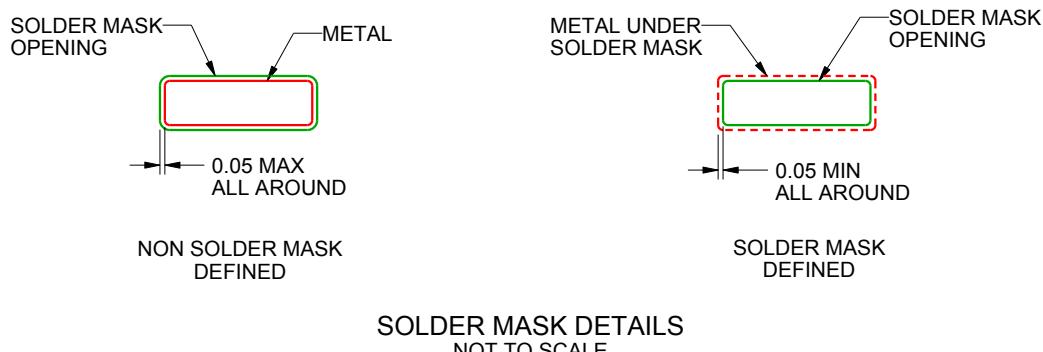
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



4221848/A 02/2015

NOTES: (continued)

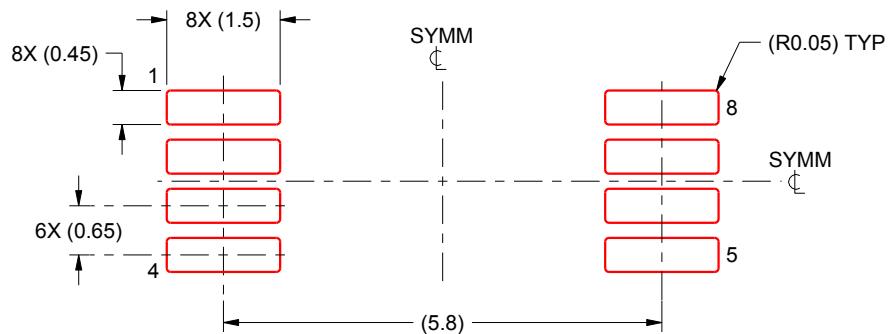
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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