GS1679 Cable Driver with HD/SD Capability

The GS1679 is a high-speed BiCMOS integrated circuit designed to drive one to four 75Ω coaxial cables. The GS1679 can drive data rates up to 1.485Gb/s, and provides two selectable slew rates in order to achieve compliance to SMPTE 292M, SMPTE 259M and SMPTE 344M.

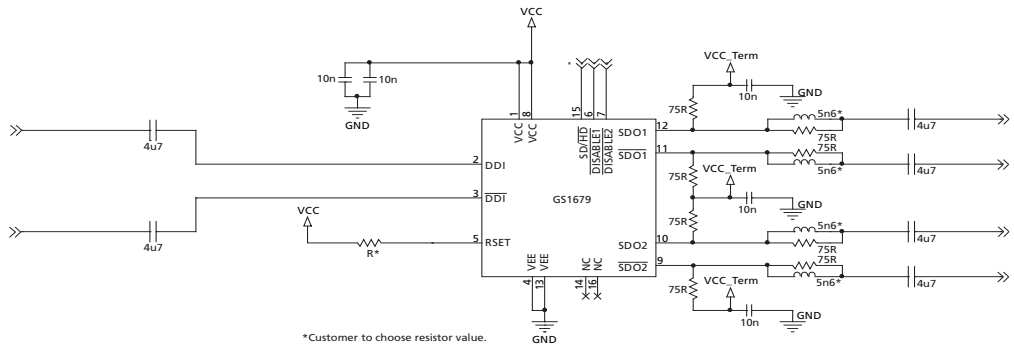
The GS1679 accepts industry-standard differential input levels, including LVPECL and CML. The $\overline{\text{DISABLE1}}$ and $\overline{\text{DISABLE2}}$ pins power-down the first and second output drivers respectively, leaving the serial data output in a high-impedance state. The GS1679 features an adjustable output swing using an external bias resistor. The single-ended output swing is adjustable from 600mVpp to 1200mVpp. The GS1679 can be powered from either a 3.3V or a 2.5V supply. Power consumption is typically 110mW using a 2.5V power supply.

The GS1679 is forward footprint-compatible with Gennum's 3G GS2989, allowing for an easier migration of HD designs to 3G.

Key Features

- SMPTE 292M, SMPTE 259M and SMPTE 344M compliant
- Supports data rates from 270Mb/s to 1.485Gb/s
- Supports DVB-ASI at 270Mb/s
- Dual differential coaxial-cable-driving outputs
  - selectable slew rates
  - adjustable output swing from 600mVpp to 1200mVpp
  - DISABLE control
- Wide common-mode range input buffer
  - 100mV sensitivity
  - Supports DC-coupling to industry-standard differential logic
  - on-chip 100Ω differential data input termination
- Excellent output eye quality
- Power supply operation at 3.3V or 2.5V
- 110mW power consumption (2.5V supply)
- Operating temperature range: -40°C to +85°C
- Small footprint QFN package (4mm x 4mm)
- Pb-free and RoHS compliant
- Forward pin-compatible with Gennum's 3G GS2989

Typical Application Circuit



NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise stated.

* Typical value: varies with layout, and represents a trade-off between good eye shape and output return loss.
5n6 is the optimum value for an 800mV output swing and 3.3V operation.
4n7 is the optimum value for an 800mV output swing and 2.5V operation.
6n8 is the optimum value for an 1200mV output swing.

Contents

1. Pin Out

1.1 Pin Assignment

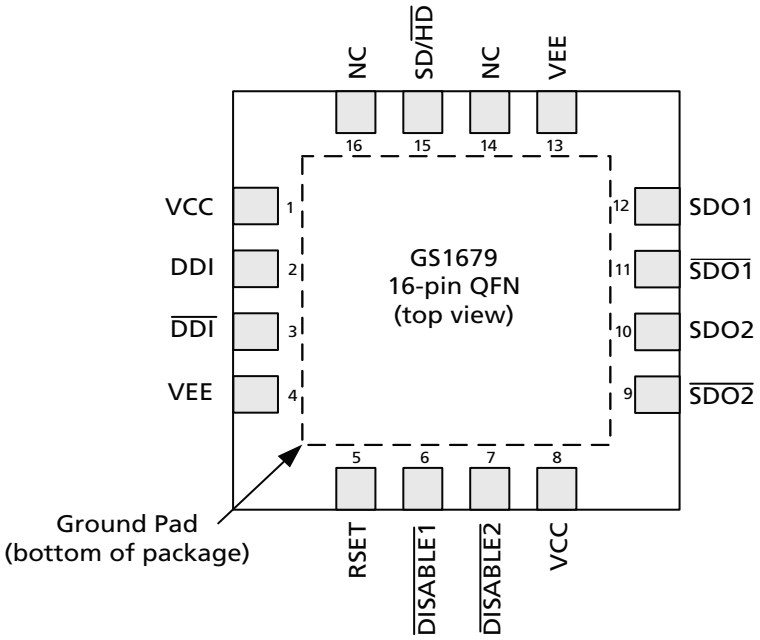


Figure 1-1: 16-Pin QFN

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
1, 8	VCC	Power	Most positive power supply connection for the input buffer and core. Connect to 3.3V or 2.5V.
2, 3	DDI, $\overline{\text{DDI}}$	Input	Serial digital differential input.
4, 13	VEE	Power	Most negative power supply connection for the input buffer and core. Connect to GND.
5	RSET	Input	External output amplitude control resistor connection.
6*	$\overline{\text{DISABLE1}}$	Input	Control signal input. When set LOW, the first serial digital output is disabled (powered-down) and the SDO1/$\overline{\text{SDO1}}$ pins are set to high-impedance. When set HIGH, the SDO1/$\overline{\text{SDO1}}$ pins will output a serial digital signal. **NOTE:** if this pin is left floating, the first serial digital output will be **enabled**.

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
7*	$\overline{\text{DISABLE2}}$	Input	Control signal input. When set LOW, the second serial digital output is disabled (powered-down) and the SDO2/$\overline{\text{SDO2}}$ pins are set to high-impedance. When set HIGH, the SDO2/$\overline{\text{SDO2}}$ pins will output a serial digital signal. **NOTE:** if this pin is left floating, the second serial digital output will be **disabled**.
9,10	$\overline{\text{SDO2}}$/ SDO2	Output	Serial digital differential output of second output buffer.
11,12	$\overline{\text{SDO1}}$/ SDO1	Output	Serial digital differential output of first output buffer.
14, 16	NC	–	No connect. Not internally bonded.
15	SD/$\overline{\text{HD}}$	Input	Control signal input. When set HIGH, the serial digital outputs will meet the SMPTE 259M rise/fall time specification. When set LOW, the serial outputs will meet the SMPTE 292M rise/fall time specification. **NOTE:** if this pin is left floating, the serial digital outputs will meet the SMPTE 259M rise/fall time specification.
–	Center Pad	Power	Connect to most negative power supply plane following the recommendations in Recommended PCB Footprint on page 13.

*NOTE: When pins 6 and 7 are driven LOW together (or similarly when pin 6 is driven LOW while pin 7 is left floating), the entire device is powered-down. In this state, bare minimum power consumption occurs.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to 3.6 V_{DC}
Input ESD Voltage	2.5kV
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	-40°C to +85°C
Solder Reflow Temperature	260°C
NOTE: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristic sections is not implied.	

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{CC} = 3.3V ±5% or 2.5V ±5%; T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	V_{CC}	3.3V Typical	3.135	3.3	3.465	V	–
		2.5V Typical	2.375	2.5	2.625	V	–
Power Consumption (2.5V)	P_D	SDO1/$\overline{SDO1}$ enabled, SDO2/$\overline{SDO2}$ disabled	–	110	130	mW	1
		SDO1/$\overline{SDO1}$ and SDO2/$\overline{SDO2}$ enabled	–	180	215	mW	1
		SDO1/$\overline{SDO1}$ and SDO2/$\overline{SDO2}$ disabled	–	3	5	mW	1
Power Consumption (3.3V)		SDO1/$\overline{SDO1}$ enabled, SDO2/$\overline{SDO2}$ disabled	–	155	183	mW	1
		SDO1/$\overline{SDO1}$ and SDO2/$\overline{SDO2}$ enabled	–	250	300	mW	1
		SDO1/$\overline{SDO1}$ and SDO2/$\overline{SDO2}$ disabled	–	4	6	mW	1
Supply Current	I_S	1 channel, VCC = 3.3V	–	47	53	mA	1
		1 channel, VCC = 2.5V	–	44	50	mA	1
		2 channels, VCC = 3.3V	–	76	87	mA	1
		2 channels, VCC = 2.5V	–	72	82	mA	1
		Power-down	–	1	1.8	mA	1
Output Voltage	V_{CMOUT}	Common mode	–	V_{CC} - V_{OUT}	–	V	–
Input Voltage	V_{CMIN}	Common mode	1.4 + $\Delta V_{DDI}/2$	–	V_{CC} - $\Delta V_{DDI}/2$	V	–
SD/$\overline{HD}$, $\overline{DISABLE}$	V_{IH}	I_{IH} <= 150µA	1.7	–	–	V	–
	V_{IL}	I_{IL} <= 150µA	–	–	0.8	V	–
OSP Drive Strength	–	–	2	–	–	mA	–

NOTES:

1. Power consumed in GS1679 only. Termination resistors draw extra current with output swing = 800mV.

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{CC} = 3.3V ±5% or 2.5V ±5%; T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input data rate	DR_{SDO}	–	.27	–	1.485	Gb/s	1
Additive jitter	–	1.485Gb/s	–	10	–	ps_{p-p}	2
	–	270Mb/s	–	30	–	ps_{p-p}	2
Rise/Fall time	t_r, t_f	SD/$\overline{HD}$=0	–	–	135	ps	3
	t_r, t_f	SD/$\overline{HD}$=1	400	–	800	ps	3
Mismatch in rise/fall time	$\triangle t_r$, $\triangle t_f$	HD mode only	–	–	35	ps	–
Duty cycle distortion	–	SD/$\overline{HD}$=0	–	–	20	ps	4, 5
	–	SD/$\overline{HD}$=1	–	–	50	ps	4, 5
Overshoot	–	SD/$\overline{HD}$=0,	–	–	10	%	4
Output Return Loss	ORL	–	17	19	–	dB	6
Output Voltage Swing	V_{OUT}	R_{SET} = 750Ω	750	800	850	mV_{p-p}	4
Input Voltage Swing	$\triangle V_{DDI}$	Differential	300	–	2000	mV_{p-pd}	–
Output Enable Delay	–	–	–	–	100	ns	–
Output Disable Delay	–	–	–	–	80	ns	–

NOTES:

1. The input coupling capacitor must be set accordingly for lower data rates.
2. Turning on input trace equalization will reduce jitter in most applications.
3. Rise/Fall time measured between 20% and 80% applies to 800mV output swing only.
4. Single-ended into a 75Ω external load.
5. Calculated as the actual positive bit-width compared to the expected positive bit-width using a 1010 pattern.
6. ORL depends on board design. The GS1679 achieves this specification on Gennum's evaluation boards.

3. Detailed Description

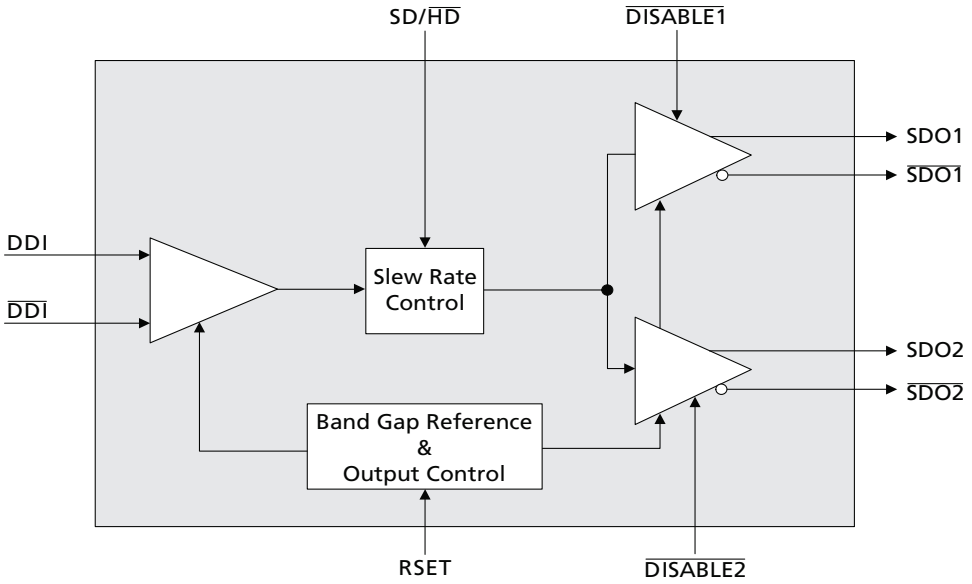


Figure 3-1: GS1679 Functional Block Diagram

3.1 Serial Data Input

The GS1679 features a differential input buffer with on-chip 100Ω differential termination.

The serial data input signal is connected to the DDI and $\overline{\text{DDI}}$ input pins of the device.

Input signals can be single-ended or differential, DC or AC-coupled.

The serial digital input buffer is capable of operation with any binary coded signal that meets the input signal level requirements, in the range of 270Mb/s to 1.485Gb/s.

The input circuit is self-biasing to allow for simple AC or DC-coupling of input signals to the device.

3.2 Serial Digital Output

The GS1679 features dual current-mode differential output drivers capable of driving up to 1200mVpp single-ended into a 1m length of 75Ω cable terminated at both ends.

The output signal amplitude or swing is user configurable using an external RSET resistor.

The SDO1/$\overline{\text{SDO1}}$ and SDO2/$\overline{\text{SDO2}}$ pins of the device provide the serial digital outputs.

3.2.1 Slew Rate Selection (Rise/Fall Time Requirement)

The GS1679 supports two user-selectable output slew rates.

Control of the slew rate is determined by the setting of the SD/$\overline{\text{HD}}$ input pin.

Table 3-1: Slew Rate Selection

SD/$\overline{HD}$	Rise/Fall Time
0	292M compliant
1	SMPTE 259M compliant
Floating	SMPTE 259M compliant

3.3 Output Disable

The GS1679 supports an output disable function for each serial digital differential output.

Control of this function is determined by the setting of the $\overline{DISABLE1}$ and $\overline{DISABLE2}$ control pins.

The serial output disables ($\overline{DISABLE1}$ and $\overline{DISABLE2}$), disable power to the current mode serial digital output drivers. When asserted LOW, the SDO/$\overline{SDO}$ output drivers are powered-down.

Table 3-2: Output Disable

$\overline{DISABLE1}$	$\overline{DISABLE2}$	SDO1/$\overline{SDO1}$	SDO2/$\overline{SDO2}$
0	0 or Floating	All Chip Power Down	
0	1	High-Impedance	Operational
1 or Floating	0 or Floating	Operational	High-Impedance
1 or Floating	1	Operational	Operational
Floating	Floating	Operational	High-Impedance

When $\overline{DISABLE1}$ and $\overline{DISABLE2}$ are driven LOW simultaneously, the entire device is powered down, and the power consumption is minimized.

3.4 Output Amplitude (RSET)

The output amplitude of the GS1679 can be adjusted by changing the value of the RSET resistor as shown in Figure 3-2. For an 800mV$_{p-p}$ output with a nominal ±7% tolerance, a value of 750Ω is required. A ±1% SMT resistor should be used.

The RSET resistor is part of the GS1679's high-speed output circuit. The resistor should be placed as close as possible to the R_{SET} pin, and be connected directly to the VCC plane (traces/wires may cause instability). In addition, the PCB capacitance should be minimized at this node by removing the PCB groundplane beneath the RSET resistor and the RSET pin.

NOTE: Care should be taken when considering layout of the RSET resistor. Please refer to Section 4.1 for more details.

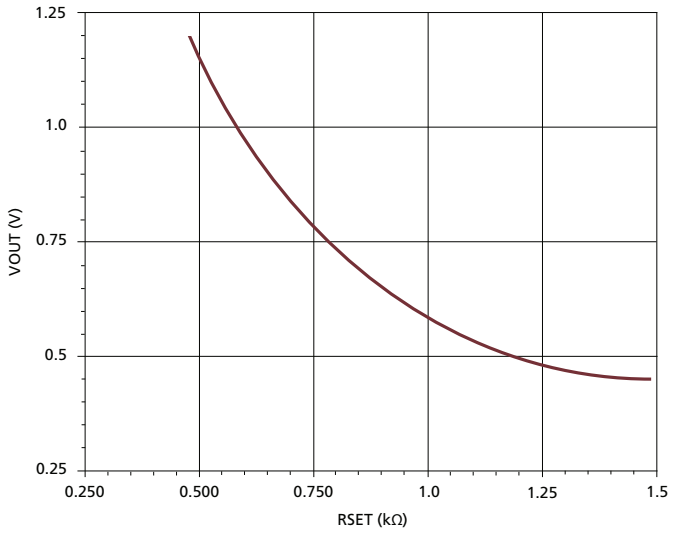


Figure 3-2: V_{OUT} vs. RSET

Table 3-3: Typical RSET Values

RSET (Ω)	Output Swing (mV)
500	1200*
750	800
1000	600

*NOTE: In order to generate output swings greater than 1040mV, VCC_TERM must be connected to a 5V supply.

For other swing values, the following formula should be used:

V_{OUT} = 600,000/Rset

Where:

V_{OUT} is the single-ended output swing in mV

Rset is the Rset resistor value in Ω

Termination resistors assumed to be 75Ω

4. Application Information

4.1 PCB Layout

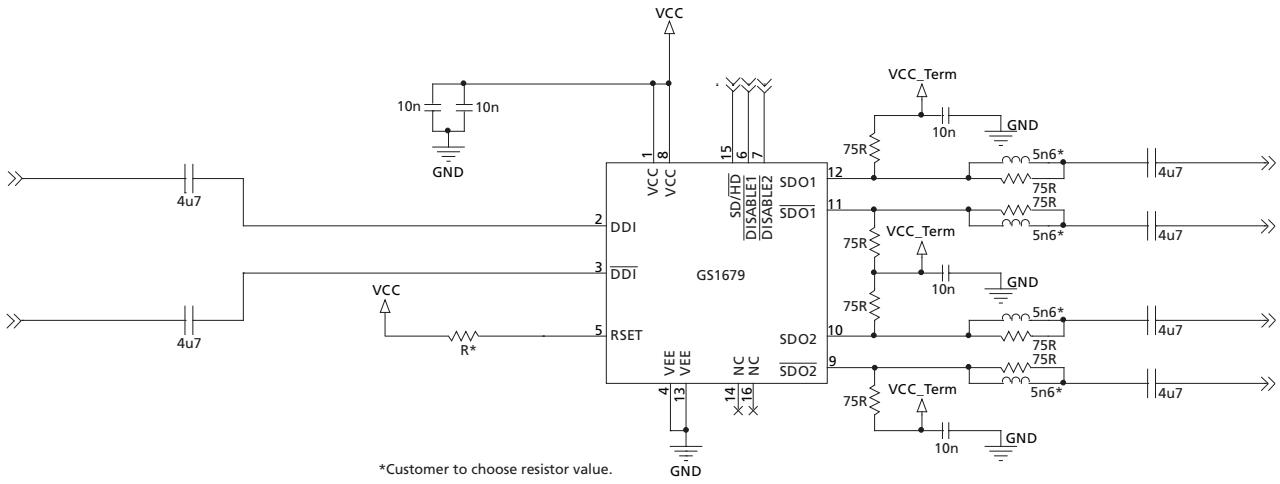
Special attention must be paid to component layout when designing serial digital interfaces for HDTV.

An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- The PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to changes in trace impedance
- The PCB ground plane is removed under the GS1679 output components to minimize parasitic capacitance (NOTE: care should be taken, as removing too much of the plane will make the system susceptible to EMI)
- The PCB ground plane is removed under the GS1679 RSET pin and resistor to minimize parasitic capacitance. The RSET resistor should be directly connected to the VCC plane
- High-speed traces are round-curved (rather than 45° or 90° angles) to minimize impedance variations due to change of PCB trace width

NOTE: For more recommendations on Trace Lengths, ORL Inductor Values and other PCB Layout Considerations, please refer to Gennum's GS2989 Design Guide (Doc ID 52070).

4.2 Typical Application Circuit



NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise stated.

* Typical value: varies with layout, and represents a trade-off between good eye shape and output return loss.
5n6 is the optimum value for an 800mV output swing and 3.3V operation.
4n7 is the optimum value for an 800mV output swing and 2.5V operation.
6n8 is the optimum value for an 1200mV output swing.

Figure 4-1: Typical Application Circuit

5. Input/Output Circuits

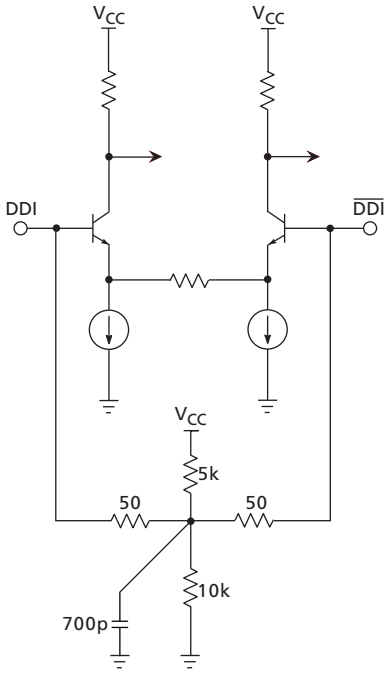


Figure 5-1: Differential Input Stage (DDI/$\overline{\text{DDI}}$)

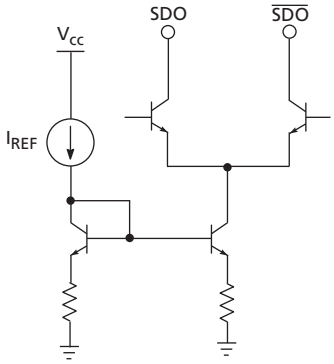


Figure 5-2: Differential Output Stage (SDO1/$\overline{\text{SDO1}}$, SDO2/$\overline{\text{SDO2}}$)

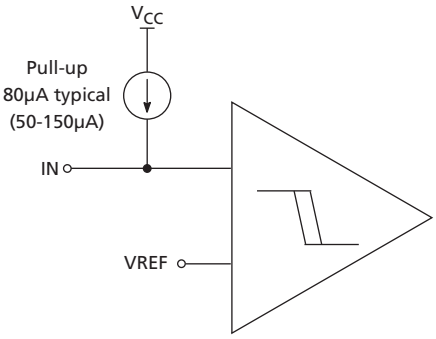


Figure 5-3: Control Input ($\overline{\text{DISABLE1}}$, SD/$\overline{\text{HD}}$)

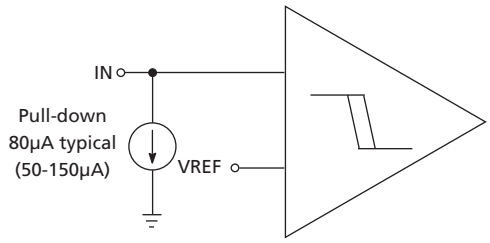
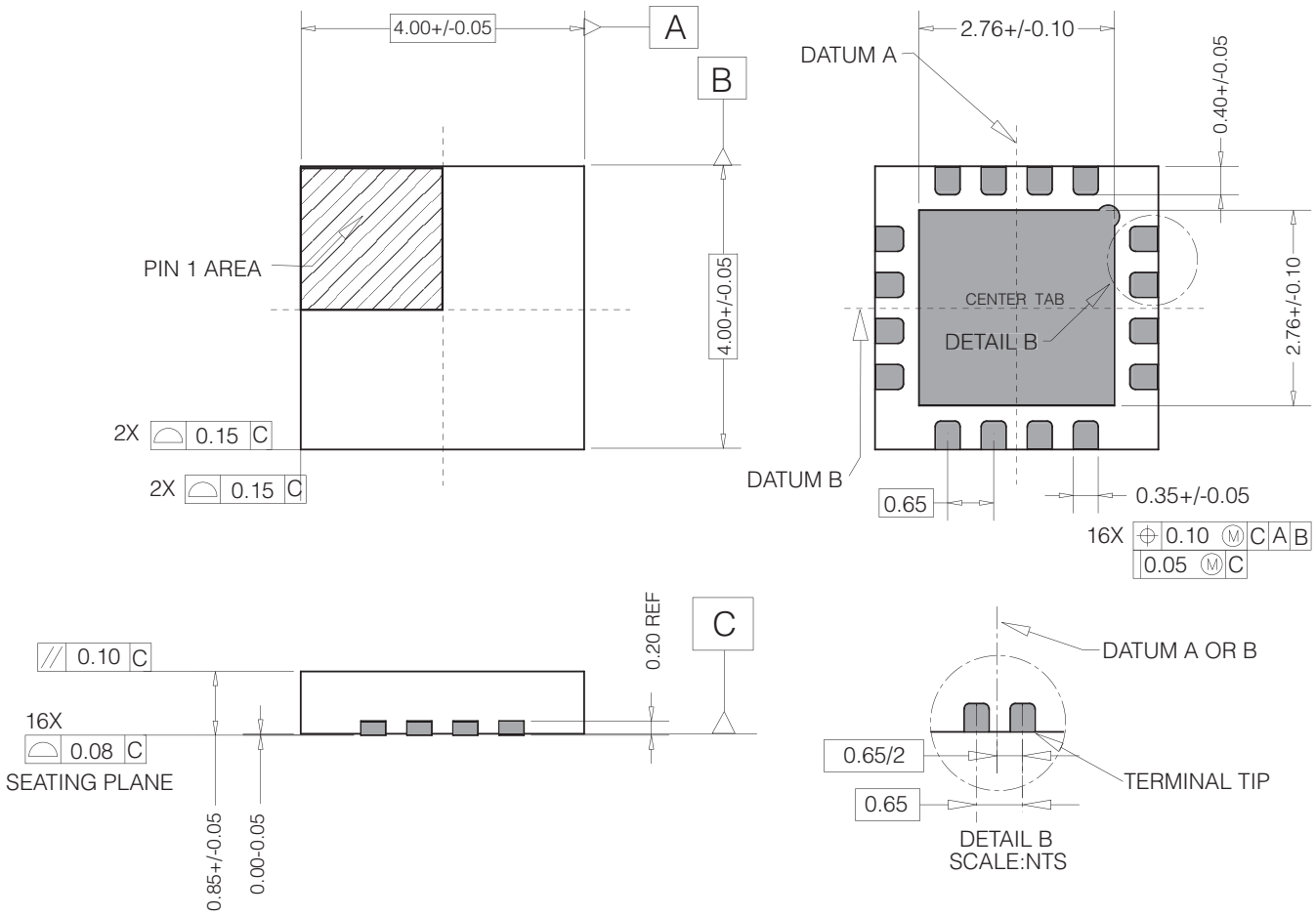


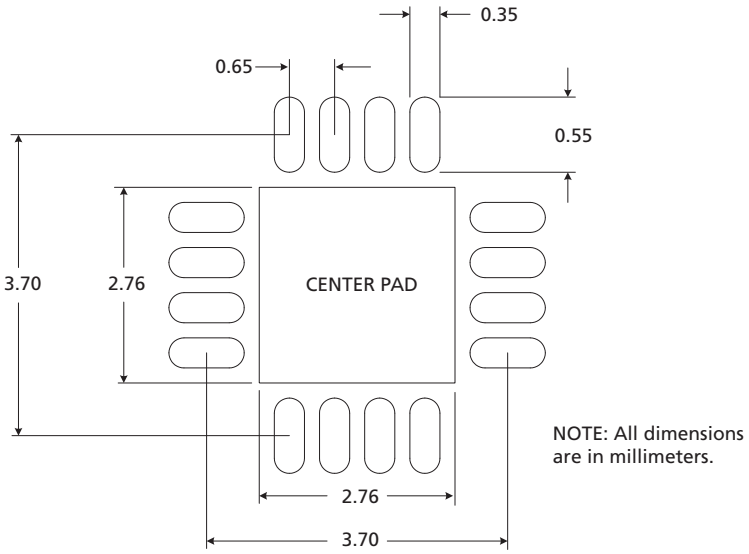
Figure 5-4: Control Input ($\overline{\text{DISABLE2}}$)

6. Package & Ordering Information

6.1 Package Dimensions



6.2 Recommended PCB Footprint



The Center Pad should be connected to the most negative power supply plane (VEE) by a minimum of five vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.3 Packaging Data

Parameter	Value
Package type / dimensions / pad pitch	16-pin QFN / 4mm x 4mm / 0.65mm
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi, Ψ	11.0°C/W
Pb-free and RoHS compliant, Halogen-free	Yes

6.4 Solder Reflow Profiles

The GS1679 device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 6-1.

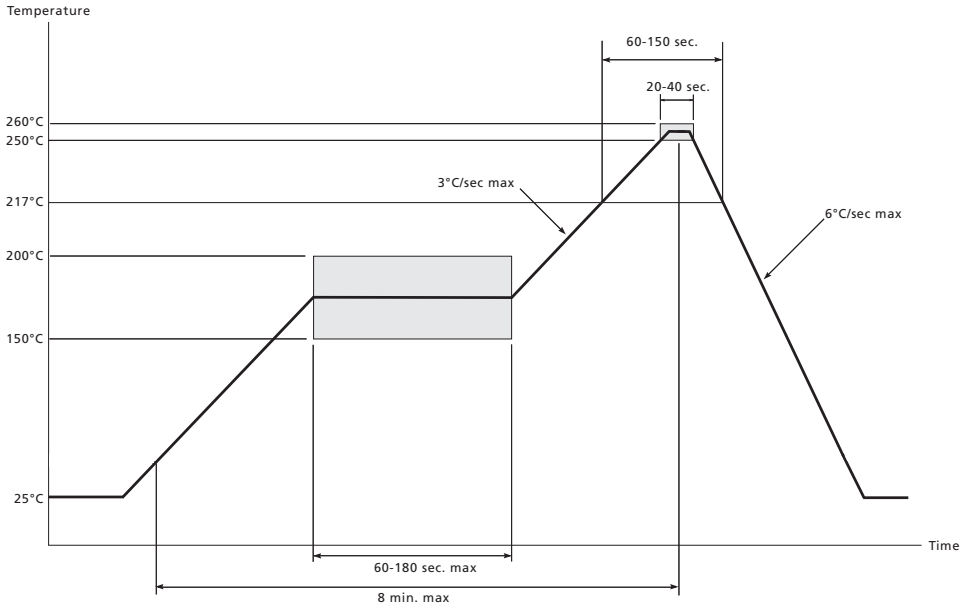
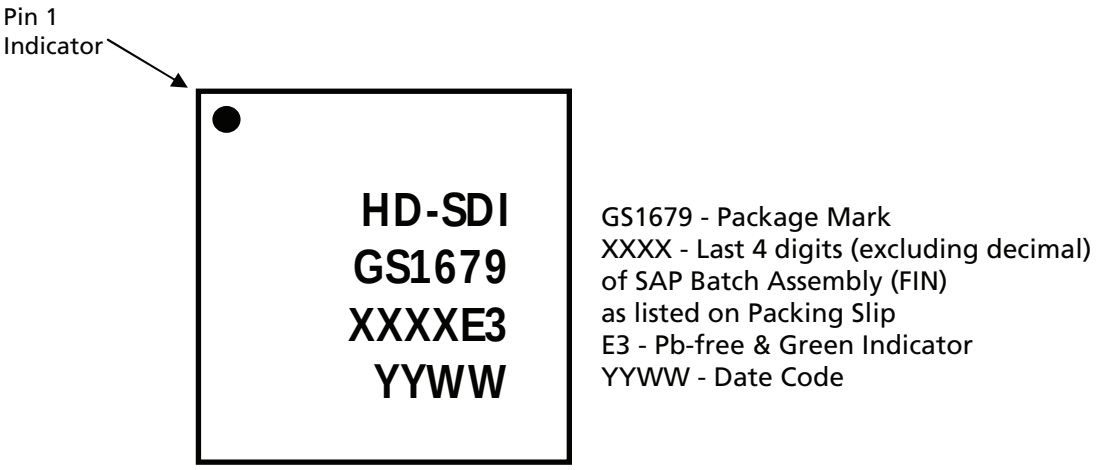


Figure 6-1: Maximum Pb-free Solder Reflow Profile

6.5 Marking Diagram



6.6 Ordering Information

	Part Number	Package	Temperature Range
GS1679	GS1679-INE3	16-pin QFN	-40°C to 85°C
GS1679	GS1679-INTE3	16-pin QFN 250pc Reel	-40°C to 85°C
GS1679	GS1679-INTE3Z	16-pin QFN 2,500pc Reel	-40°C to 85°C

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
1	155922	–	March 2011	Redefined pin #16 in Pin Assignment, Pin Descriptions and Typical Application Circuit. Revised Figure 3-2: V_{OUT} vs. RSET.
0	154128	–	May 2010	Converted to Data Sheet.
A	153976	–	April 2010	New document.

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

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