GW1NZ series of FPGA Products

Datasheet

DS841-2.7E, 4/25/2025

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Revision History

Date	Version	Description
01/23/2019	1.0E	Initial release.
02/12/2019	1.1E	Part naming figures updated.
04/03/2019	1.2E	● I/O BANK view updated. ● Description of I3C bus and SPMI added; Description of the tolerance of the on-chip oscillator added. ● Operating temperature changed to Junction temperature.
09/25/2019	1.3E	● Note of “The IOs of the GW1NZ-1 device do not support differential input” added. ● Power supply ramp rates updated.
11/06/2019	1.4E	The number of maximum I/Os updated.
01/06/2020	1.5E	● The static current of ZV devices added. ● Description of the low power feature of the User Flash added.
06/30/2020	1.6E	GW1NZ-1 FN32F added.
12/12/2020	1.7E	GW1NZ-2 added.
01/19/2021	1.7.1E	Information on I/O Standards updated.
01/27/2021	1.7.2E	GW1NZ-2 QN48/QN48M added.
02/26/2021	1.8E	GW1NZ-2 removed.
11/26/2021	1.8.1E	Information on I/O logic optimized.
11/18/2022	1.9E	● Note about DC current limit added. ● “Figure 2-1 Architecture Overview of GW1NZ-1” updated. ● “Table 2-1 Output I/O Standards and Configuration Options Supported by GW1NZ-1” updated. ● “Table 3-3 Power Supply Ramp Rates” updated. ● “Table 3-5 POR Parameters” updated. ● “Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions” updated. ● “Table 3-12 Recommended I/O Operating Conditions” updated. ● Section 3.6.4 Byte-enable removed. ● Description of configuration Flash added.
02/27/2023	2.0E	● “Table 3-1 Absolute Max. Ratings” updated. ● “Table 3-23 User Flash Timing Parameters” updated. ● “Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions” updated. ● Information on Slew Rate removed. ● Description added to “2.7User Flash (GW1NZ-1)”.
07/20/2023	2.1E	● Note about the default state of GPIOs modified. ● The I/O logic output diagram and the I/O logic input diagram combined into “Figure 2-8 I/O Logic Input and Output”.

Date	Version	Description
		● Description of Flash resources updated. ● “2.6.2BSRAM Configuration Modes” added. ● “Table 3-3 Power Supply Ramp Rates” updated. ● “Table 3-9 Static Current(LV Version)” updated. ● “Figure 4-3 Package Marking Examples” updated. ● GW1NZ-2 added.
08/18/2023	2.2E	● “Table 1-1 Product Resources” updated. ● “Table 1-2” and its notes updated. ● Note for “Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions” modified. ● “Table 3-23 User Flash Timing Parameters[1], [4], [5]” and its notes updated. ● “Figure 4-3 Package Marking Examples” updated. ● Note about default state of GPIOs optimized. ● Editorial updates.
09/08/2023	2.3E	● GW1NZ-1 FN24/CG25 added. ● “2.6.7 Power up Conditions” removed.
11/30/2023	2.4E	● GW1NZ-2 CS42 added. ● “Table 1-1 Product Resources” updated. ● Note added to “Table 2-3 Output I/O Standards and Configuration Options Supported by GW1NZ-2” and “Table 3-13 Single-ended I/O DC Characteristics”. ● “Table 3-2 Recommended Operating Conditions[1]” updated.
12/28/2023	2.4.1E	● “Table 1-1 Product Resources” updated. ● “Table 1-2 Device-Package Combinations and Maximum User I/Os (True LVDS Pairs)” updated. ● “Table 3-2 Recommended Operating Conditions[1]” updated. ● “Figure 2-6 I/O Bank Distribution View of GW1NZ-2” updated. ● Description of Flash resources updated.
07/12/2024	2.5E	● “Table 3-3 Power Supply Ramp Rates” updated, modifying ramp rate for V_{CC}. ● Recommended operating range of LV version V_{CC} modified. ● “Table 3-1 Absolute Max. Ratings” and “Table 3-2 Recommended Operating Conditions[1]” updated, adding voltage information for hard core MIPI D-PHY. ● Description of Bank6 in “Figure 2-6 I/O Bank Distribution View of GW1NZ-2” added. ● Note on Maximum GPIOs added to “Table 1-1 Product Resources”. ● Description of IODELAY module updated. ● “Table 3-13 Single-ended I/O DC Characteristics” updated, modifying I_{OL} and I_{OH} of LVCMOS12 standard. ● Note on functional description of dual port BSRAM and semi-dual port BSRAM modified.
02/28/2025	2.6E	● “Table 3-16 Gearbox Timing Parameters” and “Table

Date	Version	Description
		3-17 External Switching Characteristics” updated. ● “Table 1-2 Device-Package Combinations and Maximum User I/Os (True LVDS Pairs)” updated, correcting the number of maximum user IOs of the GW1NZ-2 device in the CS100H package. ● “Table 3-13 Single-ended I/O DC Characteristics” updated, modifying I_{OL} and I_{OH} of LVCMOS12 standard. ● Description of MIPI IO optimized. ● GW1NZ-2 CG56 added.
04/25/2025	2.7E	● “Table 2-1 Output I/O Standards and Configuration Options Supported by GW1NZ-1” and “Table 2-3 Output I/O Standards and Configuration Options Supported by GW1NZ-2” updated: correcting drive strength values for some I/O types. ● “Table 2-2 Input I/O Standards and Configuration Options Supported by GW1NZ-1” and “Table 2-4 Input I/O Standards and Configuration Options Supported by GW1NZ-2” updated: modifying V_{CCIO} values for some I/O types. ● “3.3.5 Differential I/O DC Characteristics” added.

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1 General Description

The GW1NZ series of FPGA products are the first generation products in the LittleBee family. They are non-volatile FPGA products featuring low power, instant-on, low-cost, enhanced security, small footprint, various packaging options, and flexible usage, and can be widely used in communication, industrial control, consumer, video surveillance, etc.

Gowin provides an advanced FPGA hardware development environment that supports FPGA synthesis, placement & routing, bitstream generation and download, etc.

1.1 Features

- Zero power consumption
  - 55nm embedded Flash technology
  - LV: Supports 1.1V/1.2V core voltage
  - ZV: Supports 0.9V/1.0V core voltage. Please refer to Table 3-10 for the static currents.
  - Supports dynamically turning on/off the clock
  - Supports dynamically turning on/off the User Flash
- Power Management (GW1NZ-1)
  - SPMI: system power management interface
  - VCC and VCCM independent in the device
- User Flash (GW1NZ-1)
  - NOR Flash
  - Can be turned on or off dynamically
  - Capacity: 64 Kbits
  - Data width: 32 bits
  - 10,000 write cycles
  - Greater than 10 years of data retention at +85℃
  - Page erase capability: 2048 bytes per page
  - Read duration: 25ns (Max)
  - Current

    Read operation: 2.19mA/25ns (V_{CC}) & 0.5mA/25ns (V_{CCX}) (Max)

    Program/erase operation: 12/12mA(Max)
  - Fast Page Erase/Word Program Operation
  - Clock frequency: 40 MHz
  - Word Program Time: ≤16μs
  - Page Erase Time: ≤120 ms
- User Flash (GW1NZ-2)
  - 10,000 write cycles
  - Greater than 10 years of data retention at +85℃
  - Data width: 32 bits
  - Capacity: 96 Kbits
  - Page Erase Capability: 2,048 bytes per page
  - Word Program Time: ≤16μs
  - Page Erase Time: ≤120 ms
- Configuration Flash (GW1NZ-1)

  - NOR Flash
  - 10,000 write cycles
  - Greater than 10 years of data retention at +85℃
- Configuration Flash (GW1NZ-2)
  - NOR Flash
  - 10,000 write cycles
  - Greater than 10 years of data retention at +85℃
- Hard MIPI D-PHY RX core (GW1NZ-2)
  - Supports MIPI CSI-2 and DSI RX
  - Available on Bank6
  - MIPI data rate up to 2Gbps per lane
  - Supports up to 4 data lanes and 1 clock lane
- MIPI D-PHY RX/TX Implemented by Using GPIOs
  - Supports MIPI CSI-2 and MIPI DSI RX/TX with a data rate of up to 1.2Gbps per lane
  - Three IO types are available: TLVDS, ELVDS, and MIPI IO. GW1NZ-1 only supports ELVDS output. For more information, see 2.9.2 MIPI D-PHY RX/TX Implemented by Using GPIOs
- Multiple I/O standards
  - GW1NZ-1：LVCMOS33/25/18/15/12；LVTTL33，PCI，LVDS25E，BLVDSE，MLVDSE，LVPECLE，RSDSE
  - GW1NZ-2：LVCMOS33/25/18/15/12；LVTTL33，SSTL33/25/18 I，SSTL33/25/18 II，SSTL15；HSTL18 I，HSTL18 II，HSTL15 I；PCI，LVDS25，RSDS，LVDS25E，BLVDSE，MLVDSE，LVPECLE，RSDSE
  - Input hysteresis options
  - Drive strength options
  - Individual Bus Keeper, Pull-up/Pull-down, and Open Drain options
  - Hot socketing
  - Hard I3C core supporting SDR mode
- Abundant basic logic cells
  - 4-input LUTs (LUT4s)
  - Supports shift registers and shadow SRAMs
- Block SRAMs with multiple modes
  - Supports Dual Port mode, Single Port mode, and Semi-Dual Port mode
  - Supports byte-enable
- Flexible PLLs
  - Frequency adjustment (multiplication and division) and phase adjustment
  - Supports global clocks
- Built-in Flash programming
  - Instant-on
  - Supports security bit operation
  - Supports AUTO BOOT and DUAL BOOT
- Configuration
  - JTAG configuration[1]

    Note!

    [1] The GW1NZ-1 device in the CG25/FN24 packages does not support JTAG configuration mode.
  - Supports up to six GowinCONFIG configuration modes: AUTO BOOT, SSPI, MSPI, CPU, SERIAL, DUAL BOOT

1.2 Product Resources

Table 1-1 Product Resources

Device	GW1NZ-1	GW1NZ-2
LUT4s	1,152	2,304
Registers	864	2,016
Shadow SRAM (SSRAM) Capacity (bits)	4K	18K
Block SRAM (BSRAM) Capacity (bits)	72K	72K
PLLs	1	1
User Flash(bits)	64K	96K
Maximum GPIOs[1]	48	125
Core Voltage Typ.(LV Version)	1.1V/1.2V	1.1V/1.2V
Core Voltage Typ.(ZV Version)	0.9V/1.0V	0.9V/1.0V

Note!

[1] This is the maximum number of GPIOs the device can provide without package limitation. Please refer to Table 1-2 for the maximum number of user I/Os available for the specific packages.

1.3 Package Information

Table 1-2 Device-Package Combinations and Maximum User I/Os (True LVDS Pairs)

Package	Pitch (mm)	Size (mm)	GW1NZ-1	GW1NZ-2
CG25	0.35	1.8 x 1.8	20	-
CG56	0.35	2.4 x 2.9	-	46 (14)
CS100H	0.4	4 x 4	-	79 (21)
CS16	0.4	1.8 x 1.8	11	-
CS42	0.4	2.4 x 2.9	-	35 (11)
FN24	0.4	3 x 3	18	-
FN32	0.4	4 x 4	25	-
FN32F	0.4	4 x 4	25	-
QN48	0.4	6 x 6	41	41 (12)

Note!

- The package types in this manual are referred to by acronyms, see 4.1 Part Naming for more information.
- JTAGSEL_N and JTAG pins cannot be used as GPIOs simultaneously. However, when mode [2:0] = 001, the JTAGSEL_N pin is always a GPIO, in other words the JTAGSEL_N pin and the four JTAG pins (TCK, TMS, TDI, TDO) can be used as GPIOs simultaneously.

2 Architecture

2.1 Architecture Overview

Figure 2-1 Architecture Overview of GW1NZ-1

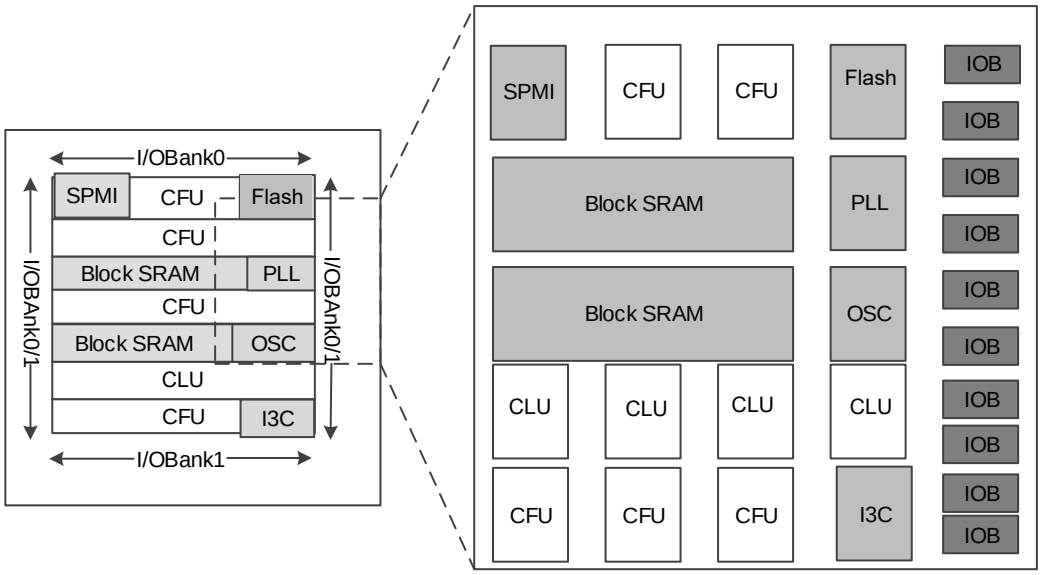
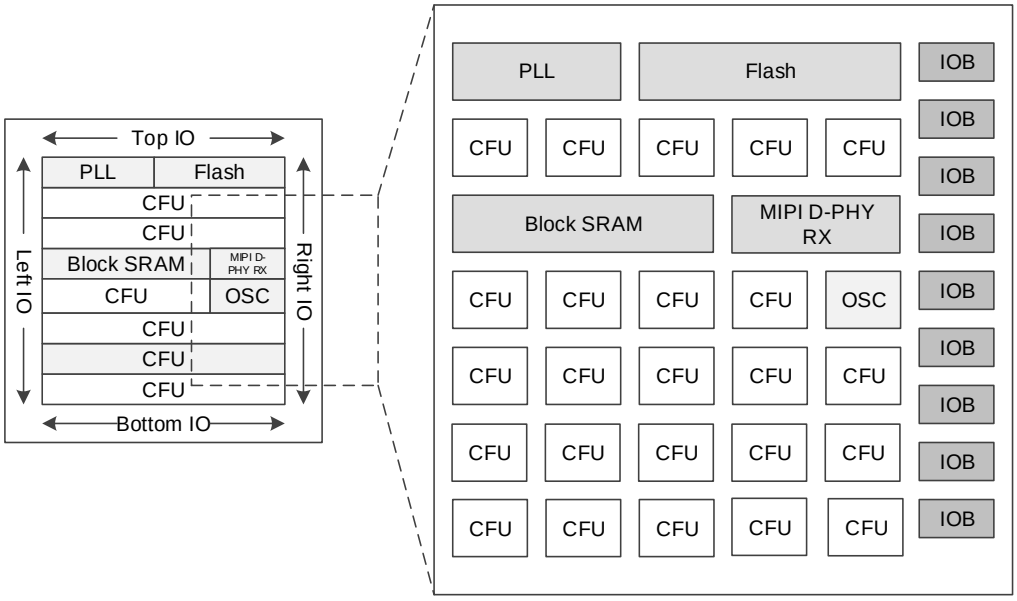


Figure 2-2 Architecture Overview of GW1NZ-2



As shown in Figure 2-1 and Figure 2-2, the core of the FPGA is an array of logic cells surrounded by IO blocks. Besides, BSRAMs, PLLs, an on-chip oscillator, and Flash resources that support instant-on are provided. In addition, GW1NZ-1 is embedded with an SPMI module and an I3C module. See Table 1-1 for more information on the resources provided.

The Configurable Function Unit (CFU) and the Configurable Logic Unit (CLU) are the two kinds of basic logic blocks that form the core of Gowin FPGAs. Devices with different capacities have different numbers of rows and columns of CFUs/CLUs. The CFU can be configured into LUT4 mode, ALU mode, and memory mode. See 2.2 Configurable Function Units for more information.

The I/O resources in the GW1NZ series of FPGA products are arranged around the periphery of the devices in groups referred to as banks. The I/O resources support multiple I/O standards and can be used for regular mode, SDR mode, and generic DDR mode. See 2.3 Input/Output Blocks for more information.

BSRAMs are arranged in row(s) inside the GW1NZ series of FPGA products. Each BSRAM has a capacity of 18 Kbits and supports multiple configuration modes and operation modes. See 2.6 Block SRAM for more information.

The GW1NZ series of FPGA products feature embedded Flash resources with a capacity of 1 Mbits. Configuration Flash resources are used for internal Flash programming, see 2.13 Programming & Configuration for more information. User Flash resources are used for user storage, see 2.8 User Flash (GW1NZ-2) for more information.

The GW1NZ-2 device contains a hard MIPI D-PHY RX core, see 2.9 MIPI D-PHY(GW1NZ-2) for more information.

The GW1NZ series of FPGA products have embedded PLL resources. The PLLs can provide synthesizable clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be realized by configuring the parameters. In addition, an programmable on-chip oscillator is provided, see 2.10 Clocks and 2.14 On-chip Oscillator for more information.

There are also abundant Configurable Routing Units (CRUs) that interconnect all the resources within the FPGA. For example, routing resources distributed in CFUs and IOBs interconnect resources in them. Routing resources can be automatically generated by the Gowin software. In addition, the GW1NZ series of FPGA products also provide abundant dedicated clock resources, long wires (LWs), global set/reset (GSR) resources, programming options, etc. See 2.10 Clocks, 2.11 Long Wires, 2.12 Global Set/Reset for more information.

2.2 Configurable Function Units

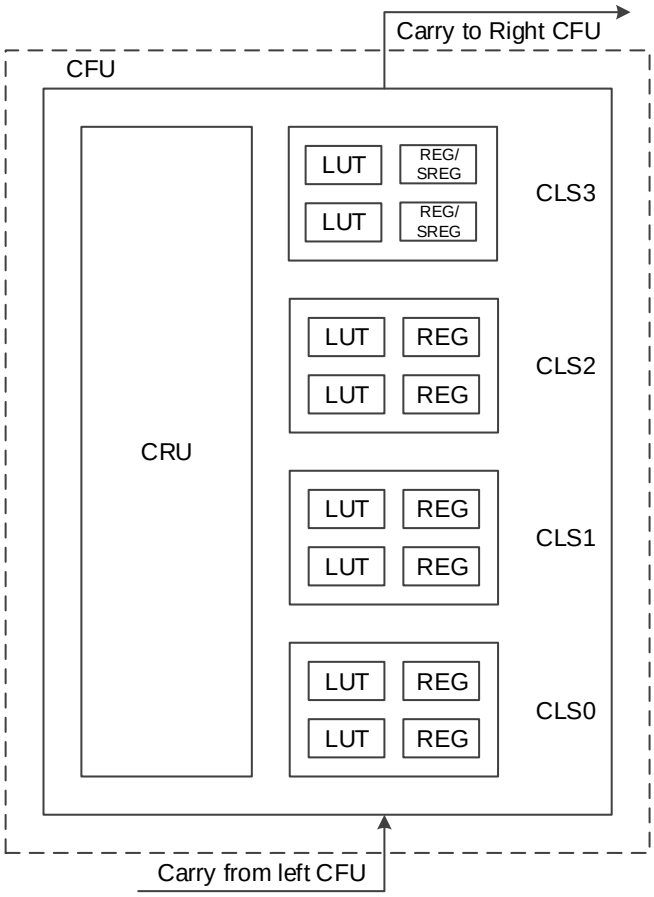
Configurable Function Units (CFUs) and/or Configurable Logic Units (CLUs) are the basic cells that make up the core of Gowin FPGAs. Each basic cell consists of four Configurable Logic Sections (CLSs) and their routing resource Configurable Routing Units (CRUs), with three of the

CLSs each containing two 4-input LUTs and two registers, and the remaining one only containing two 4-input LUTs, as shown in Figure 2-3.

The CLSs in the CLUs cannot be configured as SRAMs, but can be configured as basic LUTs, ALUs, and ROMs. The CLSs in the CFUs can be configured as basic LUTs, ALUs, SRAMs, and ROMs according to application scenarios.

For more information on the CFUs, see UG288, Gowin Configurable Function Unit (CFU) User Guide.

Figure 2-3 CFU Structure View



Note!

- The SREGs need special patch support. Please contact Gowin's technical support or local office for this patch.
- Only GW1NZ-2 supports the REGs in CLS3 currently, and the CLK, CE, and SR of CLS3 and CLS2 are driven by the same source.

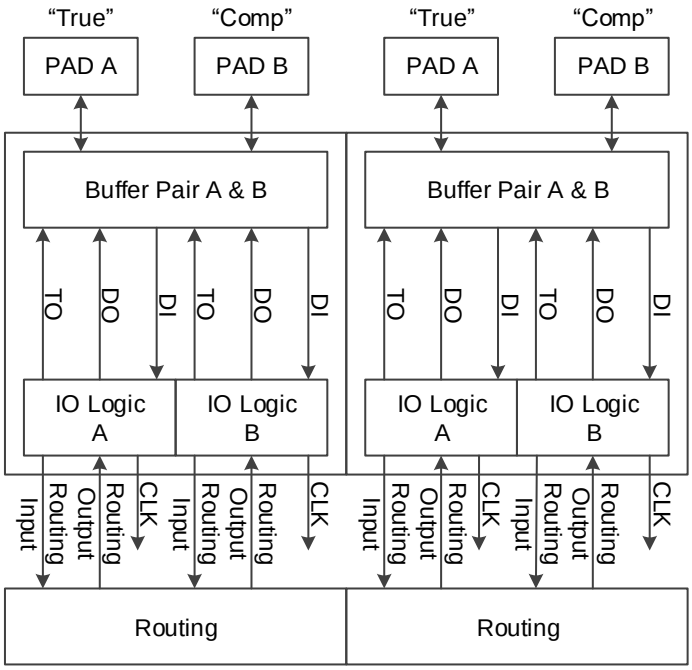
2.3 Input/Output Blocks

The Input/Output Block (IOB) in the GW1NZ series of FPGA products consists of a buffer pair, IO logic, and corresponding routing units. As shown in the figure below, each IOB connects to two pins (marked as A and B), which can be used as a differential pair or as two single-ended inputs/outputs.

Note!

The IOs of the GW1NZ-1 device do not support differential input.

Figure 2-4 IOB Structure View



The features of the IOB include:

- V_{CCIO} supplied to each bank
- LVCMOS, PCI, LVTTL, LVDS, SSTL, HSTL, etc.
- Input hysteresis options
- Drive strength options
- Individual Bus Keeper, Pull-up/Pull-down, and Open Drain options
- Hot socketing
- IO logic supports basic mode, SDR mode, DDR mode, etc.
- Hard I3C core supporting SDR mode(GW1NZ-1)

2.3.1 I/O Standards

There are two I/O banks in the GW1NZ-1 device, as shown in Figure 2-5. There are six I/O banks in the GW1NZ-2 device, while in the case of GW1NZ-2 in the CS100H package, there are seven banks, of which Bank6 is a dedicated MIPI Bank for MIPI D-PHY RX, as shown in Figure 2-6. Each bank has its own I/O power supply V_{CCIO}. V_{CCIO} can be 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V.

Note!

[1] If the MIPI function is not used, the pins of Bank6 can be left floating. Bank6 can also be used for differential inputs (with common mode voltage ≤ 0.5V) by bypassing the MIPI logic.

Figure 2-5 I/O Bank Distribution View of GW1NZ-1

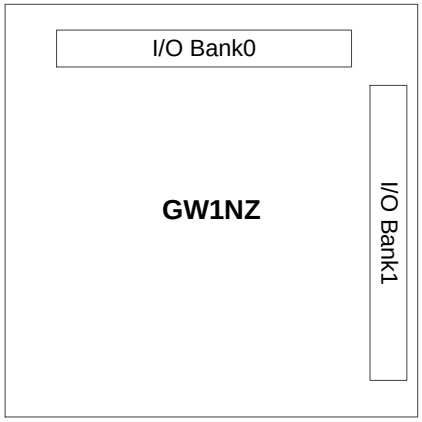
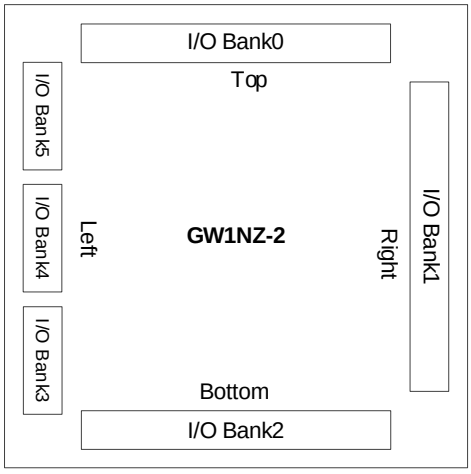
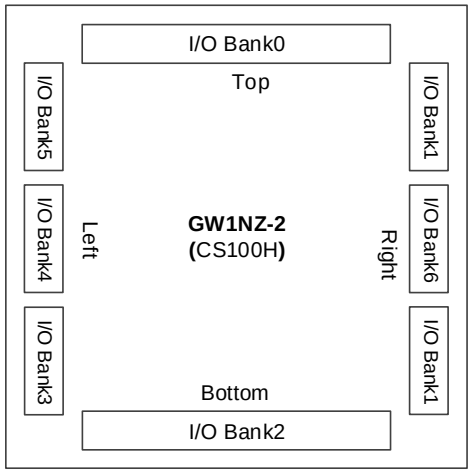


Figure 2-6 I/O Bank Distribution View of GW1NZ-2





The GW1NZ series of FPGA products support LV version and ZV version. The LV version devices support 1.1V/1.2V V_{CC} (core voltage), which can achieve low power consumption, and the ZV version devices support 0.9V/1.0V V_{CC}, which can achieve zero power consumption. V_{CCIO} (I/O bank voltage) can be set to 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V as needed. V_{CCX} (auxiliary voltage) supports 1.8V, 2.5V, and 3.3V.

Note!

During configuration, all GPIOs of the device are high-impedance with internal weak pull-ups. After the configuration is complete, the I/O states are controlled by user programs and constraints. The states of configuration-related I/Os differ depending on the configuration mode.

For the V_{CCIO} requirements of different I/O standards, see Table 2-1 to Table 2-4.

Table 2-1 Output I/O Standards and Configuration Options Supported by GW1NZ-1

I/O Type (output)	Single-ended/ Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
LVCMOS33/LVTTL33	Single-ended	3.3	4/8/12/16/24	Universal interface
LVCMOS25	Single-ended	2.5	4/8/12/16	Universal interface
LVCMOS18	Single-ended	1.8	4/8/12	Universal interface
LVCMOS15	Single-ended	1.5	4/8	Universal interface
LVCMOS12	Single-ended	1.2	4/8	Universal interface
PCI33	Single-ended	3.3	4/8	PC and embedded system
LVCMOS33D	Differential	3.3	4/8/12/16/24	Universal interface
LVCMOS25D	Differential	2.5	4/8/12/16	Universal interface
LVCMOS18D	Differential	1.8	4/8/12	Universal interface
LVCMOS15D	Differential	1.5	4/8	Universal interface
LVCMOS12D	Differential	1.2	4/8	Universal interface

Table 2-2 Input I/O Standards and Configuration Options Supported by GW1NZ-1

I/O Type(input)	Single-ended/ Differential	Bank V_{CCIO}(V)	Hysteresis Options Supported?	V_{REF} Required?
LVCMOS33/LVTTL33	Single-ended	3.3	Yes	No
LVCMOS25	Single-ended	2.5	Yes	No
LVCMOS18	Single-ended	1.8	Yes	No
LVCMOS15	Single-ended	1.5	Yes	No
LVCMOS12	Single-ended	1.2	Yes	No
PCI33	Single-ended	3.3	Yes	No
LVCMOS33OD25	Single-ended	2.5	Yes	No
LVCMOS33OD18	Single-ended	1.8	Yes	No
LVCMOS33OD15	Single-ended	1.5	Yes	No
LVCMOS25OD18	Single-ended	1.8	Yes	No

I/O Type(input)	Single-ended/ Differential	Bank V_{CCIO}(V)	Hysteresis Options Supported?	V_{REF} Required?
LVCMOS25OD15	Single-ended	1.5	Yes	No
LVCMOS18OD15	Single-ended	1.5	Yes	No
LVCMOS15OD12	Single-ended	1.2	Yes	No
LVCMOS25UD33	Single-ended	3.3	Yes	No
LVCMOS18UD25	Single-ended	2.5	Yes	No
LVCMOS18UD33	Single-ended	3.3	Yes	No
LVCMOS15UD18	Single-ended	1.8	Yes	No
LVCMOS15UD25	Single-ended	2.5	Yes	No
LVCMOS15UD33	Single-ended	3.3	Yes	No
LVCMOS12UD15	Single-ended	1.5	Yes	No
LVCMOS12UD18	Single-ended	1.8	Yes	No
LVCMOS12UD25	Single-ended	2.5	Yes	No
LVCMOS12UD33	Single-ended	3.3	Yes	No

Table 2-3 Output I/O Standards and Configuration Options Supported by GW1NZ-2

I/O Type (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
MIPI[1]	Differential (TLVDS)	1.2	3.5	Mobile Industry Processor Interface
LVDS25	Differential (TLVDS)	2.5/3.3	2.5/3.5/4.5/6	High-speed point-to-point data transmission
RSDS	Differential (TLVDS)	2.5/3.3	2.5	High-speed point-to-point data transmission
MINILVDS	Differential (TLVDS)	2.5/3.3	2.5	LCD timing driver interface and column driver interface
PPLVDS	Differential (TLVDS)	2.5/3.3	3.5	LCD row/column driver
LVDS25E	Differential	2.5	8	High-speed point-to-point data transmission
BLVDS25E	Differential	2.5	16	Multi-point high-speed data transmission
MLVDS25E	Differential	2.5	16	LCD timing driver interface and column driver interface

I/O Type (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
RSDS25E	Differential	2.5	8	High-speed point-to-point data transmission
LVPECL33E	Differential	3.3	16	Universal interface
HSTL18D_I	Differential	1.8	8	Memory interface
HSTL18D_II	Differential	1.8	8	Memory interface
HSTL15D_I	Differential	1.5	8	Memory interface
SSTL15D	Differential	1.5	8	Memory interface
SSTL18D_I	Differential	1.8	8	Memory interface
SSTL18D_II	Differential	1.8	8	Memory interface
SSTL25D_I	Differential	2.5	8	Memory interface
SSTL25D_II	Differential	2.5	8	Memory interface
SSTL33D_I	Differential	3.3	8	Memory interface
SSTL33D_II	Differential	3.3	8	Memory interface
LVCMOS12D	Differential	1.2	2/6	Universal interface
LVCMOS15D	Differential	1.5	4/8	Universal interface
LVCMOS18D	Differential	1.8	4/8/12	Universal interface
LVCMOS25D	Differential	2.5	4/8/12/16	Universal interface
LVCMOS33D	Differential	3.3	4/8/12/16	Universal interface
HSTL15_I	Single-ended	1.5	8	Memory interface
HSTL18_I	Single-ended	1.8	8	Memory interface
HSTL18_II	Single-ended	1.8	8	Memory interface
SSTL15	Single-ended	1.5	8	Memory interface
SSTL18_I	Single-ended	1.8	8	Memory interface
SSTL18_II	Single-ended	1.8	8	Memory interface
SSTL25_I	Single-ended	2.5	8	Memory interface
SSTL25_II	Single-ended	2.5	8	Memory interface
SSTL33_I	Single-ended	3.3	8	Memory interface

I/O Type (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
SSTL33_II	Single-ended	3.3	8	Memory interface
LVCMOS12	Single-ended	1.2	2/6	Universal interface
LVCMOS15	Single-ended	1.5	4/8	Universal interface
LVCMOS18	Single-ended	1.8	4/8/12	Universal interface
LVCMOS25	Single-ended	2.5	4/8/12/16	Universal interface
LVCMOS33/ LVTTL33	Single-ended	3.3	4/8/12/16	Universal interface
PCI33	Single-ended	3.3	4/8	PC and embedded system

Note!

- [1] Bank0/Bank3/Bank4/Bank5 of the GW1NZ-2 device support MIPI output by using MIPI IO type.

Table 2-4 Input I/O Standards and Configuration Options Supported by GW1NZ-2

I/O Type(input)	Single-ended/Differential	Bank V_{CCIO}(V)	Hysteresis Options Supported?	V_{REF} Required?
MIPI[1]	Differential (TLVDS)	1.2	No	No
LVDS25	Differential (TLVDS)	2.5/3.3	No	No
RSDS	Differential (TLVDS)	2.5/3.3	No	No
MINILVDS	Differential (TLVDS)	2.5/3.3	No	No
PPLVDS	Differential (TLVDS)	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33E	Differential	3.3	No	No
HSTL18D_I	Differential	1.8	No	No
HSTL18D_II	Differential	1.8	No	No
HSTL15D_I	Differential	1.5	No	No
SSTL15D	Differential	1.5	No	No
SSTL18D_I	Differential	1.8	No	No
SSTL18D_II	Differential	1.8	No	No
SSTL25D_I	Differential	2.5	No	No
SSTL25D_II	Differential	2.5	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
LVCMOS12D	Differential	1.2	No	No
LVCMOS15D	Differential	1.5	No	No
LVCMOS18D	Differential	1.8	No	No
LVCMOS25D	Differential	2.5	No	No
LVCMOS33D	Differential	3.3	No	No
HSTL15_I	Single-ended	1.5	No	Yes
HSTL18_I	Single-ended	1.8	No	Yes
HSTL18_II	Single-ended	1.8	No	Yes
SSTL15	Single-ended	1.5	No	Yes
SSTL18_I	Single-ended	1.8	No	Yes
SSTL18_II	Single-ended	1.8	No	Yes
SSTL25_I	Single-ended	2.5	No	Yes
SSTL25_II	Single-ended	2.5	No	Yes
SSTL33_I	Single-ended	3.3	No	Yes
SSTL33_II	Single-ended	3.3	No	Yes

I/O Type(input)	Single-ended/Differential	Bank V_{CCIO}(V)	Hysteresis Options Supported?	V_{REF} Required?
LVCMOS12	Single-ended	1.2	Yes	No
LVCMOS15	Single-ended	1.5	Yes	No
LVCMOS18	Single-ended	1.8	Yes	No
LVCMOS25	Single-ended	2.5	Yes	No
LVCMOS33/ LVTTL33	Single-ended	3.3	Yes	No
PCI33	Single-ended	3.3	Yes	No
LVCMOS33OD25	Single-ended	2.5	No	No
LVCMOS33OD18	Single-ended	1.8	No	No
LVCMOS33OD15	Single-ended	1.5	No	No
LVCMOS25OD18	Single-ended	1.8	No	No
LVCMOS25OD15	Single-ended	1.5	No	No
LVCMOS18OD15	Single-ended	1.5	No	No
LVCMOS15OD12	Single-ended	1.2	No	No
LVCMOS25UD33	Single-ended	3.3	No	No
LVCMOS18UD25	Single-ended	2.5	No	No
LVCMOS18UD33	Single-ended	3.3	No	No
LVCMOS15UD18	Single-ended	1.8	No	No
LVCMOS15UD25	Single-ended	2.5	No	No
LVCMOS15UD33	Single-ended	3.3	No	No
LVCMOS12UD15	Single-ended	1.5	No	No
LVCMOS12UD18	Single-ended	1.8	No	No
LVCMOS12UD25	Single-ended	2.5	No	No
LVCMOS12UD33	Single-ended	3.3	No	No

Note!

- [1] Bank6 (hard core) and Bank2 of GW1NZ-2 support MIPI I/O input.

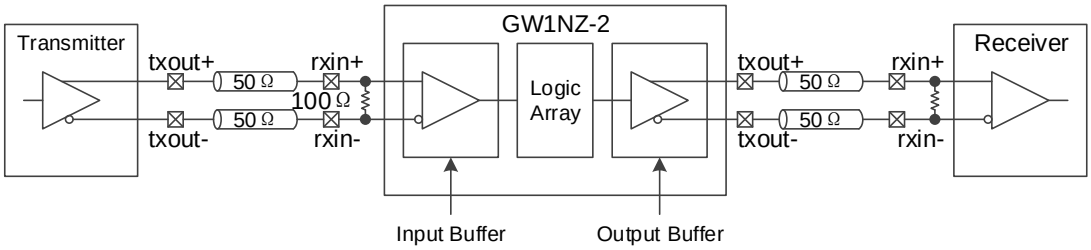
2.3.2 True LVDS Design(GW1NZ-2)

GW1NZ-2 supports true LVDS output as well as LVDS25E, MLVDS25E, BLVDS25E, etc.

For more information about true LVDS, see *UG847, GW1NZ-2 pinout.*

True LVDS input needs a 100Ω termination resistor, see Figure 2-7 for the reference design. Bank2 of the GW1NZ-2 device supports programmable on-chip 100Ω input differential termination resistors, see *UG289, Gowin Programmable IO User Guide*.

Figure 2-7 True LVDS Design



For information about termination for LVDS25E, MLVDS25E, and BLVDS25E, please refer to *UG289, Gowin Programmable IO User Guide*.

2.3.3 I/O Logic

Figure 2-8 shows the I/O logic input and output of the GW1NZ series of FPGA products.

Figure 2-8 I/O Logic Input and Output

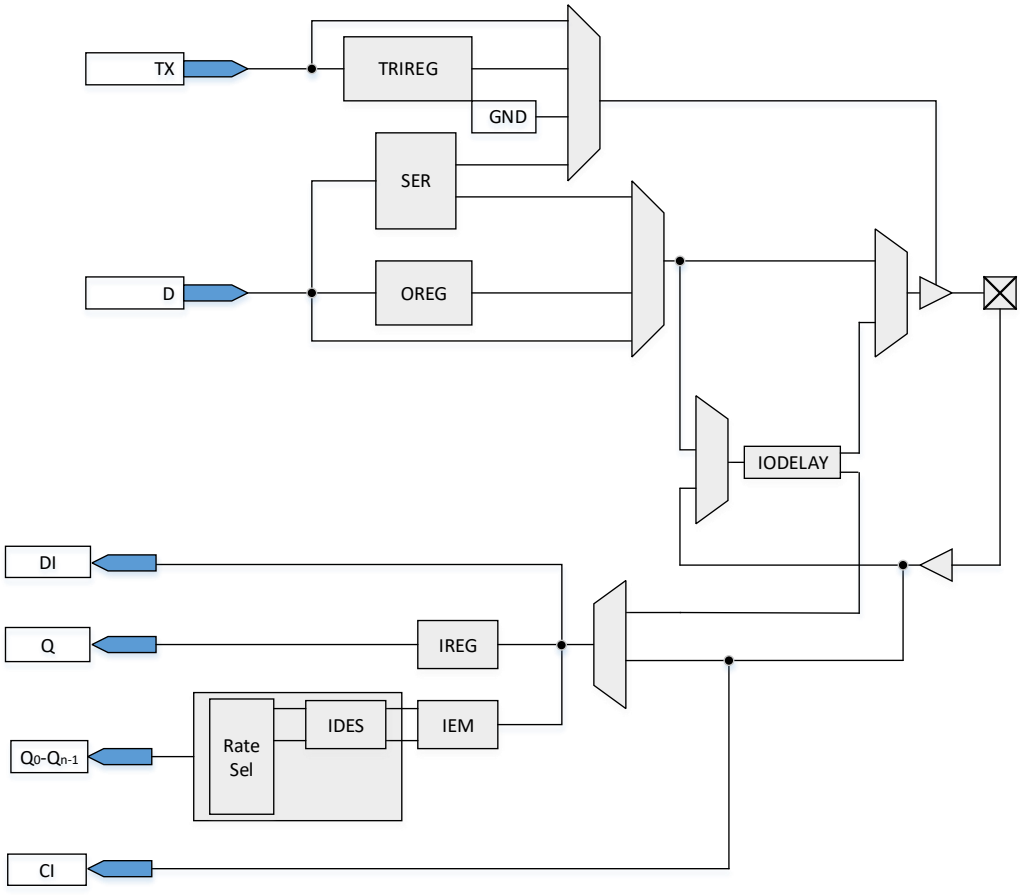


Table 2-5 Port Description

Port	I/O	Description
CI[1]	Input	GCLK input signal. For the number of GCLK input signals, please refer to *UG842，GW1NZ-1 Pinout* and *UG847，GW1NZ-2 Pinout*.
DI	Input	IO port low-speed input signal input into the fabric directly.
Q	Output	IREG output signal in the SDR module.
Q_0-Q_{n-1}	Output	IDES output signal in the DDR module.

Note!

[1] When CI is used as GCLK input, DI, Q, and Q_0-Q_{n-1} cannot be used as I/O input and output.

Descriptions of the I/O logic modules of the GW1NZ series of FPGA products are presented below.

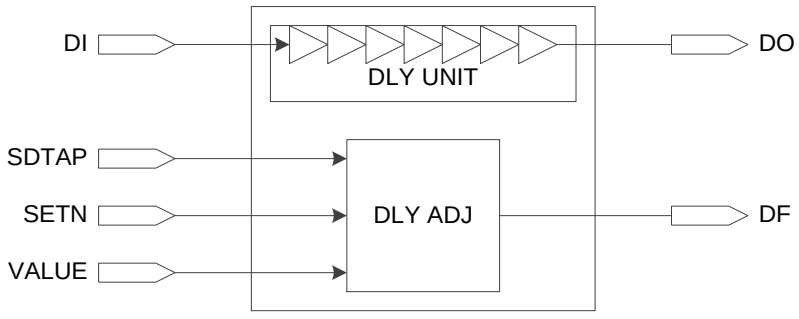
IODELAY

See Figure 2-9 for an overview of the IODELAY module. Each I/O of the GW1NZ series of FPGA products contains the IODELAY module, through which you can add additional delays to the I/O to adjust the delay of the signal. The delay time of each step is $T_{dlyunit}$, and the number of steps is DLYSTEP. The total delay time of IODELAY can be calculated as follows: $T_{totdly} = T_{dlyoffset} + T_{dlyunit} * DLYSTEP$. See Table 2-6 for the total delay time.

Table 2-6 Total Delay of IODELAY Module

	Min.	Typ.	Max.
$T_{dlyoffset}$	450ps	500ps	550ps
$T_{dlyunit}$	-	30ps	-
DLYSTEP	0	-	127

Figure 2-9 IODELAY Diagram



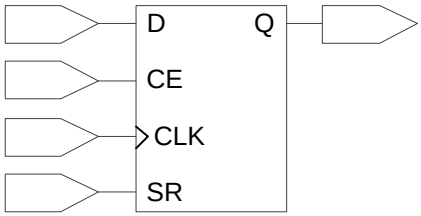
There are two ways to control the delay:

- Static control
- Dynamic control: can be used with the IEM module to adjust the dynamic sampling window. The IODELAY module cannot be used for both input and output at the same time.

I/O Register

See Figure 2-10 for the I/O register in the GW1NZ series of FPGA products. Each I/O provides one input register (IREG), one output register (OREG), and one tristate register (TRIREG).

Figure 2-10 I/O Register Diagram



Note!

- CE can be programmed as either active low (0: enable) or active high (1: enable).
- CLK can be programmed as either rising edge triggering or falling edge triggering.
- SR can be programmed as either synchronous/asynchronous SET/RESET or disabled.
- The register can be programmed as a register or a latch.

IEM

The IEM(Input Edge Monitor) module is used to sample data edges and is used in generic DDR mode, as shown in Figure 2-11.

Figure 2-11 IEM Diagram

DES

This series of FPGA products provide a simple deserializer(DES) for input I/O logic to support advanced I/O protocols.

SER

This series of FPGA products provide a simple serializer(SER) for output I/O logic to support advanced I/O protocols.

2.3.4 I/O Logic Modes

The I/O Logic of the GW1NZ series of FPGA products supports several operation modes. In each operation mode, the I/O (or I/O differential pair) can be configured as output, input, INOUT or tristate output (output signal with tristate control).

Pins IOR6 (A,B,C….J) of GW1NZ-1 do not support IO logic.

For more information about I/O logic modes, please refer to UG289, Gowin Programmable IO User Guide.

2.4 I3C Bus (GW1NZ-1)

2.4.1 Overview

The GW1NZ series of FPGA products is embedded with a hard I3C bus controller IP core that supports SDR mode. The I3C bus is backward compatible with I2C, featuring low power consumption, high speed, and scalability. This I3C bus, compliant with the MIPI I3C specification, uses the register interface, and supports I3C SDR Master mode and I3C SDR Slave mode.

2.4.2 Features

I3C SDR Master

- Compliant with MIPI I3C specification.
- Supports I3C address arbitration detection.
- Supports Single Data Rate (SDR) mode.
- The data rate can be up to 12.5Mbps.
- Start / Stop / Repeated Start / Acknowledge generation.
- Start / Stop / Repeated Start detection.
- Supports dynamic address assignment via SETDASA or ENTDAA.
- Supports receiving/sending data.
- Supports In-band Interrupts.
- Supports Hot-Join.
- Supports dynamic address assignment upon Hot-Join.
- Supports Common Command Codes (CCCs).
- Supports dynamically adjusting the SCL frequency.
- Compatible with I^2C Slaves.
- Uses the register interface.

I3C SDR Slave

- Compliant with MIPI I3C specification.
- Start / Acknowledge generation.
- Start / Stop / Repeated Start detection.
- Supports dynamic address assignment via SETDASA or ENTDAA.
- Supports receiving/sending data.
- Supports sending an IBI or hot-join request. If more than one slave sends an IBI or Hot-Join request, the slave with the lowest address wins the arbitration.
- Supports configuring the static address of the slave.
- Uses the register interface.

2.4.3 Signal Description

For more information about I3C signals, operations, timing, and examples, please refer to *IPUG508, Gowin I3C SDR IP User Guide*.

Table 2-7 I3C Signals

Port Name	Direction	Description
AAC	Input	Clears the ACK response setting. single pulse signal
AAO	Output	Outputs the ACK signal
AAS	Input	Sets the ACK response. single pulse signal
ACC	Input	Clears the continuous operation mode setting. single pulse signal
ACKHS	Input	Sets the ACK high time
ACKLS	Input	Sets the ACK low time
ACO	Output	Continuous operation mode output
ACS	Input	Sets continuous operation mode. single pulse signal
ADDRS	Input	Sets the slave address
CE	Input	Clock enable signal
CLK	Input	Clock input
CMC	Input	Clears the current master role. single pulse signal
CMO	Output	Master output
CMS	Input	Sets the device as the master. single pulse signal
DI[7:0]	Input	Data input
DO[7:0]	Output	Data output
DOBUF[7:0]	Output	Buffer data output
LGYC	Input	Clears the setting that the current communication object is an I2C device. single pulse signal
LGYO	Output	The current communication object being an I2C device
LGYS	Input	Set the current communication object as an I2C device. single pulse signal
PARITYERROR	Output	Parity error signal
RECVDHS	Input	Sets the high time when receiving data
RECVDLS	Input	Sets the low time when receiving data
RESET	Input	Asynchronous reset, active high
SCLI	Input	I3C serial clock input
SCLO	Output	I3C serial clock output
SCLOEN	Output	I3C serial clock output enable
SCLPULLO	Output	I3C serial clock pull-up output
SCLPULLOEN	Output	I3C serial clock pull-up output enable
SDAI	Input	I3C serial data input
SDAO	Output	I3C serial data output
SDAOEN	Output	I3C serial data output enable
SDAPULLO	Output	I3C serial data pull-up output
SDAPULLOEN	Output	I3C serial data pull-up output enable

Port Name	Direction	Description
SENDAHS	Input	Sets the high time when sending address
SENDALS	Input	Sets the low time when sending address
SENDDHS	Input	Sets the high time when sending data
SENDDLS	Input	Sets the low time when sending data
SIC	Input	Sets the interrupt flag clear signal
SIO	Output	Outputs the interrupt flag
STRTC	Input	Clears the START command setting. single pulse signal
STRTO	Output	Outputs the START command
STRTS	Input	Sets the START command. single pulse signal
STATE	Output	Outputs the internal state
STRTHDS	Input	Sets the hold time of the START command
STOPC	Input	Clears the STOP command setting. single pulse signal
STOPO	Output	Outputs the STOP command
STOPS	Input	Sets the STOP command. single pulse signal
STOPSUS	Input	Sets the set-up time of the STOP command
STOPHDS	Input	Sets the hold time of the STOP command

2.5 SPMI (GW1NZ-1)

2.5.1 Overview

The GW1NZ-1 device provides an SPMI module as well as an SPMI controller IP. As a master, it supports controlling external slave devices through the SPMI interface for power management. As a slave, it supports FPGA power management.

The GW1NZ-1 device supports controlling the main power supply in the following way: you can turn off the main power supply by sending the shutdown command from the master. And the main power supply of the FPGA can be restored by sending the reset/sleep/wakeup command from the master, or by a low-going pulse of the SPMI_EN signal.

For more information on operation modes, communication modes, supported commands, timing, etc, please refer to *IPUG529, Gowin SPMI User Guide*.

2.5.2 Signal Description

Table 2-8 SPMI Signals

Port Name	Direction	Description
SPMI_EN	Input	SPMI enable signal
SPMI_CLK	Input	System clock signal
SPMI_SCLK	Input/Output	SPMI serial clock signal
SPMI_SDATA	Input/Output	SPMI serial data signal

2.6 Block SRAM

2.6.1 Introduction

The GW1NZ series of FPGA products provide abundant block SRAM resources. These memory resources are distributed as blocks throughout the FPGA array in the form of rows. Therefore, they are called block static random access memories (BSRAMs). The capacity of each BSRAM can be up to 18,432 bits (18 Kbits). There are four configuration modes: Single Port mode, Dual Port mode, Semi-Dual Port mode, and ROM mode.

The abundant BSRAM resources are available for implementing high-performance designs. The features of BSRAMs include:

- Up to 18,432 bits per BSRAM
- Clock frequency up to 170MHz (100MHz in read-before-write mode)
- Supports Single Port mode
- Supports Dual Port mode
- Supports Semi-Dual Port mode
- Provides parity bits
- Supports ROM Mode
- Data widths from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Byte Enable function for 2-byte and above data widths
- Normal read and write
- Read-before-write
- Write-through

2.6.2 BSRAM Configuration Modes

BSRAMs in the GW1NZ series of FPGA products support various data widths, see Table 2-9.

Table 2-9 Memory Size Configuration

Single Port Mode	Dual Port Mode[1]	Semi-Dual Port Mode
16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32
2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36

Note!

[1] GW1NZ-1 does not support dual port mode.

Single Port Mode

The single port mode supports 2 read modes (Bypass mode and Pipeline mode) and 3 write modes (Normal mode, Write-Through mode, and Read-before-Write mode). In single port mode, writing to or reading from one port is supported. During the write operation, the written data will be transferred to the output of the BSRAM. When the output register is bypassed, the new data will show up at the same write clock rising edge.

For more information on single port mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

Dual Port Mode

The dual port mode supports 2 read modes (Bypass mode and Pipeline mode) and 2 write modes (Normal mode and Write-Through mode). The applicable operations are as follows:

- Two independent read operations
- Two independent write operations
- An independent read operation and an independent write operation

Note!

Performing read and write operations to the same address at the same time is not allowed.

For more information on dual port mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

Semi-Dual Port Mode

The semi-dual port mode supports 2 read modes (Bypass mode and Pipeline mode) and 1 write mode (Normal mode). Semi-dual port mode supports simultaneous read and write operations in the form of writing to port A and reading from port B.

Note!

Performing read and write operations to the same address at the same time is not allowed.

For more information on semi-dual port mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

ROM Mode

BSRAMs can be configured as ROMs. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization is completed during the device power-on process.

Each BSRAM can be configured as one 16Kbit ROM. For more information on ROM mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

2.6.3 Mixed Data Width Configuration

The BSRAMs in the GW1NZ series of FPGA products support mixed data width operations. In dual port mode and semi-dual port mode, the data widths for read and write can be different, see Table 2-10 and Table 2-11.

Table 2-10 Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

Note!

"*" denotes the modes supported.

Table 2-11 Semi-dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512 x 32	2K x 9	1K x 18	512 x 36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512 x 32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

Note!

"*" denotes the modes supported.

2.6.4 Byte-enable

BSRAMs support the byte-enable function. For data longer than a byte, the additional bits can be blocked, allowing only the selected portion to be written into the memory. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB) and byte-enable parameter options can be used to control the BSRAM write operation.

Note!

For the GW1NZ series, only GW1NZ-2 support the byte-enable function.

2.6.5 Parity Bit

There are parity bits in BSRAMs. The 9th bit in each byte can be used as a parity bit to check the correctness of data transmission. It can also be used for data storage.

2.6.6 Synchronous Operation

- All the input registers of BSRAMs support synchronous write.
- The output registers can be used as pipeline registers to improve design performance.
- The output registers are bypass-able.

2.6.7 BSRAM Operation Modes

The BSRAM supports five different operations, including two read modes (Bypass mode and Pipeline mode) and three write modes (Normal mode, Write-Through mode, and Read-before-Write mode).

Read Mode

The following two read modes are supported.

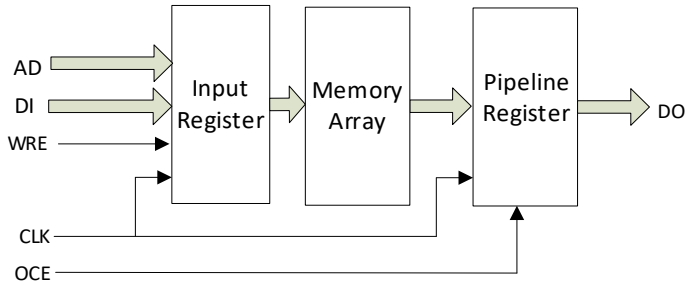
PIPELINE MODE

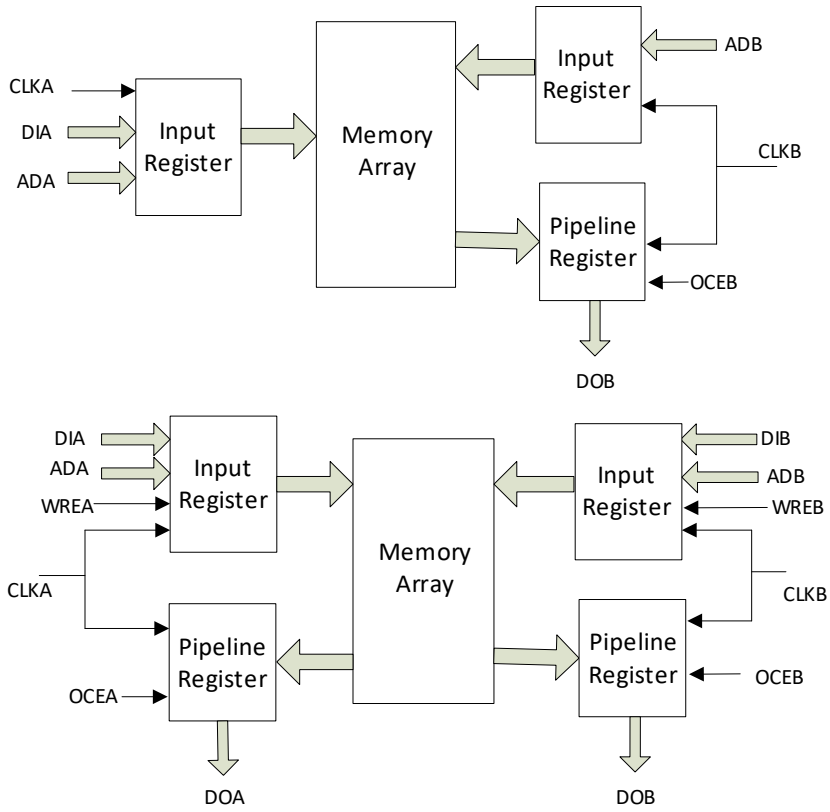
When a synchronous write cycles into a memory array with pipeline registers enabled, the data can be read from pipeline registers in the next clock cycle. The data bus can be up to 36 bits in this mode.

BYPASS MODE

When a synchronous write cycles into a memory array with pipeline registers bypassed, the outputs are registered at the memory array.

Figure 2-12 Pipeline Mode in Single Port Mode, Dual Port Mode, and Semi-dual Port Mode





Write Mode

NORMAL MODE

In this mode, when you write data to one port, the output data of this port does not change. The written data will not appear at the read port.

WRITE-THROUGH MODE

In this mode, when you write data to one port, the written data will appear at the output of this port.

READ-BEFORE-WRITE MODE

In this mode, when you write data to one port, the written data will be stored in the memory according to the address, and the original data in this address will appear at the output of this port.

2.6.8 Clock Mode

Table 2-12 lists the clock modes in different BSRAM modes:

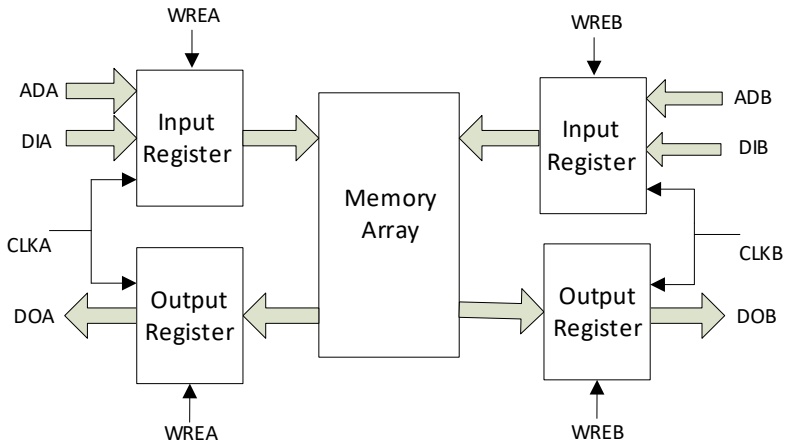
Table 2-12 Clock Modes in Different BSRAM Modes

Clock Mode	Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

Independent Clock Mode

Figure 2-13 shows the independent clock operation in dual port mode with one clock at each port. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

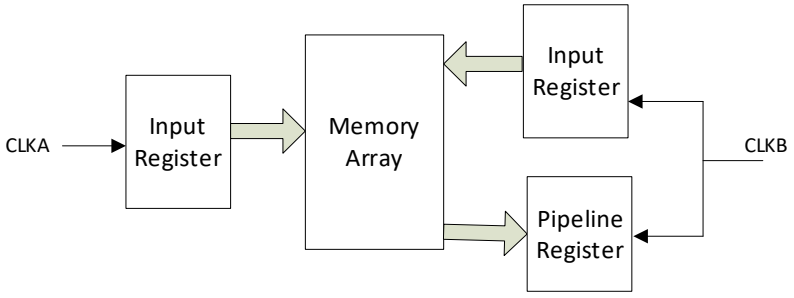
Figure 2-13 Independent Clock Mode



Read/Write Clock Mode

Figure 2-14 shows the read/write clock operation in semi-dual port mode with one clock at each port. The write clock (CLKA) controls data inputs, write addresses and write enable signals of Port A. The read clock (CLKB) controls data outputs, read addresses, and read enable signals of Port B.

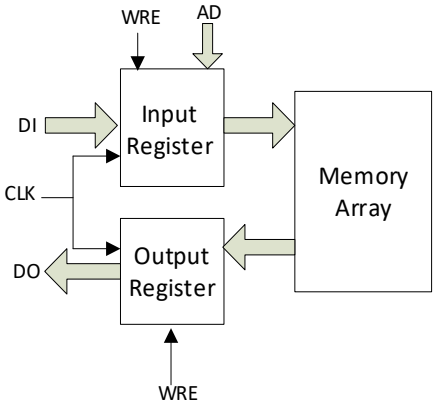
Figure 2-14 Read/Write Clock Mode



Single Port Clock Mode

Figure 2-15 shows the clock operation in single port mode.

Figure 2-15 Single Port Clock Mode



2.7 User Flash (GW1NZ-1)

2.7.1 Features

- NOR Flash
- 10,000 write cycles
- Capacity: 64 Kbits
- Greater than 10 years of data retention at +85℃
- Page erase capability: 2048 bytes per page
- Fast Page Erase/Word Program Operation
- Clock frequency: 40 MHz
- Word Program Time: ≤16μs
- Page Erase Time: ≤120 ms
- Current

– Read operation: 2.19mA/25ns (V_{CC}) & 0.5mA/25ns (V_{CCX})(MAX)
– Program/erase operation: 12/12mA (MAX)

2.7.2 Mode

There are two kinds of User Flash in the GW1NZ-1 devices: normal mode User Flash and low-power mode User Flash.

- The normal mode User Flash is on by default, so normal operations such as erase, read, and write can be performed after the FPGA device is powered up. The normal mode User Flash cannot be switched to the off state.
- The low-power mode User Flash is off by default, effectively minimizing power consumption. You can turn on/off the low-power mode User Flash dynamically by controlling the SLEEP pin. When the low-power mode User Flash is switched on, erase/read/write operations can be performed, just like the normal mode User Flash.

Different device versions and speed grades have different modes of User Flash, for more information, see Table 2-13.

Table 2-13 User Flash Modes

Mode	Default State	State Switching	Device Version	Speed Grade
Normal Mode	On	Not Supported	LV version	C6/I5
				C5/I4
			ZV version	C5/I4
Low-power Mode	Off	Dynamic Switching	ZV version	I2
				I3

For more information about the User Flash in GW1NZ-1, please refer to UG295, Gowin User Flash User Guide. For the correspondence between User Flash primitives and devices supported, please refer to Table 3-1 Devices Supported of UG295, Gowin User Flash User Guide.

2.8 User Flash (GW1NZ-2)

2.8.1 Introduction

The GW1NZ-2 device offers User Flash. The capacity of the User Flash in the GW1NZ-2 device is 96 Kbits. The User Flash consists of row memories and column memories. One row memory consists of 64 column memories. The capacity of one column memory is 32 bits, and the capacity of one row memory is 64*32=2048 bits. Page erase is supported, and the capacity of one page is 2048 bytes, that is, one page contains 8 rows. The key features include:

- NOR Flash
- 10,000 write cycles
- Greater than 10 years of data retention at +85℃
- Data width: 32 bits
- Capacity: 48 rows x 64 columns x 32 = 96 Kbits
- Page erase capability: 2,048 bytes per page
- Fast Page Erase/Word Program Operation
- Clock frequency: 40 MHz
- Word Program Time: ≤16μs
- Page Erase Time: ≤120 ms
- Current
  - Read current/duration: 2.19mA/25ns (V_{CC}) & 0.5mA/25ns (V_{CCX})(MAX)
  - Program/erase operation: 12/12mA(MAX)

For more information about the User Flash in GW1NZ-2, please refer to UG295, Gowin User Flash User Guide. For the correspondence between User Flash primitives and devices supported, please refer to Table 3-1 Devices Supported of UG295, Gowin User Flash User Guide.

2.9 MIPI D-PHY(GW1NZ-2)

2.9.1 Hard MIPI D-PHY RX Core(GW1NZ-2)

GW1NZ-2 provides a hard MIPI D-PHY RX core that supports the “MIPI Alliance Standard for D-PHY Specification(Version 2.1)”. The dedicated D-PHY core supports MIPI DSI and CSI-2 mobile video

interfaces for cameras and displays.

The key features include:

- Supports unidirectional high-speed (HS) mode at up to 8Gbps per quad(four data lanes)
- Supports up to 4 data lanes and 1 clock lane
- Supports bidirectional low-power (LP) mode at up to 10Mbps per lane
- Supports built-in HS Sync, bit and lane alignment
- Supports MIPI D-PHY RX 1:8 and 1:16 deserialization modes
- Supports MIPI DSI and MIPI CSI-2 link layers
- Available on Bank6

For more information, see IPUG778, Gowin GW1N-2 Hardened MIPI D-PHY RX User Guide..

2.9.2 MIPI D-PHY RX/TX Implemented by Using GPIOs

When implementing soft MIPI D-PHY RX/TX with GPIOs, three IO types are available: TLVDS, ELVDS, and MIPI IO.

GW1NZ-1 only supports ELVDS output. GW1NZ-2 supports TLVDS/ELVDS types. To implement MIPI D-PHY with the TLVDS/ELVDS types, you need to emulate MIPI HS and MIPI LP by using LVDS25(E)+LVCMOS12 and need to add external resistors.

In addition, GW1NZ-2 also supports MIPI IO type. The MIPI IO has an internal resistor network and supports automatic switching between HS and LP. The support list of the MIPI IO type is shown in Table 2-14.

For information on IO type selection and off-chip termination, please refer to “4 Functional Description” in IPUG948, Gowin MIPI D-PHY RX TX Advance User Guide.

Table 2-14 List of GW1NZ series of FPGA Products that Support MIPI IO Type

MIPI Input/Output	GW1NZ-2
MIPI Input	Bank2
MIPI Output	Bank0/3/4/5

The key features of the soft MIPI D-PHY RX/TX include:

- MIPI Alliance Standard for D-PHY Specification, Version 1.2
- High Speed RX and TX at up to 4.8Gbps
- Supports up to 4 data lanes and 1 clock lane
- Supports multiple PHYs(if there are enough IOs available)
- Supports bidirectional low-power (LP) mode
- Supports MIPI DSI and MIPI CSI-2 link layers
- Supports built-in HS Sync, bit and lane alignment
- Supports MIPI D-PHY RX 1:8 and 1:16 deserialization modes
- Supports IO Types of ELVDS, TLVDS, MIPI IO, etc.

For more information, see IPUG948, Gowin MIPI D-PHY RX TX Advance IP User Guide.

2.10 Clocks

The clock resources and wiring are critical for high-performance applications in FPGA. The GW1NZ series of FPGA products provide global clocks (GCLKs) which connect to all the registers directly. In addition, high-speed clocks (HCLKs), PLLs, etc. are provided.

For more information on the GCLKs, HCLKs, PLLs, see UG286, Gowin Clock User Guide.

2.10.1 Global Clocks

The Global Clock(GCLK) resources are distributed across multiple quadrants within the device. Each quadrant provides eight GCLKs. The clock sources of GCLKs include dedicated clock input pins and CRUs, and better clock performance can be achieved by using the dedicated clock input pins.

2.10.2 PLLs

The PLL (Phase-locked Loop) is a feedback control circuit. The frequency and phase of the internal oscillator signal are controlled by the external input reference clock.

PLLs in the GW1NZ series of FPGA products can provide synthesizable clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be achieved by configuring the parameters.

2.10.3 High-speed Clocks

The high-speed clocks (HCLKs) are designed to facilitate high-performance I/O data transmission and are specifically tailored for source synchronous data transmission protocols, see Figure 2-16 and Figure 2-17. HCLKs can be used for the whole I/O Bank.

Figure 2-16 GW1NZ-1 HCLK Distribution

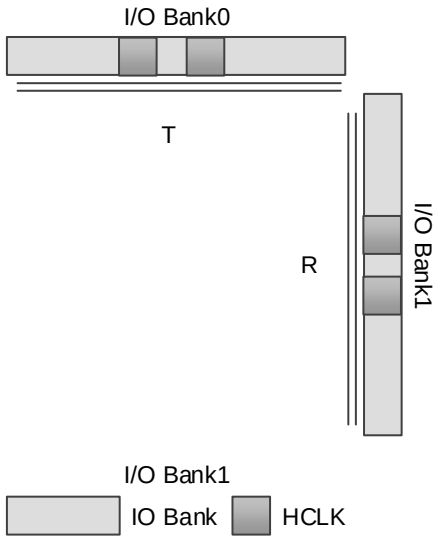
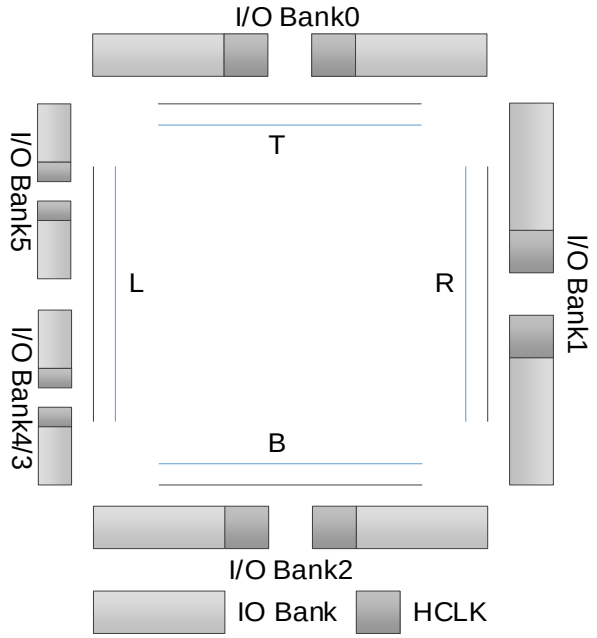


Figure 2-17 GW1NZ-2 HCLK Distribution



2.11 Long Wires

As a supplement to the CRU, the GW1NZ series of FPGA products provide another kind of routing resource - the long wire, which can be used for clock, clock enable, set/reset, or other high fan-out signals.

2.12 Global Set/Reset

The GW1NZ series of FPGA products offer a dedicated global set/reset (GSR) network that connects directly to the device's internal logic and can be used as asynchronous/synchronous set or asynchronous/synchronous reset, with the registers in the CFUs and I/Os being able to be configured independently.

2.13 Programming & Configuration

The GW1NZ series of FPGA products support SRAM configuration and Flash programming. Flash programming includes on-chip Flash programming and off-chip Flash programming. The GW1NZ series of FPGA products(Automotive) support DUAL BOOT, allowing you to back up data to the off-chip Flash as needed.

In addition to JTAG[1], the GW1NZ series of FPGA products also support Gowin's own GowinCONFIG configuration modes: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU. For more information, please refer to *UG290, Gowin FPGA Products Programming and Configuration User Guide*.

Note!

[1] The GW1NZ-1 device in the CG25/FN24 packages does not support JTAG configuration mode.

2.13.1 SRAM Configuration

If SRAM configuration is used, the configuration data needs to be re-downloaded after each power-up.

2.13.2 Flash Programming

The Flash programming data is stored in the on-chip Flash. Each time the device is powered up, the configuration data is transferred from the Flash to the SRAM. Configuration can be completed within a few milliseconds after power-up, which is also known as "instant on".

The GW1NZ series of FPGA products support the feature of background upgrade. That is to say, you can program the on-chip Flash or off-chip Flash via the JTAG[1] interface without affecting the current working state. During programming, the device works according to the previous configuration. After the programming is done, power cycle the FPGA or trigger RECONFIG_N with a low level to complete the upgrade. This feature is suitable for the applications requiring long online time and irregular upgrades.

Note!

[1] Currently, the goConfig IP is required to achieve the background upgrade of GW1NZ-1 in the CG25/FN24 packages. Step 1: configure the goConfig IP into SRAM via serial mode (mode[2:0]=101); Step 2: use the goConfig IP to program the on-chip Flash (reset mode[2:0] to "000" after the programming is completed).

In addition, the GW1NZ series of FPGA products support off-chip Flash programming and DUAL BOOT. For more information, please refer to *UG290, Gowin FPGA Products Programming and Configuration User Guide*.

2.14 On-chip Oscillator

The GW1NZ series of FPGA products have an embedded programmable on-chip clock oscillator which provides a clock source for the MSPI configuration mode with a tolerance of ±5%. See Table 2-15 for the output frequencies.

Table 2-15 Output Frequency Options of the On-chip Oscillator

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.5MHz[1]	8	7.8MHz	16	15.6MHz
1	5.4MHz	9	8.3MHz	17	17.9MHz
2	5.7MHz	10	8.9MHz	18	21MHz
3	6.0MHz	11	9.6MHz	19	25MHz
4	6.3MHz	12	10.4MHz	20	31.3MHz
5	6.6MHz	13	11.4MHz	21	41.7MHz
6	6.9MHz	14	12.5MHz	22	62.5MHz
7	7.4MHz	15	13.9MHz	23	125MHz[2]

Note!

- [1] The default frequency is 2.5MHz.

- [2] 125MHz is not available for the MSPI configuration mode.

The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. The following formula is used to get the output clock frequency:

f_{out}=250MHz /Param。

“Param” should be even numbers from 2 to 128.

3 DC and Switching Characteristics

3.1 Operating Conditions

3.1.1 Absolute Max. Ratings

Table 3-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V_{CC}	Core voltage	-0.5V	1.32V
V_{CCIO}	I/O Bank voltage	-0.5V	3.75V
V_{CCX}	Auxiliary voltage	-0.5V	3.75V
V_{CCD}	Hard MIPI D-PHY core voltage(GW1NZ-2)	-0.5V	1.32V
V_{CCIOD}	Hard MIPI D-PHY I/O voltage(GW1NZ-2)	-0.5V	1.32V
-	I/O voltage applied[1]	-0.5V	3.75V
Storage Temperature	Storage temperature	-65℃	+150℃
Junction Temperature	Junction temperature	-40℃	+125℃

Note!

- [1] Overshoot and undershoot of -2V to (V_{IHMAX} + 2)V are allowed for a duration of <20 ns.

3.1.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions[1]

Name	Description	Min.	Max.
V_{CC}[3]	Core voltage(LV version)	1.07V	1.26V
	Core voltage(ZV version)	0.88V	1.05V
V_{CCIO}[3]	I/O Bank voltage	1.14V	3.6V
V_{CCX}[3]	Auxiliary voltage	1.71V	3.6V[2]
V_{CCD}[4]	Hard MIPI D-PHY core voltage(GW1NZ-2)	1.14V	1.26V
V_{CCIOD}[4]	Hard MIPI D-PHY I/O voltage(GW1NZ-2)	1.14V	1.26V
T_{JCOM}	Junction temperature for commercial operations	0℃	+85℃
T_{JIND}	Junction temperature for industrial operations	-40℃	+100℃

Note!

- [1] For more information on the power supplies, please refer to *UG842, GW1NZ-1 Pinout* and *UG847, GW1NZ-2 Pinout* .
- [2] The low power mode of GW1NZ-2 requires V_{CCX}≤2.5V.
- [3] The allowable ripples on V_{CC}, V_{CCIO}, and V_{CCX} are 3%, 5%, and 5% respectively. 1). For devices of which the PLL is powered directly with V_{CC}, the ripple on V_{CC} can affect the jitter characteristics of the PLL output clock; 2). The ripple on V_{CCIO} can eventually be passed on to the output waveform of the IO Buffer.
- [4]If the hard MIPI D-PHY is not used, you can leave the V_{CCD} and V_{CCIOD} pins floating, or connect them to a 1.2V supply.

3.1.3 Power Supply Ramp Rates

Table 3-3 Power Supply Ramp Rates

Name	Description	Min.	Typ.	Max.
V_{CC} Ramp	Power supply ramp rates for V_{CC}	0.6mV/μs	-	6mV/μs
V_{CCX} Ramp	Power supply ramp rates for V_{CCX}	0.6mV/μs	-	10mV/us
V_{CCIO} Ramp	Power supply ramp rates for V_{CCIO}	0.1mV/μs	-	10mV/us

Note!

- A monotonic ramp is required for all power supplies.
- All power supplies need to be in the operating range as defined in Table 3-2 before configuration. Power supplies that are not in the operating range need to be adjusted to a faster ramp rate, or you have to delay configuration.

3.1.4 Hot Socketing Specifications

Table 3-4 Hot Socketing Specifications

Name	Description	Condition	I/O Type	Max.
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}$(MAX)	I/O	150uA
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}$(MAX)	TDI,TDO, TMS,TCK	120uA

3.1.5 POR Specifications

Table 3-5 POR Parameters

Name	Description	Device	Name	Value
V_{POR_UP}	Power on reset ramp up trip point	GW1NZ-1	V_{CC}	0.8V
			V_{CCX}	1.5V
			V_{CCIO}	0.9V
V_{POR_DOWN}	Power on reset ramp down trip point		V_{CC}	0.65V
			V_{CCX}	1.4V
			V_{CCIO}	0.7V
V_{POR_UP}	Power on reset ramp up trip point	GW1NZ-2	V_{CC}	0.8V
			V_{CCX}	1.5V
			V_{CCIO}	0.95V
V_{POR_DOWN}	Power on reset ramp down trip point		V_{CC}	0.65V
			V_{CCX}	1.3V
			V_{CCIO}	0.75V

3.2 ESD performance

Table 3-6 GW1NZ ESD - HBM

Device	GW1NZ-1	GW1NZ-2
CG25	HBM>1,000V	-
CG56	-	HBM>1,000V
CS100H	-	HBM>1,000V
CS16	HBM>1,000V	-
CS42	-	HBM>1,000V
FN24	HBM>1,000V	-
FN32	HBM>1,000V	-
FN32F	HBM>1,000V	-
QN48	HBM>1,000V	HBM>1,000V

Table 3-7 GW1NZ ESD - CDM

Device	GW1NZ-1	GW1NZ-2
CG25	CDM>500V	-
CG56	-	CDM>500V
CS100H	-	CDM>500V
CS16	CDM>500V	-
CS42	-	CDM>500V
FN24	CDM>500V	-
FN32	CDM>500V	-
FN32F	CDM>500V	-
QN48	CDM>500V	CDM>500V

3.3 DC Electrical Characteristics

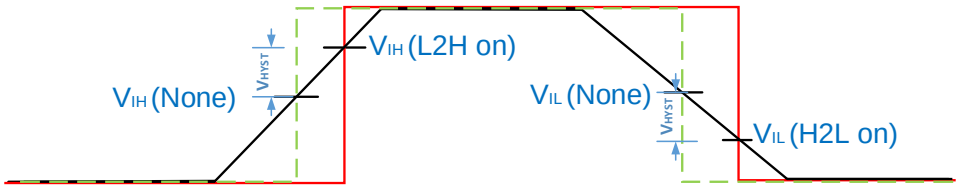
3.3.1 DC Electrical Characteristics over Recommended Operating Conditions

Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
IIL,IIH	Input or I/O leakage current	$V_{CCIO}<V_{IN}<V_{IH}$(MAX)	-	-	210μA
		$0<V_{IN}<V_{CCIO}$	-	-	10μA
IPU	I/O Active Pull-up Current	$0<V_{IN}<0.7V_{CCIO}$	-30μA	-	-150μA
IPD	I/O Active Pull-down Current	V_{IL}(MAX)$<V_{IN}<V_{CCIO}$	30μA	-	150μA
IBHLS	Bus Hold Low Sustaining Current	$V_{IN}=V_{IL}$(MAX)	30μA	-	-
IBHHS	Bus Hold High Sustaining Current	$V_{IN}=0.7V_{CCIO}$	-30μA	-	-
IBHLO	Bus Hold Low Overdrive Current	$0\leqslant V_{IN}\leqslant V_{CCIO}$	-	-	150μA
IBHHO	Bus Hold High Overdrive Current	$0\leqslant V_{IN}\leqslant V_{CCIO}$	-	-	-150μA
VBHT	Bus Hold Trip Points		VIL(MAX)	-	VIH(MIN)
C1	I/O Capacitance			5pF	8pF
VHYST	Hysteresis for Schmitt Trigger inputs	V_{CCIO}=3.3V, Hysteresis=L2H[1],[2]	-	200mV	-
		V_{CCIO}=2.5V, Hysteresis= L2H	-	125mV	-
		V_{CCIO}=1.8V, Hysteresis= L2H	-	60mV	-
		V_{CCIO}=1.5V, Hysteresis= L2H	-	40mV	-
		V_{CCIO}=1.2V, Hysteresis= L2H	-	20mV	-
		V_{CCIO}=3.3V, Hysteresis= H2L[1],[2]	-	200mV	-
		V_{CCIO}=2.5V, Hysteresis= H2L	-	125mV	-
		V_{CCIO}=1.8V, Hysteresis= H2L	-	60mV	-
		V_{CCIO}=1.5V, Hysteresis= H2L	-	40mV	-
		V_{CCIO}=1.2V, Hysteresis= H2L	-	20mV	-
		V_{CCIO}=3.3V, Hysteresis= HIGH[1],[2]	-	400mV	-
		V_{CCIO}=2.5V, Hysteresis= HIGH	-	250mV	-
		V_{CCIO}=1.8V, Hysteresis= HIGH	-	120mV	-
		V_{CCIO}=1.5V, Hysteresis= HIGH	-	80mV	-
		V_{CCIO}=1.2V, Hysteresis= HIGH	-	40mV	-

Note!

- [1] Hysteresis="NONE", "L2H", "H2L", "HIGH" indicates the Hysteresis options that can be set when setting I/O Constraints in the FloorPlanner tool of Gowin EDA, for more details, see *SUG935, Gowin Design Physical Constraints User Guide*.
- [2] Enabling the L2H (low to high) option means raising V_{IH} by V_{HYST}; enabling the H2L (high to low) option means lowering V_{IL} by V_{HYST}; enabling the HIGH option means enabling both L2H and H2L options, i.e. V_{HYST}(HIGH) = V_{HYST}(L2H) + V_{HYST}(H2L). The diagram is shown below.



3.3.2 Static Current

Table 3-9 Static Current(LV Version)

Name	Description	Device	Typ.
I_{CC}	V_{CC} current (V_{CC}=1.2V)	GW1NZ-1	3mA
I_{CCX}	V_{CCX} current (V_{CCX}=3.3V)	GW1NZ-1	0.5mA
	V_{CCX} current (V_{CCX}=2.5V)	GW1NZ-1	0.5mA
I_{CCIO}	V_{CCIO} current (V_{CCIO}=2.5V)	GW1NZ-1	0.5mA

Table 3-10 Static Current (GW1NZ-1, ZV version)

Name	Description	Device	Typ.
I_{CC}	V_{CC} current (V_{CC}=0.9V)	GW1NZ-ZV1FN32C5/I4 GW1NZ-ZV1CS16C5/I4	50uA
		GW1NZ-ZV1FN32I3 GW1NZ-ZV1CS16I3	40uA
		GW1NZ-ZV1FN32I2 GW1NZ-ZV1CS16I2	30uA
I_{CCX}	V_{CCX} current (V_{CCX} floating)	GW1NZ-ZV1FN32C5/I4 GW1NZ-ZV1CS16C5/I4	0uA
		GW1NZ-ZV1FN32I3 GW1NZ-ZV1CS16I3	0uA
		GW1NZ-ZV1FN32I2 GW1NZ-ZV1CS16I2	0uA
	V_{CCX} current (V_{CCX}=1.8V-3.3V)	GW1NZ-ZV1FN32C5/I4 GW1NZ-ZV1CS16C5/I4	1uA
		GW1NZ-ZV1FN32I3 GW1NZ-ZV1CS16I3	1uA
		GW1NZ-ZV1FN32I2 GW1NZ-ZV1CS16I2	1uA
I_{CCIO}	V_{CCIO} current (V_{CCIO}=3.3V)	GW1NZ-ZV1FN32C5/I4 GW1NZ-ZV1CS16C5/I4	0uA
		GW1NZ-ZV1FN32I3 GW1NZ-ZV1CS16I3	0uA
		GW1NZ-ZV1FN32I2 GW1NZ-ZV1CS16I2	0uA

Note!

- After the device wakes up, you can turn off the external V_{CCX} without affecting the normal operation of the device when you are not using the User Flash.

- The typical values in the table above are tested at room temperature.
- In zero power circumstances, if you use the MODE pin, the PULL_MODE of this pin must be configured as KEEPER.

Table 3-11 Static Current (GW1NZ-2, ZV version)[1],[3],[4]

Name	Description	Typ.
I_{CC}	V_{CC} current (V_{CC}=1.1V)	600uA
	V_{CC} current (V_{CC}=1.0V)	240uA
	V_{CC} current (V_{CC}=0.9V)	120uA
I_{CCX}	V_{CCX} current (V_{CCX}=1.8V)	150uA
I_{CCIO}	V_{CCIO} current (V_{CCIO}=1.8V)	0uA[2]

Note!

- [1] Test condition: 25℃, BGEN (bandgap enable)=0.
- [2] I_{CCIO} is determined by your external IO circuit and pull-up/down state, and theoretically zero power consumption can be achieved.
- [3] Low power mode requires V_{CCX}≤2.5V.
- [4] You can also choose to turn off V_{CCX}/V_{CCIO} when entering ultra-low power mode, and the data in the device's SRAM will be retained.

3.3.3 Recommended I/O Operating Conditions

Table 3-12 Recommended I/O Operating Conditions

Name	Output V_{CCIO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.6	-	-	-
LVCMOS33	3.135	3.3	3.6	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.6	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.6	1.3	1.5	1
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.6	-	-	-
LVPECL33E	3.135	3.3	3.6	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.6	-	-	-
SSTL33D_II	3.135	3.3	3.6	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

3.3.4 Single-ended I/O DC Characteristics

Table 3-13 Single-ended I/O DC Characteristics

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24[2]	-24[2]
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35*V_{CCIO}	0.65* V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35* V_{CCIO}	0.65* V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35*V_{CCIO}	0.65* V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	4 or 2[3]	-4 or -2[3]
							8 or 6[3]	-8 or -6[3]
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
PCI33	-0.3V	0.3*V_{CCIO}	0.5*V_{CCIO}	3.6V	0.1*V_{CCIO}	0.9*V_{CCIO}	1.5	-0.5
SSTL33_I	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	3.6V	0.7	V_{CCIO}-1.1V	8	-8
SSTL25_I	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	0.54V	V_{CCIO}-0.62V	8	-8
SSTL25_II	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	N/A	N/A	N/A	N/A
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	N/A	N/A	N/A	N/A
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	N/A	N/A	N/A	N/A
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	N/A	N/A	N/A	N/A

Note!

- [1] The total DC current limit(sourced and sunk current) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n*8mA, where n represents the number of IOs bonded out from a bank.
- [2] GW1NZ-2 does not support 24mA.
- [3] GW1NZ-2 supports 2mA/6mA, and GW1NZ-1 supports 4mA/8mA.

3.3.5 Differential I/O DC Characteristics

Table 3-14 Differential I/O DC Characteristics (LVDS)

Name	Description	Test conditions	Min.	Typ.	Max.	Unit
V_{INA},V_{INB}	Input Voltage		0	-	2.15	V
V_{CM}	Input Common Mode Voltage(Input Common Mode Voltage)	Half the Sum of the Two Inputs	0.05	-	2.1	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	±100	-	±600	mV
I_{IN}	Input Current	Power On or Power Off	-	-	±20	μA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100Ω	-	-	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100Ω	0.9	-	-	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T=100Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		-	-	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T=100Ω	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between High and Low		-	-	50	mV
I_S	Short-circuit current	V_{OD} = 0V output short-circuit	-	-	15	mA

3.4 Switching Characteristics

3.4.1 CFU Switching Characteristics

Table 3-15 CFU Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{LUT4_CFU}	LUT4 delay	-	0.674	ns
t_{SR_CFU}	Set/Reset to Register output	-	1.86	ns
t_{CO_CFU}	Clock to Register output	-	0.76	ns

3.4.2 Gearbox Switching Characteristics

Table 3-16 Gearbox Timing Parameters

Device	Name	Description	Max.	Unit
GW1NZ-1[1], [2]	$FMAX_{IDDR}$	1:2 Gearbox	400	Mbps

Device	Name	Description	Max.	Unit
		maximum serial input rate		
	$FMAX_{IDES4}$	1:4 Gearbox maximum serial input rate	800	Mbps
	$FMAX_{IDES7}$	1:7 Gearbox maximum serial input rate	1000	Mbps
	$FMAX_{IDESx}$	1:8/1:10 Gearbox maximum serial input rate	1100	Mbps
	$FMAX_{ODDR}$	2:1 Gearbox maximum serial output rate	400	Mbps
	$FMAX_{OSER4}$	4:1 Gearbox maximum serial output rate	800	Mbps
	$FMAX_{OSER7}$	7:1 Gearbox maximum serial output rate	1000	Mbps
	$FMAX_{OSERx}$	8:1/10:1 Gearbox maximum serial output rate	1100	Mbps
GW1NZ-2[2]	$FMAX_{IDDR}$	1:2 Gearbox maximum serial input rate	400	Mbps
	$FMAX_{IDES4}$	1:4 Gearbox maximum serial input rate	800	Mbps
	$FMAX_{IDES7}$	1:7 Gearbox maximum serial input rate	1000	Mbps
	$FMAX_{IDESx}$	1:8/1:10/1:16 Gearbox maximum serial input rate	1200	Mbps
	$FMAX_{ODDR}$	2:1 Gearbox maximum serial output rate	400	Mbps
	$FMAX_{OSER4}$	4:1 Gearbox maximum serial output rate	800	Mbps
	$FMAX_{OSER7}$	7:1 Gearbox maximum serial output rate	1000	Mbps
	$FMAX_{OSERx}$	8:1/10:1 Gearbox maximum serial output rate	1200	Mbps

Note!

- [1] GW1NZ-1 does not support LVDS input and TLVDS output.
- [2] The LVDS IO speed can be up to 800 Mbps (GW1NZ-1, ELVDS output) and 1 Gbps (GW1NZ-2), but note that for the 1:4 Gearbox and 1:2 Gearbox, the internal core may not be able to reach the corresponding speed.

- Test conditions: Drive Strength=3.5 mA。

3.4.3 Clock and I/O Switching Characteristics

Table 3-17 External Switching Characteristics

Device	Name	C6/I5	C5/I4	Unit
		Typ.	Typ.	
GW1NZ-1	HCLK Tree delay	1.2	1.4	ns
	PCLK Tree delay(GCLK0~5)	2.4	2.6	ns
	PCLK Tree delay(GCLK6~7)	2.7	2.9	ns
	Pin-LUT-Pin Delay	4.3	4.6	ns
GW1NZ-2	HCLK Tree delay	0.8	1.1	ns
	PCLK Tree delay(GCLK0~5)	2.1	2.4	ns
	PCLK Tree delay(GCLK6~7)	2.5	2.8	ns
	Pin-LUT-Pin Delay	3	3.5	ns

Note!

Test conditions: V_{CC}=1.2V。

3.4.4 BSRAM Switching Characteristics

Table 3-18 BSRAM Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COAD_BSRAM}	Clock to output from read address/data	-	5.10	ns
t_{COOR_BSRAM}	Clock to output from output register	-	0.56	ns

3.4.5 On-chip Oscillator Switching Characteristics

Table 3-19 On-chip Oscillator Parameters

Name	Description	Min.	Typ.	Max.
f_{MAX}	Output Frequency (0 to +85℃)	106.25MHz	125MHz	143.75MHz
	Output Frequency (-40 to +100℃)	100MHz	125MHz	150MHz
t_{DT}	Output Clock Duty Cycle	43%	50%	57%
t_{OPJIT}	Output Clock Period Jitter	0.01UIPP	0.012UIPP	0.02UIPP

3.4.6 PLL Switching Characteristics

Table 3-20 PLL Parameters

Device	Version	Speed Grade	Name	Min.	Max.
GW1NZ-1	LV version	C6/I5	CLKIN	3MHz	400MHz
			PFD	3MHz	400MHz
			VCO	400MHz	800MHz
			CLKOUT	3.125MHz	400MHz
		C5/I4	CLKIN	3MHz	320MHz
			PFD	3MHz	320MHz
			VCO	320MHz	640MHz
			CLKOUT	2.5MHz	360MHz
	ZV version	C5/I4	CLKIN	3MHz	200MHz
			PFD	3MHz	200MHz
			VCO	200MHz	400MHz
			CLKOUT	1.5625MHz	200MHz
		I3	CLKIN	3MHz	150MHz
			PFD	3MHz	150MHz
			VCO	150MHz	300MHz
			CLKOUT	1.171875MHz	150MHz
		I2	CLKIN	3MHz	100MHz
			PFD	3MHz	100MHz
			VCO	100MHz	200MHz
			CLKOUT	0.78125MHz	100MHz
GW1NZ-2	ZV version	I3	CLKIN	TBD	TBD
			PFD	TBD	TBD
			VCO	TBD	TBD
			CLKOUT	TBD	TBD
		I2	CLKIN	TBD	TBD
			PFD	TBD	TBD
			VCO	TBD	TBD
			CLKOUT	TBD	TBD

3.5 User Flash Characteristics

3.5.1 DC Electrical Characteristics

Table 3-21 GW1NZ-1 User Flash DC Characteristics[1]

Name	Para meter	Max.		Unit	Wake-up time	Condition
		V_{CC}[4]	V_{CCX}			
Read mode(w/I 25ns)	I_{CC1}[2]	2.19	0.5	mA	N/A	Minimum clock period, 100% duty cycle , VIN = “1/0”
Write mode		0.1	12	mA	N/A	–
Erase mode		0.1	12	mA	N/A	–
Page erase mode		0.1	12	mA	N/A	–
Static read current (25-50ns)	I_{CC2}	980	25	μA	N/A	XE=YE=SE=“1”, between T=T_{acc} and T=50ns, the I/O current is 0mA. After T=50ns, the internal timer turns off read mode, and the I/O current turns out to be the standby current.
Standby mode	I_{SB}	5.2	20	μA	0	V_{SS}, V_{CCX}, and V_{CC}
Power down mode[3]	I_{PD}	0	0	μA	7us	V_{CCX}=0
Typical (25℃)						
Standby mode	I_{SB}	0.4	7.5	μA	0	V_{SS}, V_{CCX}, and V_{CC}
Power down mode[3]	I_{PD}	0	0	μA	3.5us	V_{CCX}=0

Note!

- [1] These values are average DC currents and the peak currents will be higher than these average currents.
- [2] I_{CC1} calculation in different cycle time of T_{new}.
  - T_{new}< T_{acc}: not allowed.
  - T_{new} = T_{acc} : see the table above.
  - T_{acc}<T_{new} - 50ns：I_{CC1} (new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + I_{CC2}
  - T_{new}>50ns：I_{CC1} (new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + 50ns*I_{CC2}/T_{new} + I_{SB}
  - t > 50ns：I_{CC2} = I_{SB}
- [3] Only supported in the low-power mode User Flash.
- [4] V_{CC} must be greater than 1.08V from time zero of the wake-up time.

Table3-22 GW1NZ-2 User Flash DC Characteristics[1], [4]

Name	Parameter	Max.		Unit	Wake-up time	Condition
		V_{CC}[3]	V_{CCX}			
Read mode(w/I 25ns)	I_{CC1}[2]	2.19	0.5	mA	NA	Minimum clock period, 100% duty cycle , VIN = “1/0”
Write mode		0.1	12	mA	NA	–
Erase mode		0.1	12	mA	NA	–
Page erase mode		0.1	12	mA	NA	–
Static read current (25-50ns)	I_{CC2}	980	25	μA	NA	XE=YE=SE=“1”, between T=T_{acc} and T=50ns, the I/O current is 0mA. After T=50ns, the internal timer turns off read mode, and the I/O current turns out to be the standby current.
Standby mode	I_{SB}	5.2	20	μA	0	V_{SS}, V_{CCX}, and V_{CC}

Note!

- [1] These values are average DC currents and the peak currents will be higher than these average currents.
- [2] I_{CC1} calculation in different cycle time of T_{new}.
  - $T_{new} < T_{acc}$: not allowed.
  - $T_{new} = T_{acc}$: see the table above.
  - $T_{acc} < T_{new}$ - 50ns： I_{CC1} (new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + I_{CC2}
  - $T_{new} > 50ns$： I_{CC1} (new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + 50ns*I_{CC2}/T_{new} + I_{SB}
  - t > 50ns： $I_{CC2} = I_{SB}$
- [3] V_{CC} must be greater than 1.08V from time zero of the wake-up time.
- [4] The leakage current of the Flash is included in the leakage current of the device, see Table 3-4.

3.5.2 Timing Parameters

Table 3-23 User Flash Timing Parameters[1], [4], [5]

User Mode	Parameter	Symbol	Min.	Max.	Unit
Access time	WC1	T_{acc}[2]	-	25	ns
	TC		-	22	ns
	BC		-	21	ns
	LT		-	21	ns
	WC		-	25	ns
Program/Erase to data storage setup time		T_{nvs}	5	-	μs
Data storage hold time		T_{nvh}	5	-	μs
Data storage hold time(mass erase)		T_{nvh1}	100	-	μs
Data storage to program setup time		T_{pgs}	10	-	μs
Program hold time		T_{pgh}	20	-	ns
Program time		T_{prog}	8	16	μs
Write prepare time		T_{wpr}	>0	-	ns
Write hold time		T_{whd}	>0	-	ns
Control to program/erase setup time		T_{cps}	-10	-	ns
SE to read control setup time		T_{as}	0.1	-	ns
Positive pulse width of SE		T_{pws}	5	-	ns
Address/data setup time		T_{ads}	20	-	ns
Address/data hold time		T_{adh}	20	-	ns
Data hold time		T_{dh}	0.5	-	ns
Address hold time in read mode	WC1	T_{ah}	25	-	ns
	TC		22	-	ns
	BC		21	-	ns
	LT		21	-	ns
	WC		25	-	ns
Negative pulse width of SE		T_{nws}	2	-	ns
Recovery time		T_{rcv}	10	-	μs
Data storage time		T_{hv}[3]	-	6	ms
Erase time		T_{erase}	100	120	ms
Mass erase time		T_{me}	100	120	ms
Wake-up time of power-down to standby		T_{wk_pd}	7	-	μs
Standby hold time		T_{sbh}	100	-	ns
V_{CC} setup time		T_{ps}	0	-	ns
V_{CCX} hold time		T_{ph}	0	-	ns

Note!

- [1] The values are simulation data and are subject to change.

- [2] After XADR, YADR, XE, and YE are valid, T_{acc} starts at the rising edge of SE. DOUT will be kept before the next valid read operation starts.
- [3] T_{hv} is the cumulative time from the start of the write operation to the next data erase operation. The same address cannot be written twice before the next erase; the same memory cell cannot be written twice before the next erase. This limitation is for security reasons.
- [4] All waveforms have a 1ns rising time and a 1ns falling time.
- [5] Control signals(X, YADR, XE, and YE) need to be held for at least T_{acc}, which starts at the rising edge of SE.

3.5.3 Timing Diagrams

Figure 3-1 Read Mode

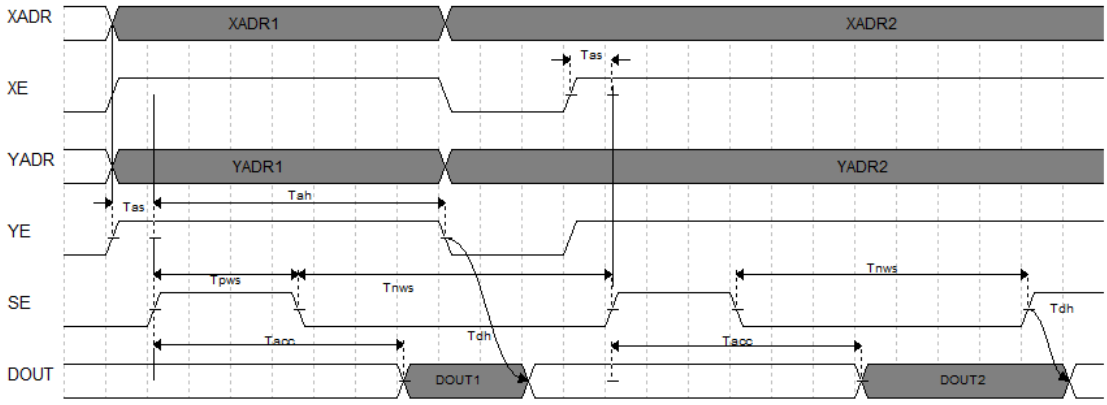


Figure 3-2 Write Mode

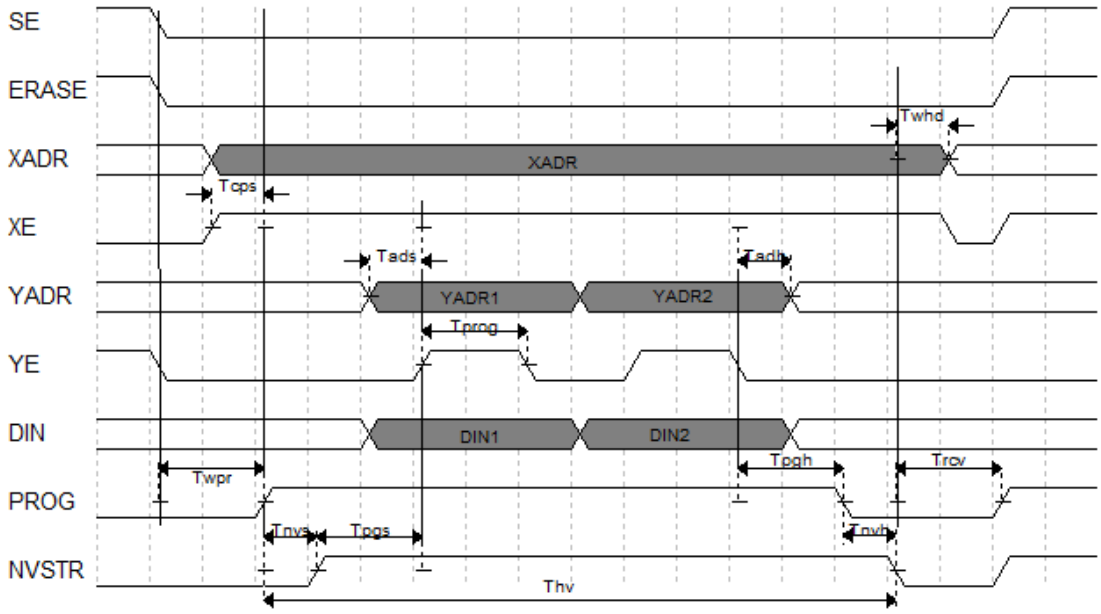
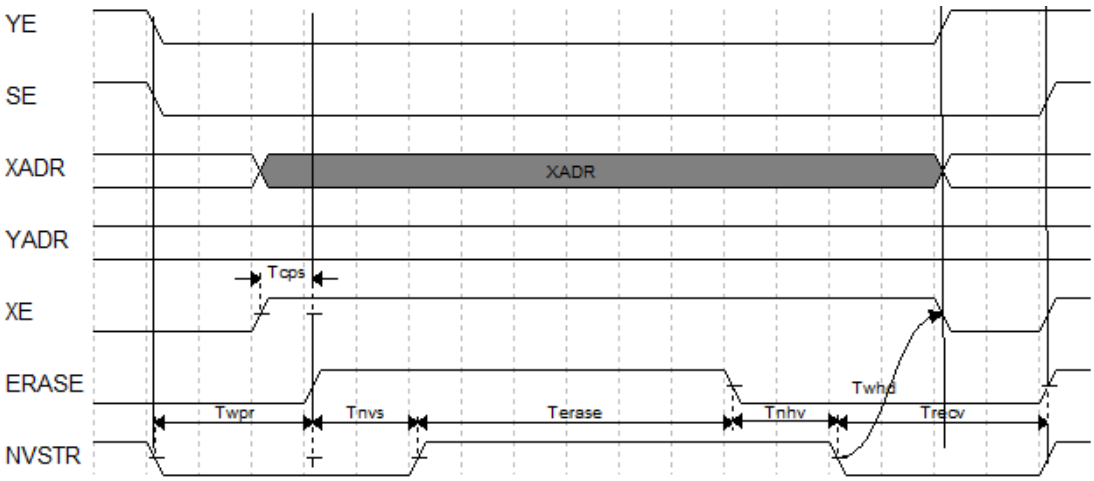


Figure 3-3 Erase Mode



3.6 Configuration Interface Timing Specification

The GW1NZ series of FPGA products support 6 GowinCONFIG modes: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU. For more information, please refer to UG290, Gowin FPGA Products Programming and Configuration User Guide.

4 Ordering Information

4.1 Part Naming

Figure 4-1 Part Naming – ES

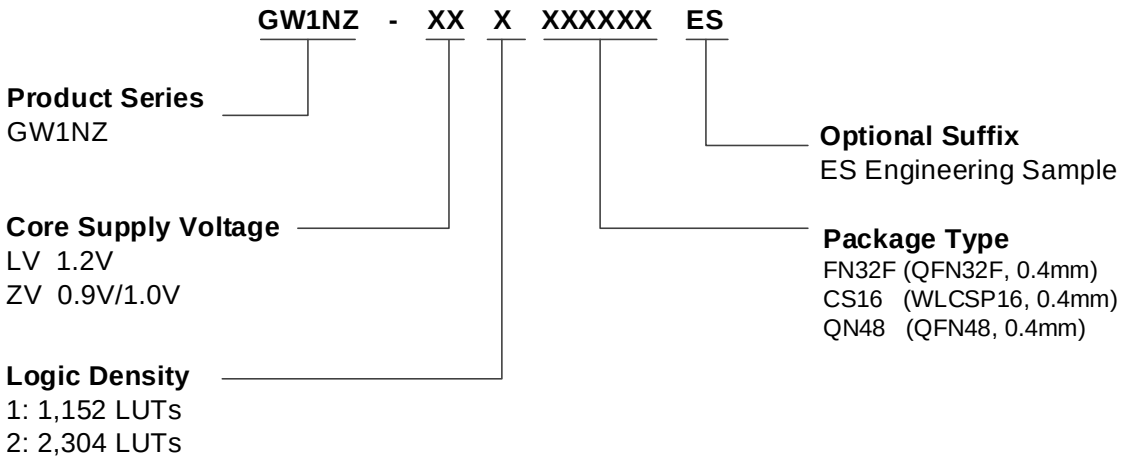


Figure 4-2 Part Naming Examples - Production

Note!

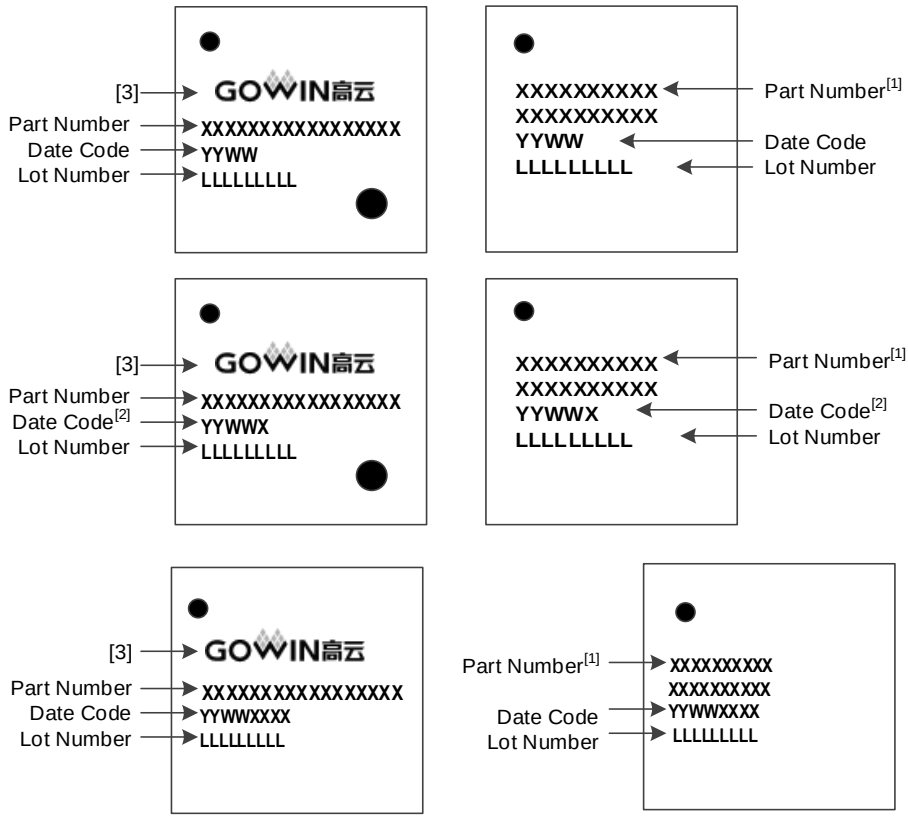
- [1] FN32 is the legacy version.

- For more information about the packages, please refer to 1.2 Product Resources and 1.3 Package Information.
- Both “C” and “I” are used in Gowin’s part name marking for one device. GOWIN devices are screened using industrial standards, so the same device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100℃, and the maximum temperature of the commercial grade is 85℃. Therefore, if the chip meets speed grade 5 in commercial grade applications, its speed grade will be 4 in industrial grade applications.
- The LittleBee family devices and Arora family devices of the same speed grade have different speeds.

4.2 Package Markings

Gowin’s devices have markings on the their surfaces, as shown in Figure 4-3.

Figure 4-3 Package Marking Examples



Note!

- [1] The first two lines in the right figure(s) above are both the “Part Number”.
- [2] The Date Code followed by an “X” is for X version devices.
- [3] Whether the package marking bears the Gowin Logo or not depends on the package type, package size, and Part Number length. The above figure are only examples of the package markings.

5 About This Manual

5.1 Purpose

This data sheet provides a comprehensive overview of the GW1NZ series of FPGA products, including their features, resources, architecture, AC/DC characteristics, and ordering details.

5.2 Related Documents

The latest documents are available at www.gowinsemi.com.

- UG290, Gowin FPGA Products Programming and Configuration User Guide
- UG843, GW1NZ series of FPGA Products Package and Pinout Manual
- UG842, GW1NZ-1 Pinout
- UG847, GW1NZ-2 Pinout

5.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are shown in Table 5-1.

Table 5-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
ALU	Arithmetic Logic Unit
BSRAM	Block Static Random Access Memory
CFU	Configurable Functional Unit
CG25	WLCSP25
CG56	WLCSP56
CLS	Configurable Logic Section
CRU	Configurable Routing Unit
CS16	WLCSP16
DCS	Dynamic Clock Selector
DP	True Dual Port 16K BSRAM
DQCE	Dynamic Quadrant Clock Enable
FN24	QFN24
FN32	QFN32
FN32F	QFN32F
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable IO
IOB	Input/output Block
LUT4	4-input Look Up Table
PLL	Phase Locked Loop
QN48	QFN48
REG	Register
SDP	Semi Dual Port 16K BSRAM
SP	Single Port 16K BSRAM
SPMI	System Power Management Interface

5.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail：support@gowinsemi.com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