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NC7SZ86

Single 2-Input Exclusive-OR Gate

www.sot23.com.tw

General Description

This single 2-input exclusive-OR gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The NC7SZ86 performs the Boolean function $Y=A \oplus B$ or $Y=\overline{A}B+A\overline{B}$ in positive logic.

A common application is as a true/complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Features

- **Supports 5V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 4 ns at 3.3 V**
- **Low Power Consumption, 10μA Max I_{CC}**
- **±24mA Output Drive at 3.3V**
- **I_{off} Supports Partial-Power-Down Mode**

Applications

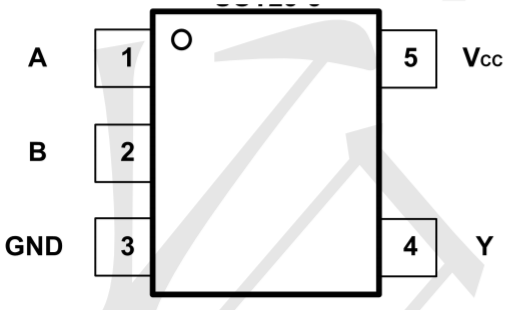
- **Wireless Headsets**
- **Motor Drives and Controls**
- **TVs**
- **Set-Top Boxes**
- **Audio**

Ordering Information

ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION
NC7SZ86M5X	SOT23-5	Tape and Reel,3000
NC7SZ86P5X	SOT353	Tape and Reel,3000

Pin Configuration

SOT23-5/SOT353

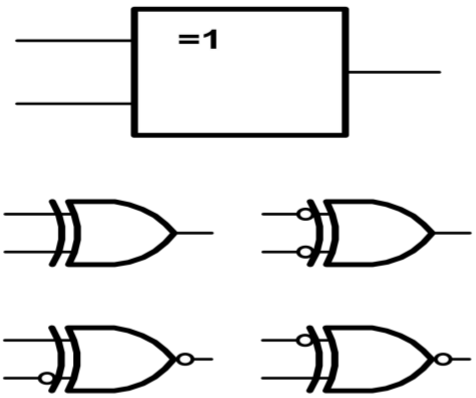


Marking

NC7SZ08M5X Marking:7Z86D

NC7SZ08P5X Marking:Z86C

Logic Diagram



Function Table

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Absolute Maximum Ratings

Parameters			Min	Max.	Unit
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range		-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state		-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_O<0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature under bias			150	˚C
T_{stg}	Storage temperature range		-65	150	˚C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability..

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

ESD Ratings

ESD			VALUE	UNIT
V(ESD)	Electrostatic discharge	Human-body model (HBM)	4K	V
		Charge device model (CDM)	2K	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameters		Min.	Max.	Unit
V_{CC}	Supply Voltage		1.65	5.5	V
V_{IH}	High-level input voltage	V_{CC}=1.65V to1.95V	0.65×V_{CC}		V
		V_{CC}=2.3V to 2.7V	1.7		
		V_{CC}=3V to 3.6V	2		
		V_{CC}=4.5V to 5.5V	0.7×V_{CC}		
V_{IL}	Low-level input voltage	V_{CC}=1.65V to1.95V		0.35×V_{CC}	V
		V_{CC}=2.3V to 2.7V		0.7	
		V_{CC}=3V to 3.6V		0.8	
		V_{CC}=4.5V to 5.5V		0.3×V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC}=1.65V		-4	mA
		V_{CC}=2.3V		-8	
		V_{CC}=3V		-16	
				-24	
		V_{CC}=4.5V		-32	
I_{OL}	Low-level output current	V_{CC}=1.65V		4	mA
		V_{CC}=2.3V		8	
		V_{CC}=3V		16	
				24	
		V_{CC}=4.5V		32	
Δt/Δv	Input transition rise or fall rate	V_{CC}=1.8V±0.15V,2.5V±0.2V		20	ns/V
		V_{CC}=3.3V±0.3V		10	
		V_{CC}=5V±0.5V		5	
TA	Operating free-air temperature		-40	125	℃

Electrical Characteristics

FULL=–40°C to +125°C, Typical values are at TA = +25°C. (unless otherwise noted)

Parameters	Symbol	Conditions	V_{CC}	T_A	Min.	Typ.	Max.	Unit
High-level output voltage	V_{OH}	I_{OH} = –100μA	1.65V to 5.5V	FULL	V_{CC}-0.1			V
		I_{OH} = –4mA	1.65		1.2			
		I_{OH} = –8mA	2.3		1.9			
		I_{OH} = –16mA	3		2.4			
		I_{OH} = –24mA			2.3			
		I_{OH} = –32mA	4.5		3.8			
Low-level output voltage	V_{OL}	I_{OL} = 100μA	1.65V to 5.5V	FULL			0.1	V
		I_{OL} = 4mA	1.65				0.45	
		I_{OL} = 8mA	2.3				0.3	
		I_{OL} = 16mA	3				0.4	
		I_{OL} = 24mA					0.55	
		I_{OL} = 32mA	4.5				0.55	
Input leakage current	I_I	A or B input, VI = 5.5V or GND	0V to 5.5V	FULL			±5	μA
	I_{off}	V_I or V_O = 5.5V	0V	FULL			±10	μA
Supply current	I_{CC}	V_I = 5.5 V or GND, I_O = 0	1.65V to 5.5V	FULL			15	μA
	ΔI_{CC}	one input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND	3V to 5.5V	FULL			500	μA
Input capacitance	C_i	V_I = V_{CC} or GND	3.3V	FULL		6		pF
Power dissipation capacitance	C_{pd}	f = 10 MHz	1.8V	25℃		22		pF
			2.5V			22		
			3.3V			22		
			5V			24		
Propagation delay time	t_{pd}	Any input to Y (output), C_L=15pF	1.8V±0.15V	FULL	2.1		9.1	ns
			2.5V±0.2V		1		4.5	
			3.3V±0.3V		0.6		4	
			5V±0.5V		0.8		3.3	
		Any input to Y (output), C_L=30pF or 50pF	1.8V±0.15V	FULL	3.5		12	
			2.5V±0.2V		1.8		7	
			3.3V±0.3V		1.3		6	
			5V±0.5V		1		5	

Electrical specifications(continued)

Detailed Description

The NC7SZ86 device performs the Boolean function $Y=\bar{A}B+A\bar{B}$ in positive logic. This single 2-input exclusive-OR gate is designed for 1.65V to 5.5V V_{CC} operation.

A common application is as a true and complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

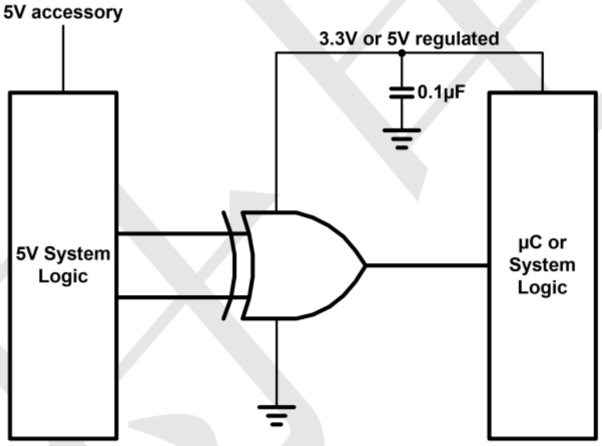
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Function Table

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Application Note

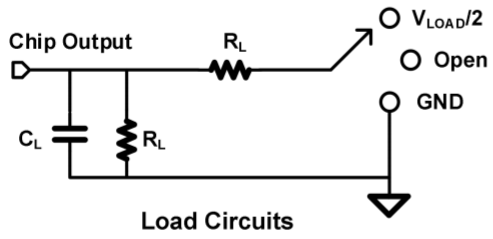
The NC7SZ86 device can accept input voltages up to 5.5 V at any valid V_{CC} which makes the device suitable for down translation. This feature of the NC7SZ86 makes it ideal for various bus interface applications.



Typical Application Schematic

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

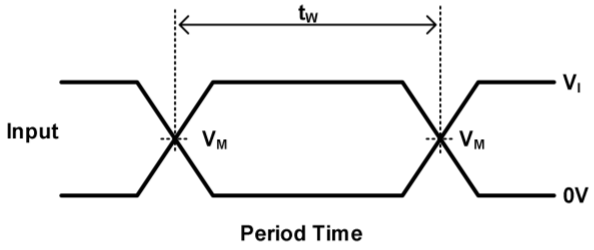
Parameter Measurement Information



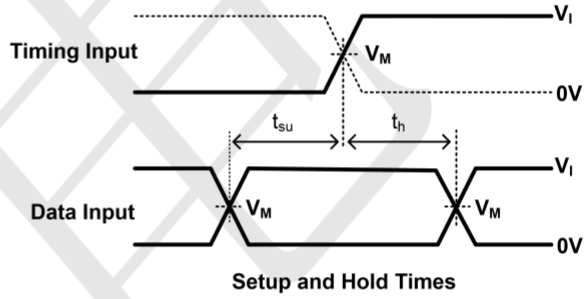
Load Circuits

Test	S1
T_{PHL}/T_{PLH}	OPEN
T_{PLZ}/T_{PZL}	V_{LOAD}
T_{PHZ}/T_{PZH}	GND

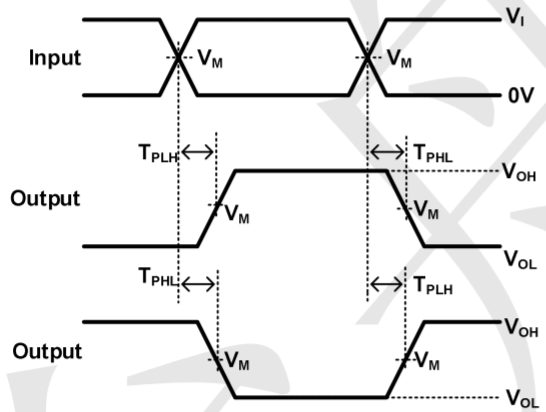
V_{CC}	Inputs		V_M	V_{LAOD}	C_L	R_L	V_Δ
	V_I	T_r/T_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	15pF	1MΩ	0.15V
2.5V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	15pF	1MΩ	0.15V
3.3V±0.15V	3V	≤2.5ns	1.5V	6V	15pF	1MΩ	0.3V
5V±0.15V	V_{CC}	≤2.5ns	$V_{CC}/2$	$2\times V_{CC}$	15pF	1MΩ	0.3V



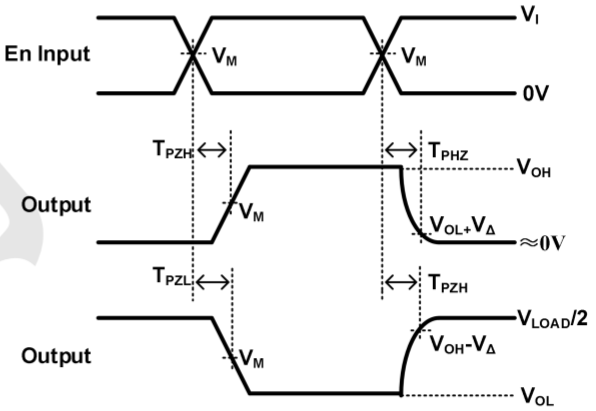
Period Time



Setup and Hold Times



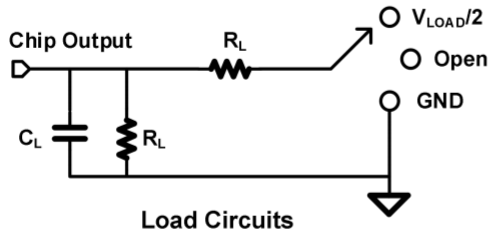
Propagation Delay
for Output and Inverted Output



Enable and Disable Times
Low-And High-Level Enabling

Notes: A. C includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z = 50 .
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .
H. All parameters and waveforms are not applicable to all device.

Parameter Measurement Information(continued)



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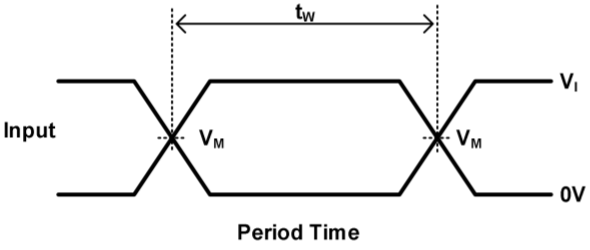
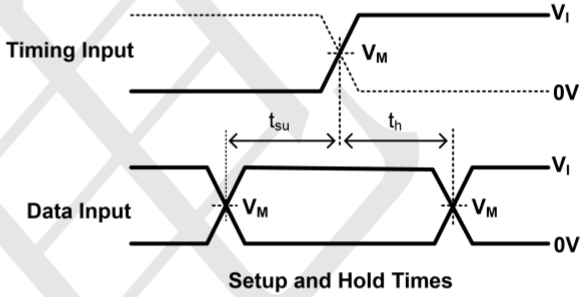
T_{PLZ}/T_{PZL}	V_{LOAD}
T_{PHZ}/T_{PZH}	GND

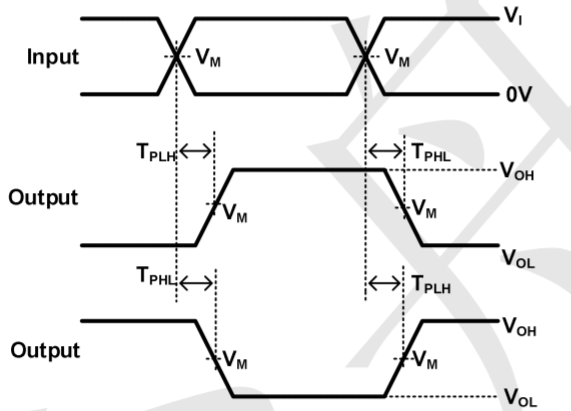
V_{CC}	Inputs		V_M	V_{LAOD}	C_L	R_L	V_Δ
	V_I	T_r/T_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	1kΩ	0.15V
2.5V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	500Ω	0.15V
3.3V±0.15V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.15V	V_{CC}	≤2.5ns	$V_{CC}/2$	$2\times V_{CC}$	50pF	500Ω	0.3V



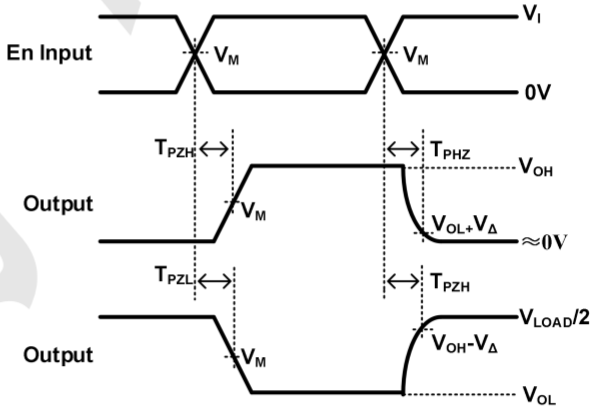
Period Time



Setup and Hold Times



Propagation Delay
for Output and Inverted Output



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Low-And High-Level Enabling

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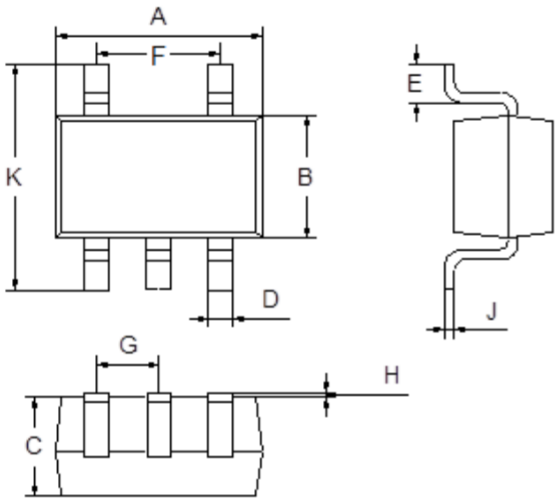
G. t_{PLH} and t_{PHL} are the same as t_{pd} .
H. All parameters and waveforms are not applicable to all device.

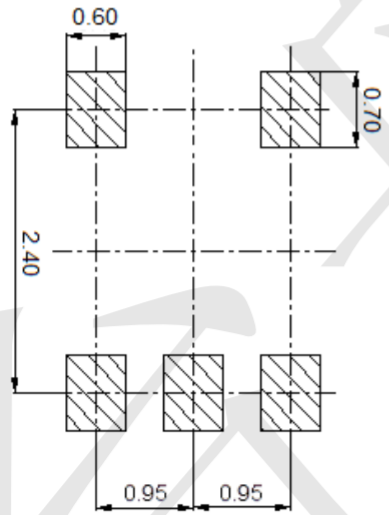
Package Outline Dimensions (Unit: mm)

SOT23-5



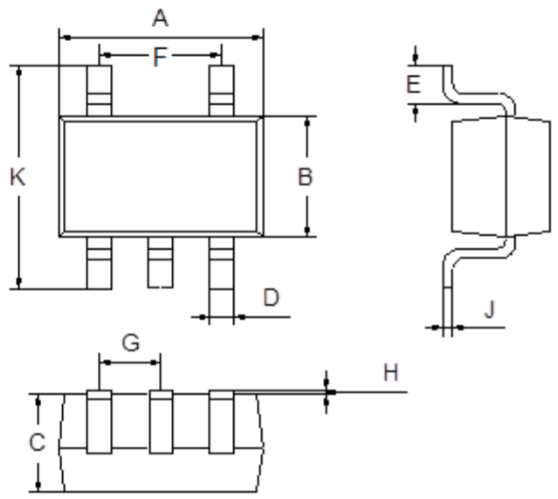
Dimension	Min.	Max.
A	2.80	3.00
B	1.50	1.70
C	1.00	1.20
D	0.35	0.45
E	0.35	0.55
F	1.80	2.00
G	0.90	1.00
H	0.02	0.10
J	0.10	0.20
K	2.60	3.00

Mounting Pad Layout (Unit: mm)



Package Outline Dimensions (Unit: mm)

SOT353



Dimension	Min.	Max.
A	2.00	2.20
B	1.15	1.35
C	0.85	1.05
D	0.15	0.35
E	0.25	0.40
F	1.20	1.40
G	0.60	0.70
H	0.02	0.10
J	0.05	0.15
K	2.20	2.40

Mounting Pad Layout (Unit: mm)