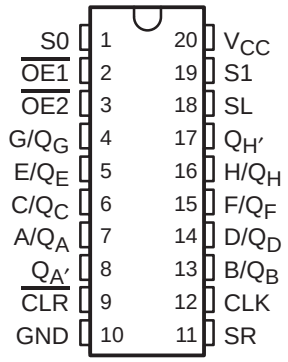
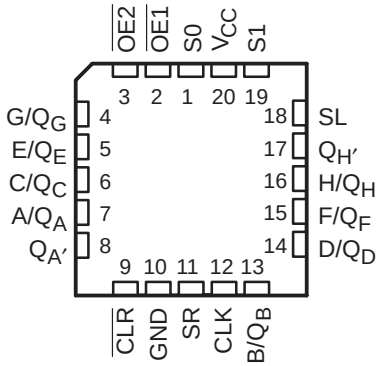
- **Multiplexed I/O Ports Provide Improved Bit Density**
- **Four Modes of Operation:**
  - **Hold (Store)**
  - **Shift Right**
  - **Shift Left**
  - **Load Data**
- **Operate With Outputs Enabled or at High Impedance**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for n-Bit Word Lengths**
- **Direct Overriding Clear**
- **Applications:**
  - **Stacked or Push-Down Registers**
  - **Buffer Storage**
  - **Accumulator Registers**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54ALS299 . . . J PACKAGE
SN74ALS299 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS299 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select (S0, S1) inputs and two output-enable ($\overline{OE1}$, $\overline{OE2}$) inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both S0 and S1 high. This places the 3-state outputs in the high-impedance state and permits data applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when the clear ($\overline{CLR}$) input is low. Taking either $\overline{OE1}$ or $\overline{OE2}$ high disables the outputs, but has no effect on clearing, shifting, or storing data.

The SN54ALS299 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS299 is characterized for operation from 0°C to 70°C.

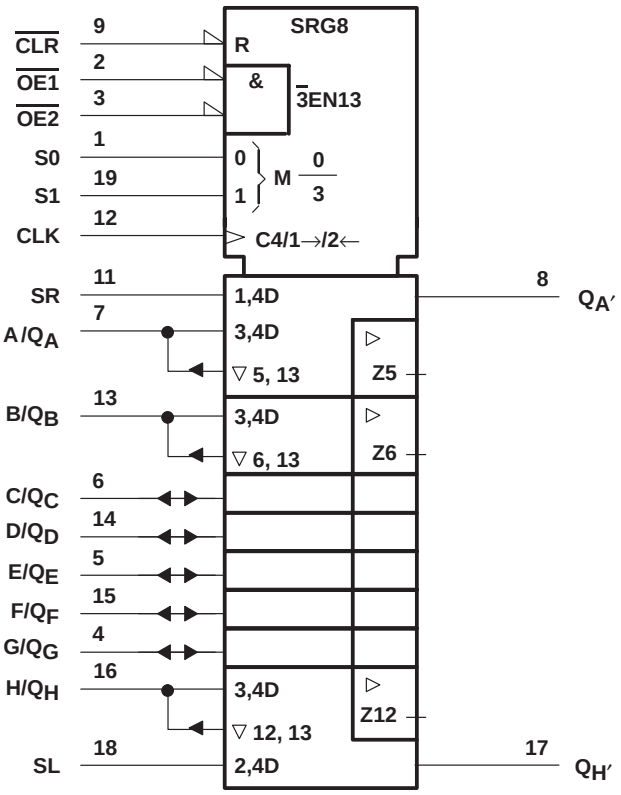
FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	$\overline{CLR}$	S1	S0	$\overline{OE1}$†	$\overline{OE2}$†	CLK	SL	SR	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

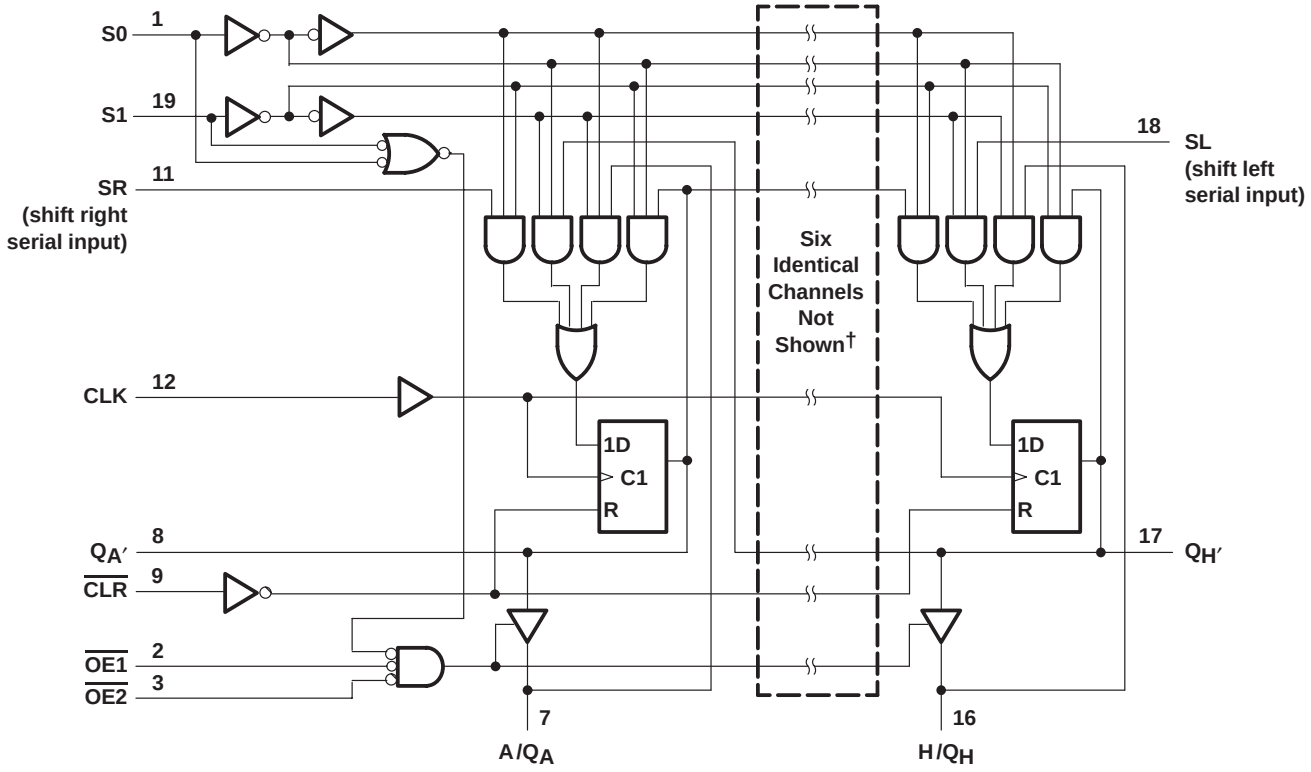
† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



† I/O ports not shown: B/Q_B (13), C/Q_C (6), D/Q_D (14), E/Q_E (5), F/Q_F (15), and G/Q_G (4).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54ALS299 . . . . . −55°C to 125°C
SN74ALS299 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS299			SN74ALS299			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current	$Q_{A'}$ or $Q_{H'}$			–0.4			–0.4	mA
		Q_A – Q_H			–1			–2.6	
I_{OL}	Low-level output current	$Q_{A'}$ or $Q_{H'}$			4			8	mA
		Q_A – Q_H			12			24	
T_A	Operating free-air temperature		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS299			SN74ALS299			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = – 0.4 mA	V_{CC} –2			V_{CC} –2			V
	Q_A – Q_H	V_{CC} = 4.5 V	I_{OH} = – 1 mA	2.4	3.3					
			I_{OH} = – 2.6 mA				2.4	3.2		
V_{OL}	$Q_{A'}$ or $Q_{H'}$	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
	Q_A – Q_H	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
			I_{OL} = 24 mA					0.35	0.5	
I_I	A – H	V_{CC} = 5.5 V	V_I = 5.5 V			0.1			0.1	mA
	Any others		V_I = 7 V			0.1			0.1	
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}‡	S0, S1, SR, SL	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2			–0.2	mA
	Any others					–0.1			–0.1	
I_O§	$Q_{A'}$ or $Q_{H'}$	V_{CC} = 5.5 V,	V_O = 2.25 V	–15		–70	–15		–70	mA
	Q_A – Q_H			–20		–112	–30		–112	
I_{CC}		V_{CC} = 5.5 V	Outputs high		15	28		15	28	mA
			Outputs low		22	38		22	38	
			Outputs disabled		23	40		23	40	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports (Q_A–Q_H), the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				SN54ALS299		SN74ALS299		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency (at 50% duty cycle)			0	17	0	30	MHz
t_w	Pulse duration	CLK high or low		22		16.5		ns
		$\overline{CLR}$ low		12		10		
t_{su}	Setup time before CLK↑	S0 or S1		25		20		ns
		Serial or parallel data	High	18		16		
			Low	15		6		
	Inactive-state setup time before CLK↑†	$\overline{CLR}$		15		15		
t_h	Hold time after CLK↑	S0 or S1		0		0		ns
		Serial or parallel data		0		0		

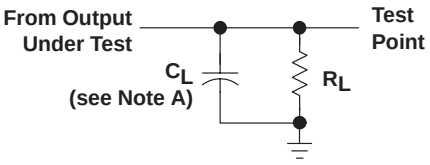
† Inactive-state setup time is also referred to as recovery time.

switching characteristics (see Figure 1)

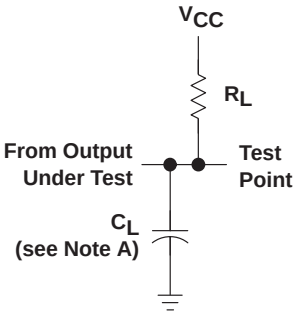
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX‡				UNIT
			SN54ALS299		SN74ALS299		
			MIN	MAX	MIN	MAX	
f_{max}			17		30		MHz
t_{PLH}	CLK	Q_A–Q_H	2	19	4	13	ns
t_{PHL}			4	25	7	19	
t_{PLH}	CLK	$Q_{A'}$ or $Q_{H'}$	2	21	5	15	ns
t_{PHL}			4	25	8	18	
t_{PHL}	$\overline{CLR}$	Q_A–Q_H	6	29	6	22	ns
		$Q_{A'}$ or $Q_{H'}$	6	29	6	22	
t_{PZH}	$\overline{OE1}$, $\overline{OE2}$	Q_A–Q_H	5	22	6	16	ns
t_{PZL}			6	27	8	22	
t_{PZH}	S0, S1	Q_A–Q_H	5	27	7	17	ns
t_{PZL}			6	26	8	22	
t_{PHZ}	$\overline{OE1}$, $\overline{OE2}$	Q_A–Q_H	1	15	1	8	ns
t_{PLZ}			4	38	5	15	
t_{PHZ}	S0, S1	Q_A–Q_H	1	16	1	12	ns
t_{PLZ}			4	34	8	25	

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

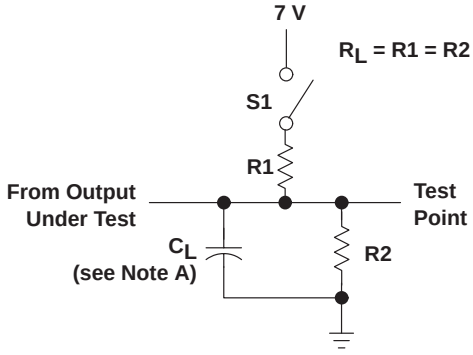
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



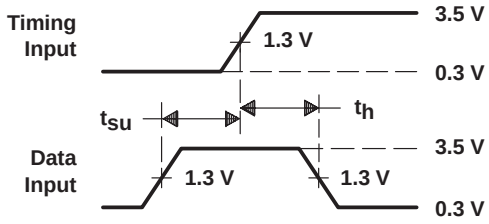
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



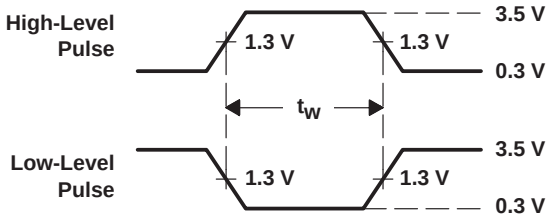
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



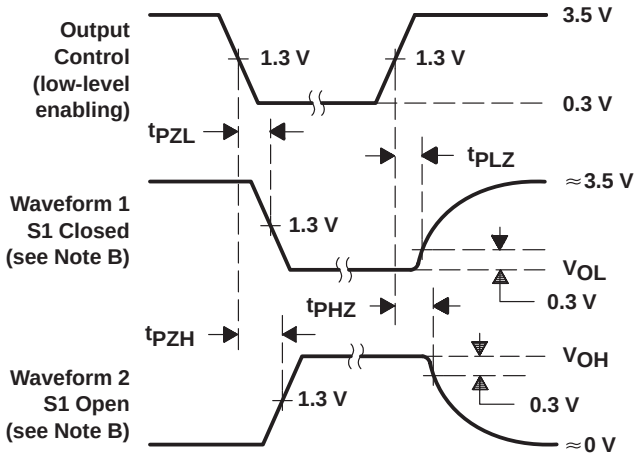
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



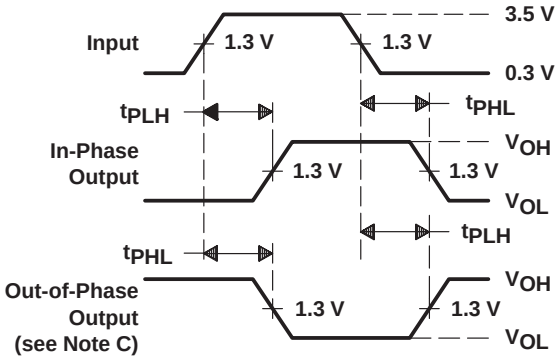
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
83021012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83021012A SNJ54ALS 299FK
8302101RA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101RA SNJ54ALS299J
8302101SA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101SA SNJ54ALS299W
SN74ALS299DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS299
SN74ALS299DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS299
SN74ALS299N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS299N
SN74ALS299N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS299N
SNJ54ALS299FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83021012A SNJ54ALS 299FK
SNJ54ALS299FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83021012A SNJ54ALS 299FK
SNJ54ALS299J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101RA SNJ54ALS299J
SNJ54ALS299J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101RA SNJ54ALS299J
SNJ54ALS299W	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101SA SNJ54ALS299W
SNJ54ALS299W.A	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302101SA SNJ54ALS299W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

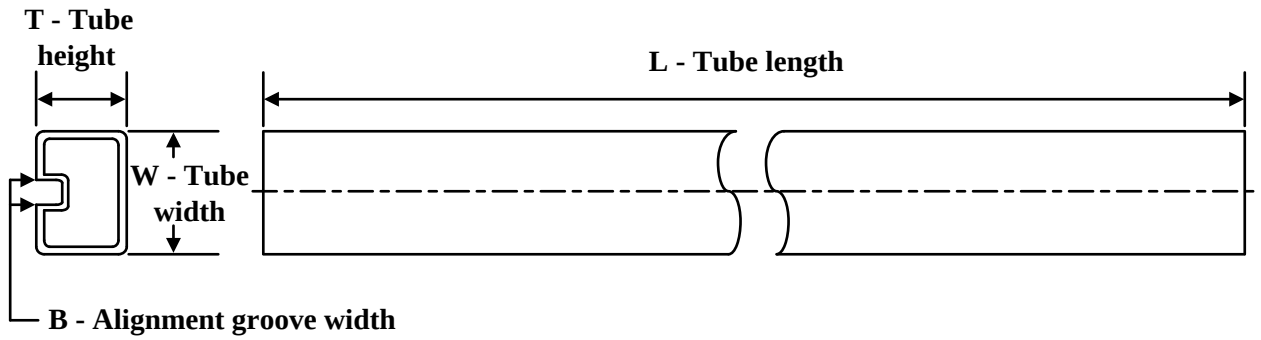
OTHER QUALIFIED VERSIONS OF SN54ALS299, SN74ALS299 :

- Catalog : SN74ALS299
- Military : SN54ALS299

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

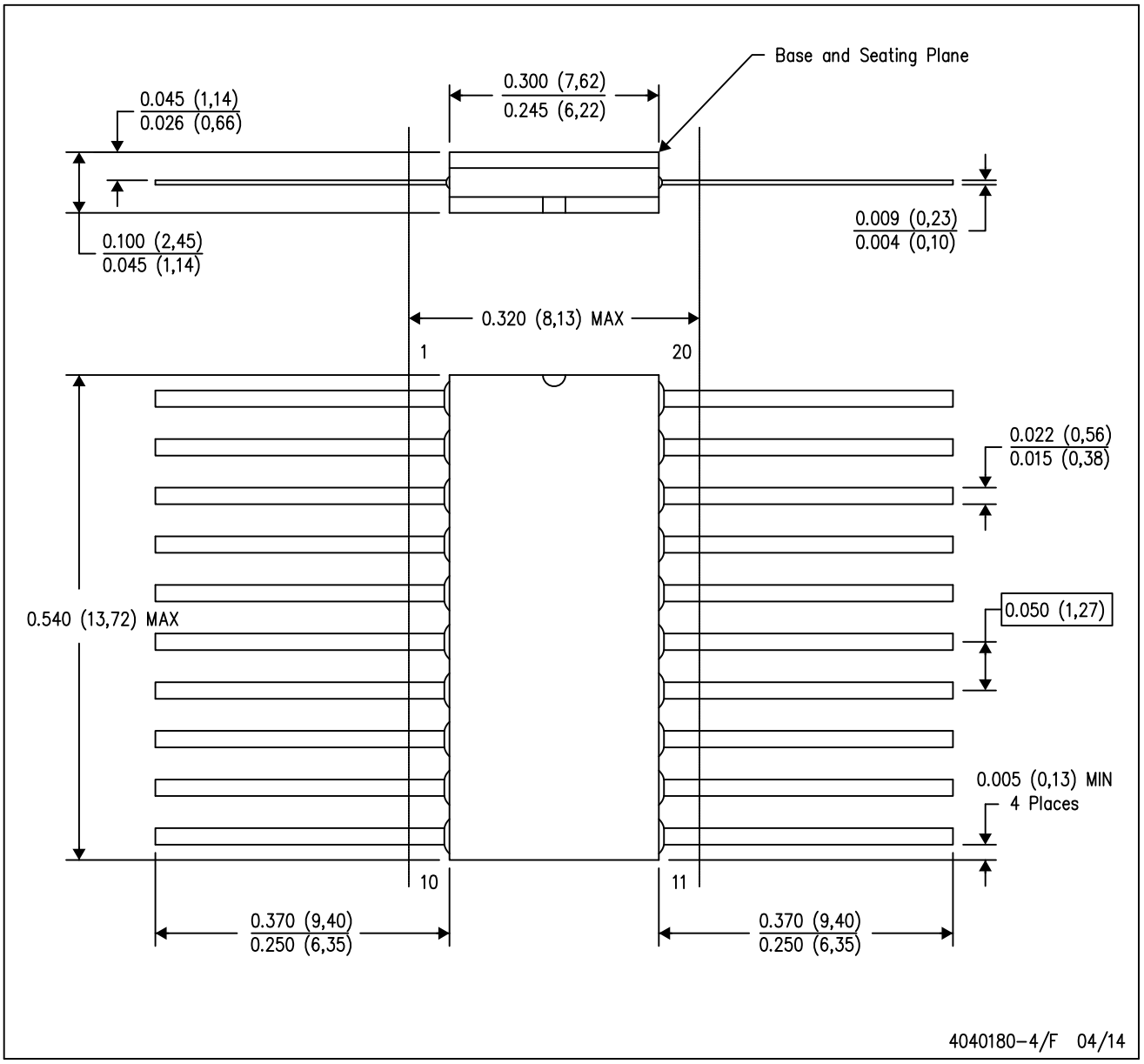
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
83021012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8302101SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74ALS299DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS299DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS299N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS299N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS299FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS299FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS299W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54ALS299W.A	W	CFP	20	25	506.98	26.16	6220	NA

W (R–GDFP–F20) CERAMIC DUAL FLATPACK

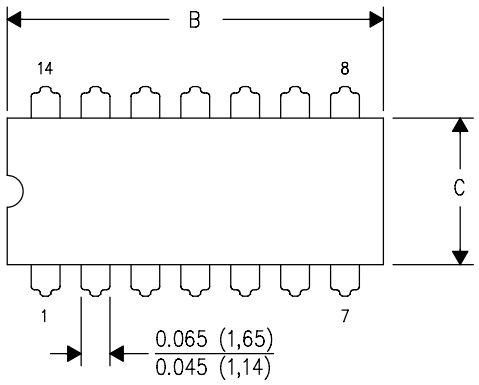


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

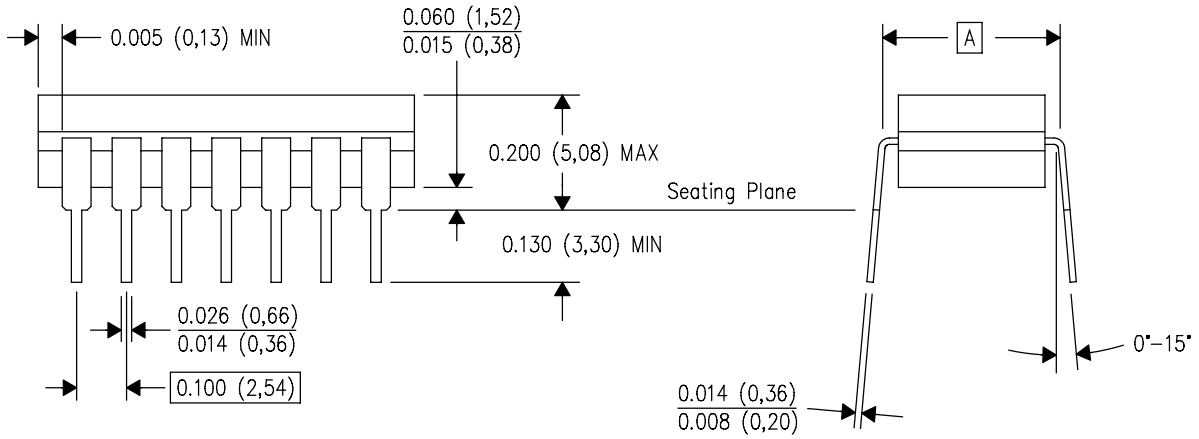
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

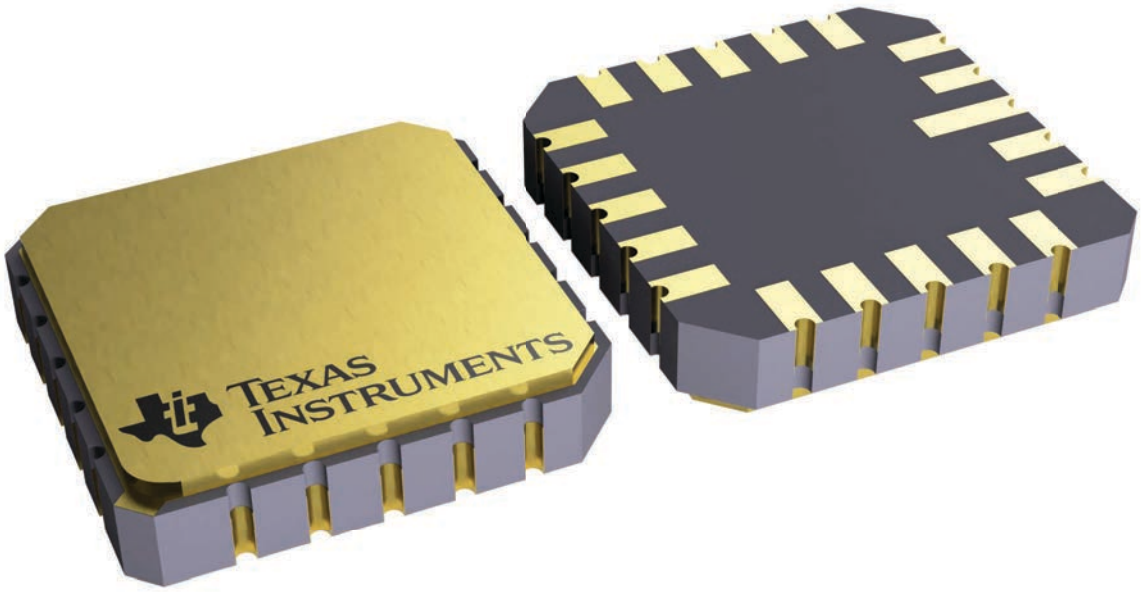
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

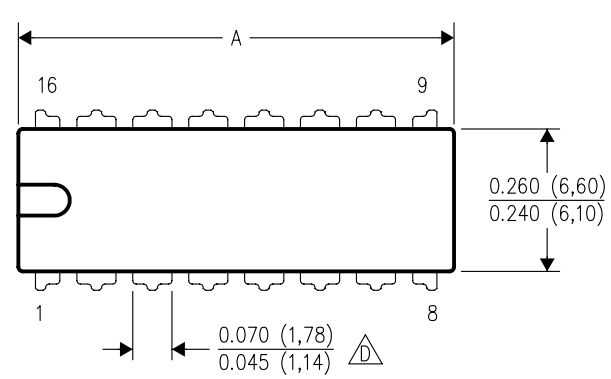


4229370VA\

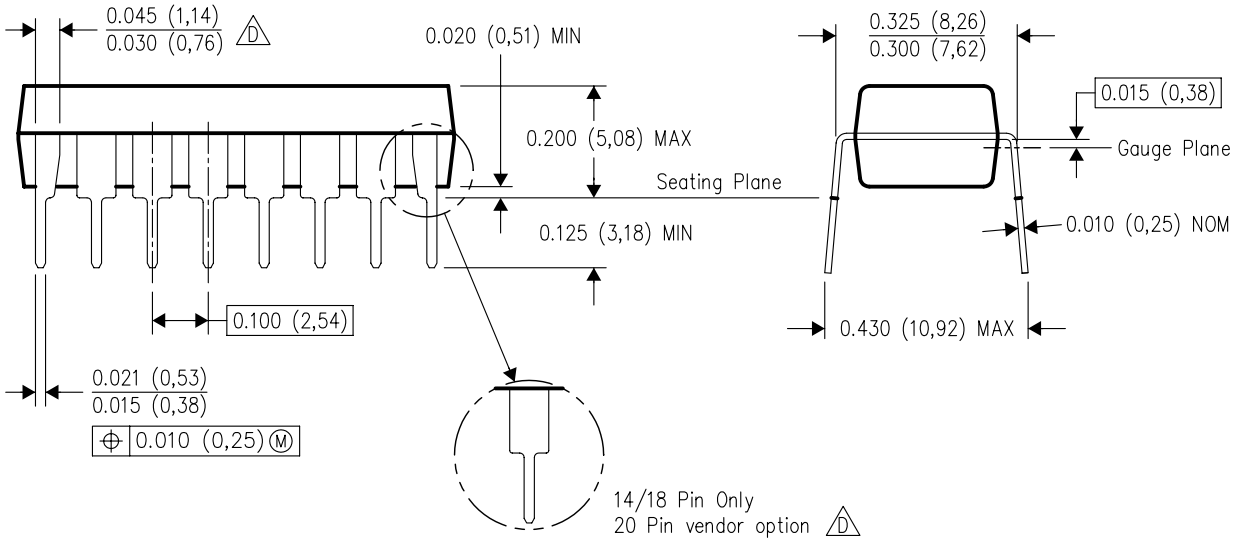
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

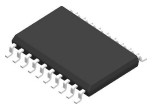


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

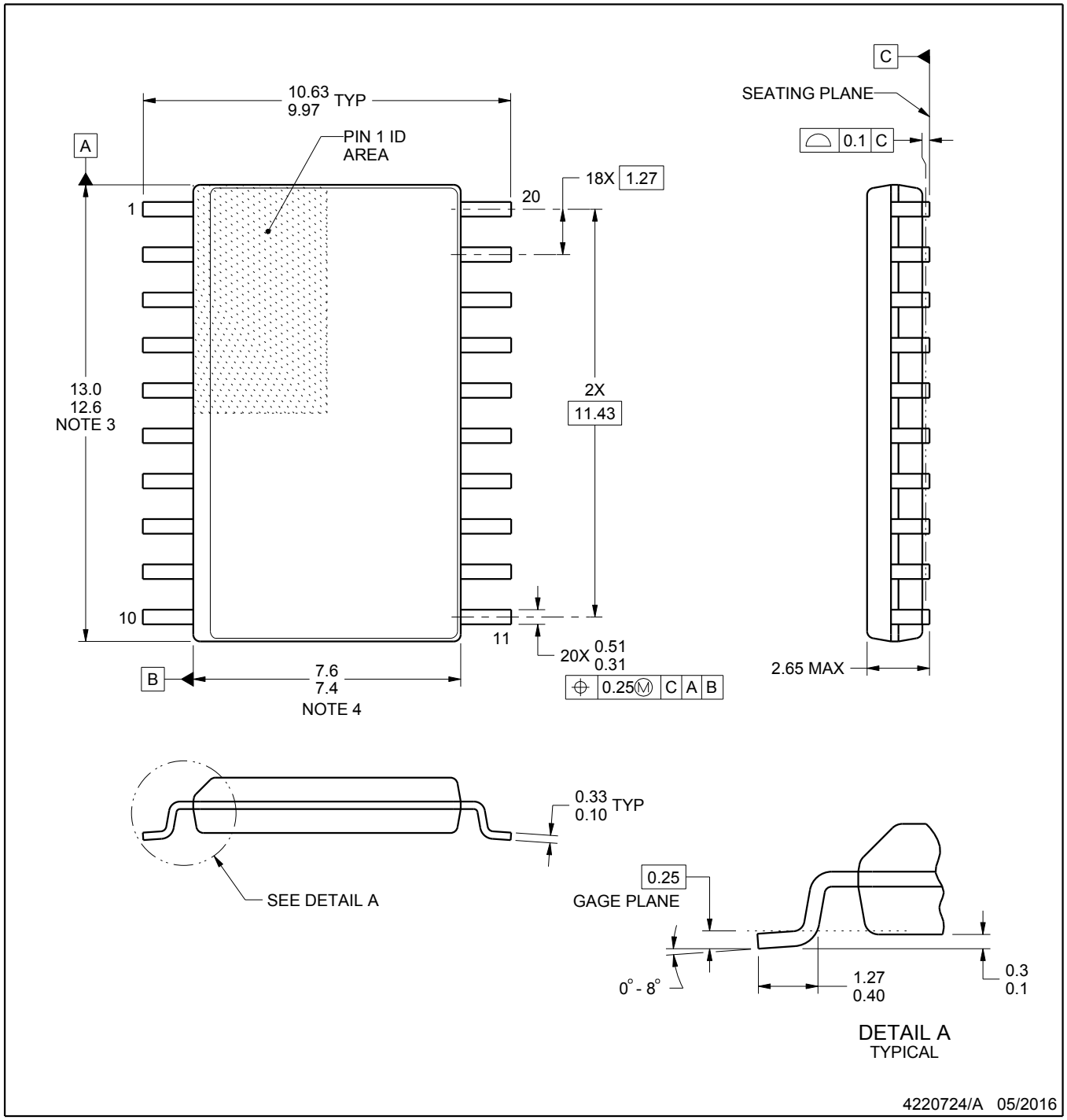


PACKAGE OUTLINE

DW0020A

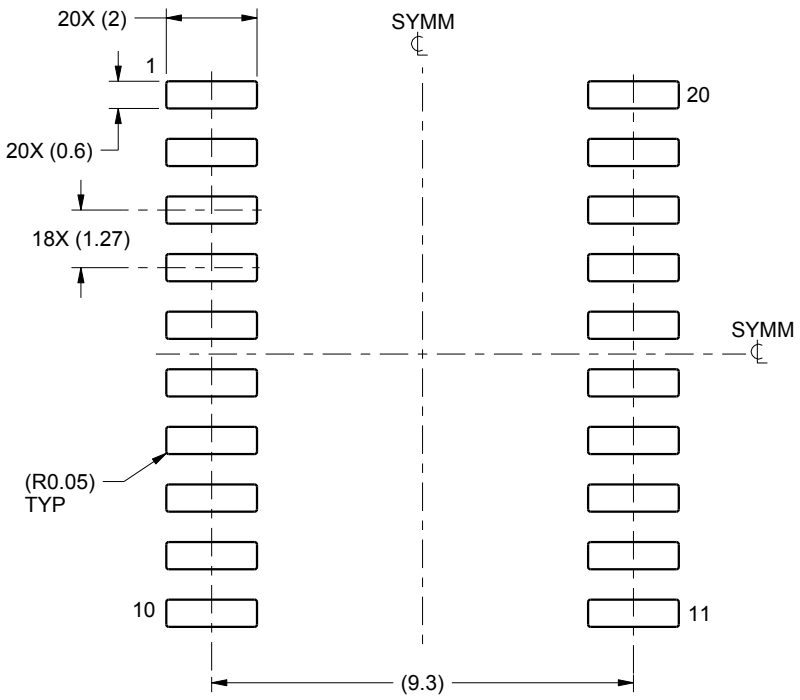
SOIC - 2.65 mm max height

SOIC

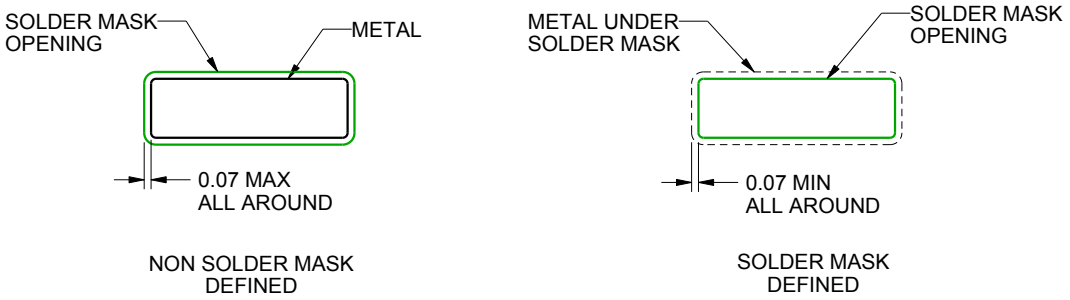


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

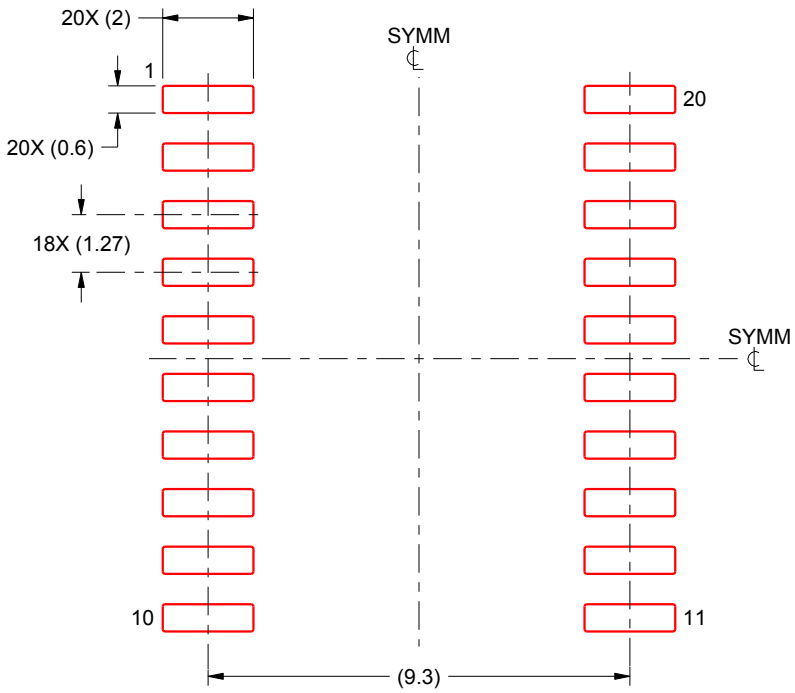


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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