Description

The F1431B is a high linearity RF Digital Variable Gain Amplifier, (DVGA) used as the power amplifier driver in transmitter applications. The F1431B provides 14dB gain, +41.1dBm OIP3, and a 4.2dB noise figure (NF) at 2.0GHz. The digital step attenuator (DSA) has 23dB range with a 0.5dB step size and operates from 0.35GHz to 3GHz with one tuning circuit. This device uses a single 5V supply and 150mA of current.

The F1431B is packaged in a 4 × 4 mm, 24-pin Thin-QFN. The impedance of RFIN and RFOUT is 50Ω for ease of integration into the RF signal path.

Competitive Advantage

- High integration
- Smallest package
- Single bill of materials (BOM) for 0.35GHz to 3GHz applications
- Complement to F1423, TX Differential Input RF Amplifier

Typical Applications

- Multi-mode, multi-carrier transmitters
- TETRA frequency bands
- GSM850/900 base stations
- PCS1900 base stations
- DCS1800 base stations
- WiMAX and LTE base stations
- UMTS/WCDMA 3G base stations
- PHS/PAS base stations
- Public safety infrastructure

Table 1. Typical Band Performance Summary

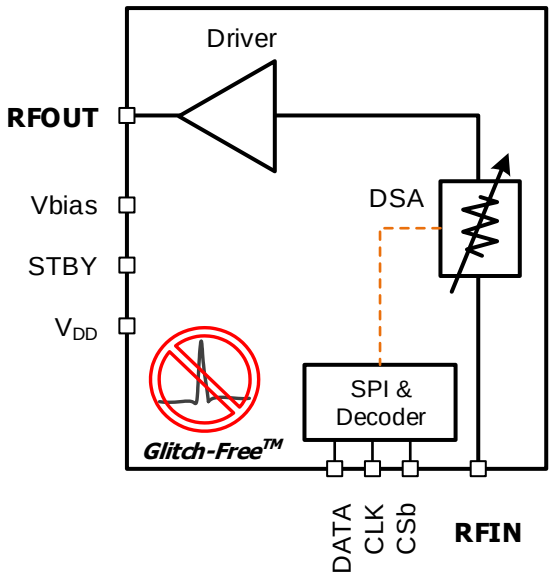
RF Frequency (GHz)	0.7	2.0	2.7
Maximum Gain (dB)	15.6	14.3	12.8
NF at Maximum Gain (dB)	4.0	4.2	4.5
OIP3 at Maximum Gain (dBm)	43.8	41.1	42
OP1dB at Maximum Gain (dBm)	23.5	23.3	23.1
DC Current (mA)	150	150	150
Power Dissipation (mW)	750	750	750

Features

- 0.35GHz to 3GHz operating range
- 14.3dB typical gain at 2GHz
- *Glitch-Free™* 23dB gain adjustment
- 0.5dB step size
- 4.2dB NF at 2GHz
- +41.1dBm OIP3 at 2GHz
- +23.3dBm output P1dB at 2GHz
- Single 5V supply voltage
- I_{DD} = 150mA
- 50Ω single-ended input/output impedances
- 1.8V and 3.3V logic support
- Standby Mode for power savings
- Operating temperature (T_{CASE}) range: -40°C to +105°C
- 4 x 4 mm, 24-TQFN package

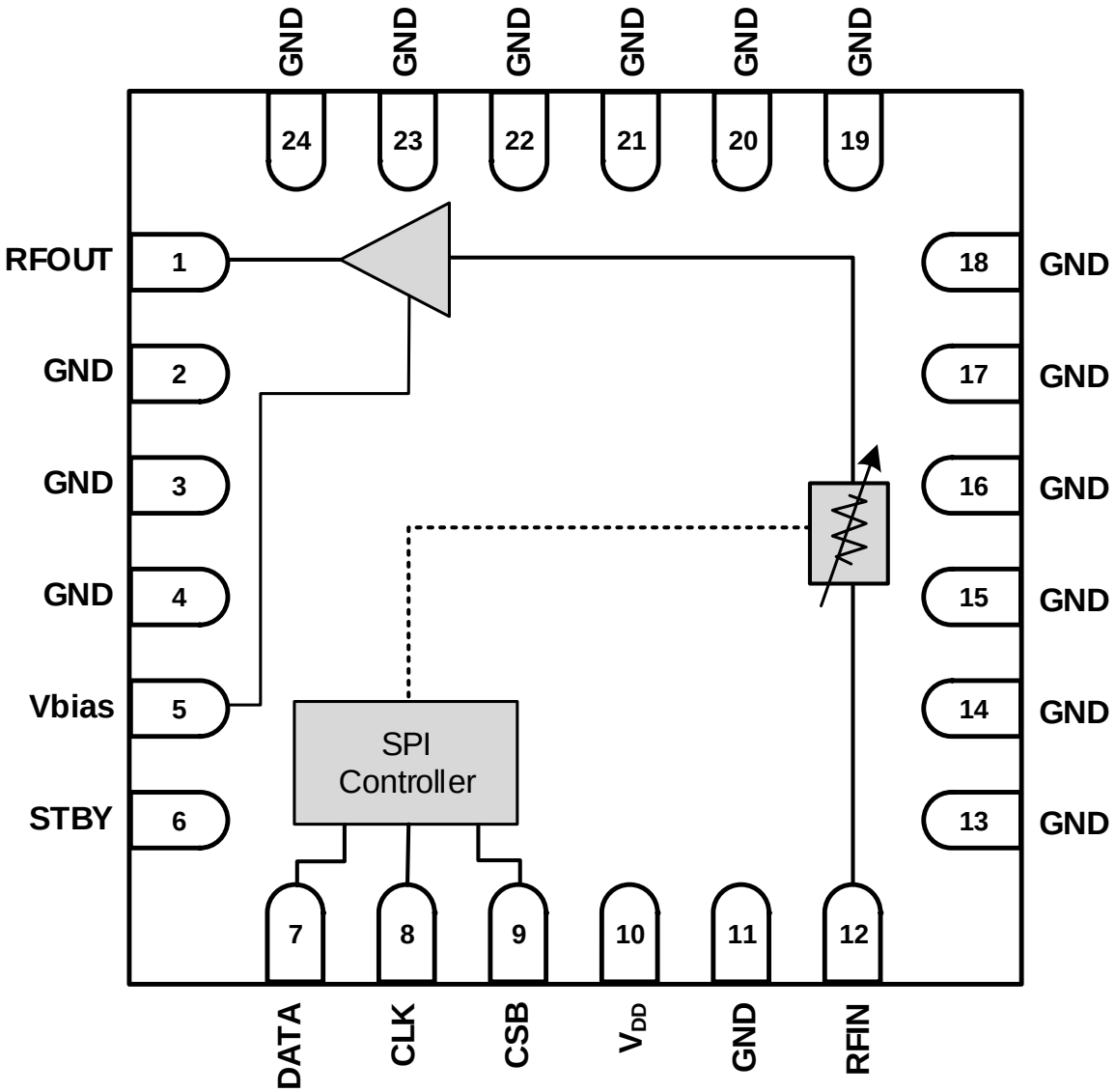
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 4 × 4 × 0.75 mm, 24-TQFN Package – Top View



Pin Descriptions

Table 2. Pin Descriptions

Number	Name	Description
1	RFOUT	The RF amplifier output is tuned and biased via an external circuit (see Figure 41). These components should be placed as close as possible to the package and pin 1 for the best RF performance. An external DC block is required before the signal is routed to the next stage. Refer to the bill of materials (see Table 13) for proper matching values.
2, 3, 4, 11, 13–24	GND	Ground this pin. This pin is internally connected to the exposed paddle.
5	Vbias	Connect a 390Ω series resistor (R1 in Figure 41) from Vbias to V_{DD}. Do not populate R2.
6	STBY	Digital pin. Set this pin to a logic LOW or open for Normal Operation Mode. Set this pin to a logic HIGH for Standby Mode. There is a 400kΩ internal pull-down resistor on this pin.
7	DATA	Data input: 1.8V and 3.3V logic compatible.
8	CLK	Clock input: 1.8V and 3.3V logic compatible.
9	CSb	Chip select input: 1.8V and 3.3V logic compatible.
10	V_{DD}	5V power supply. Connect to a common V_{DD} and use bypass capacitors as close to the pin as possible.
12	RFIN	DSA RF input. An external DC block is required if DC is present on the RF line.
	EPAD	Exposed pad. This pad is internally connected to GND. Solder this exposed pad to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the stated RF performance.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F1431B at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Power Supply Voltage	V_{DD}	-0.3	+5.5	V
DATA, CSb, CLK, STBY	V_{Cntrl}	-0.3	Lower of (V_{DD}+0.3,+3.9)	V
Vbias	V_{bias}	-0.3	+4.0	V
RFIN	V_{RFin}	-0.3	+0.3	V
RFOUT Externally Applied DC Voltage	V_{RFout}	- 0.15	+6.0	V
RF Input Power (applied for 24 hours maximum) (V_{DD} applied, STBY= LOW, Attenuation = 0 dB)	P_{in1}		+21	dBm
RF Input Power (applied for 24 hours maximum) (V_{DD} applied, STBY= LOW, Attenuation = 23 dB)	P_{in2}		+21	dBm
RF Input Power (applied for 24 hours maximum) (V_{DD} applied, STBY= HIGH, Attenuation = 0 dB)	P_{in3}		+21	dBm
RF Input Power (applied for 24 hours maximum) (V_{DD} applied, STBY= HIGH, Attenuation = 23 dB)	P_{in4}		+21	dBm
RF Input Power (applied for 24 hours maximum) (V_{DD} = 0V, STBY= LOW)	P_{in5}		+9	dBm
Continuous Power Dissipation	P_{diss}		1.5	W
Junction Temperature	T_j		150	°C
Storage Temperature Range	T_{STOR}	-65	150	°C
Lead Temperature (soldering, 10s)			260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2014)	V_{ESDHBM}		2000 (Class 2)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}		500 (Class C2)	V

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Supply Voltage	V_{DD}		4.75		5.25	V
Operating Temperature Range	T_{CASE}	Exposed Paddle Temperature	-40		+105	°C
RF Frequency Range	f_{RF}	Operating Range	0.35		3[a]	GHz
RF Source Impedance	Z_{RFI}	Single Ended		50		Ω
RF Load Impedance	Z_{RFO}	Single Ended		50		Ω
Maximum Operating Average Output Power	P_{out_max}	V_{DD} applied, STBY= LOW		14		dBm
	P_{out_max2}	V_{DD} applied, STBY= LOW, Attenuation = 23 dB		15		
Linearity RF Band Designation (IP3 and P1dB performance optimized)[a]						
Linearity RF Frequency Range	$f_{RF\_LB\_LIN}$	Low-band	0.38		1	GHz
	$f_{RF\_MB\_LIN}$	Mid-band	1.42		2.03	GHz
	$f_{RF\_HB\_LIN}$	High-band	2.1		2.7	GHz
Oversample RF Band Designation[a]						
Oversample RF Frequency Range	$f_{RF\_LB\_DPD}$	Low-band	0.35		1.1	GHz
	$f_{RF\_MB\_DPD}$	Mid-band	1.4		2.1	GHz
	$f_{RF\_HB\_DPD}$	High-band	1.93		3.0	GHz

[a] Though device linearity is specified over the desired signal bandwidth, gain flatness is specified over a broader frequency range to account for extended digital pre-distortion (DPD) bandwidth requirements.

Electrical Characteristics

See the schematic in Figure 41 for the applicable circuit. Specifications apply when operated with V_{DD} = +5.0V, T_{CASE} = +25°C, f_{RF} = 2.0GHz, STBY pin = LOW, Z_S = Z_L = 50Ω, maximum gain setting, output power = +8dBm/tone unless stated otherwise. Losses due to Evaluation Board traces and connectors are de-embedded.

Table 5. Electrical Characteristics – General

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input HIGH Threshold	V_{IH}		***1.1***[a]		Lower of (V_{DD},+3.6) [b]	V
Logic Input LOW Threshold	V_{IL}				***0.63***	V
Logic Current	I_{CNTL}	CLK, CSb, DATA	***-10***		***+10***	µA
STBY Logic Current	I_{STBY}	STBY pin	***-10***		***+10***	µA
DC Current[c]	I_{DD}			150	***177***	mA
Standby Current	I_{DD_STBY}			1.1	***1.9***	mA
Gain Range	DSA_{ADJ}			23		dB
Gain Step	G_{STEP}	LSB		0.5		dB
Attenuator Glitching	$ATTN_G$	Worse-case step condition		0.5		dB
Gain Settling Time[d]	G_{ST}	50% of CSb to 10% / 90% RF		0.5	0.8	µs
Power ON Switching Time	t_{ON}	50% Standby signal to RF output settled to within ±0.5dB.		0.1	1	µs
Power OFF Switching Time	t_{OFF}	50% Standby signal to 35dBc reduction of output power.		0.15	1	µs
Serial Clock Speed					***10***	MHz
CSb to First Serial Clock Rising Edge	t_{LS}	SPI 3-wire bus. 50% of CSb falling edge to 50% of CLK rising edge.	***10***			ns
Serial Data Hold Time	t_H	SPI 3-wire bus. 50% of CLK rising edge to 50% of DATA falling edge.	***10***			ns
Final Serial Clock Rising Edge to CSb	t_{LCS}	SPI 3-wire bus. 50% of CLK rising edge to 50% of CSb rising edge.	***10***			ns

[a] Items in min/max columns in ***bold italics*** are guaranteed by test.

[b] Items in min/max columns that are not bold/italics are guaranteed by design characterization.

[c] For input signal power level equal to P1dB, expect DC current to increase above the typical value.

[d] Speeds are measured after SPI programming is completed (data latched with CSb = HIGH).

Electrical Characteristics – Low Band

See the schematic in Figure 41 for the applicable circuit. Specifications apply when operated with V_{DD} = +5.0V, T_{CASE} = +25°C, f_{RF} = 0.7GHz, STBY pin = LOW, Z_S = Z_L = 50Ω, maximum gain setting, output power = +8dBm/tone unless stated otherwise. Losses due to Evaluation Board traces and connectors are de-embedded.

Table 6. Electrical Characteristics – Low Band

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
RF Input Return Loss	RL_{IN_LB}			17		dB
RF Output Return Loss	RL_{OUT_LB}			16		dB
Gain	G_{MAX_LB}		***14.7*** [a]	15.6	***16.5***	dB
Gain Variation versus Temperature	G_{VAR_LB}	Over exposed paddle temperature and relative to +25°C		+0.25 / -0.25		dB
Gain Attenuated	G_{MIN_LB}	23dB attenuation	***-7.9***	-7.0	***-6.1***	dB
Gain Flatness	G_{FLAT_LB}	In any 300MHz BW from 0.35GHz to 1.1GHz		0.3		dB
Step Error	$ERROR_{S\_LB}$	Maximum error between adjacent attenuation steps		-0.21 / +0.05		dB
Absolute Error	$ERROR_{A\_LB}$	Over attenuation range referenced to maximum gain state		-0.4 / +0.1		dB
Phase Deviation	θ_{DEV_LB}	Worse-case adjacent state		1		Deg
Noise Figure	NF_{LB}	0dB attenuation		4.0		dB
		T_{CASE} = +105°C		4.2		dB
		23dB attenuation		26.5		dB
Output Third-Order Intercept Point	$OIP3_{LB1}$	5MHz tone separation	***41***	43.8		dBm
	$OIP3_{LB2}$	5MHz tone separation 10dB attenuation		43.8		dBm
	$OIP3_{LB3}$	Pout = 0dBm/tone 5MHz tone separation 23dB attenuation		46		dBm
Output 1dB Compression	$OP1dB_{LB1}$		***22.3***	23.5		dBm
	$OP1dB_{LB2}$	10dB attenuation		23		dBm
	$OP1dB_{LB3}$	23dB attenuation		23		dBm

[a] Items in min/max columns in ***bold italics*** are guaranteed by test.

[b] Items in min/max columns that are not bold/italics are guaranteed by design characterization.

Electrical Characteristics – Mid Band

See the schematic in Figure 41 for the applicable circuit. Specifications apply when operated with V_{DD} = +5.0V, T_{CASE} = +25°C, f_{RF} = 2.0GHz, STBY pin = LOW, Z_S = Z_L = 50Ω, maximum gain setting, output power = +8dBm/tone unless stated otherwise. Losses due to Evaluation Board traces and connectors are de-embedded.

Table 7. Electrical Characteristics – Mid Band

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
RF Input Return Loss	RL_{IN_MB}			18		dB
RF Output Return Loss	RL_{OUT_MB}			14		dB
Gain	G_{MAX_MB}		***13.1***[a]	14.3	***15.5***	dB
Gain Variation versus Temperature	G_{VAR_MB}	Over exposed paddle temperature and relative to +25°C		+0.4 / -0.4		dB
Gain Attenuated	G_{MIN_MB}	23dB attenuation	***-9.6***	-8.4	***-7.2***	dB
Gain Flatness	G_{FLAT_MB}	In any 400MHz BW from F_{RF} = 1.4GHz to 2.1GHz		0.8		dB
Step Error	$ERROR_{S\_MB}$	Max error between adjacent attenuation steps		-0.19 / +0.06		dB
Absolute Error	$ERROR_{A\_MB}$	Over attenuation range referenced to max gain state		-0.25 / +0.13		dB
Phase Deviation	θ_{DEV_MB}	Worse-case adjacent state		2		deg
Noise Figure	NF_{MB}	0dB attenuation		4.2		dB
		T_{CASE} = +105°C		4.5		dB
		23dB attenuation		27		dB
Output Third Order Intercept Point	$OIP3_{MB1}$	5MHz tone separation	***38***	41.1		dBm
	$OIP3_{MB2}$	5MHz tone separation 10dB attenuation		41		dBm
	$OIP3_{MB3}$	Pout = 0dBm/tone 5MHz tone separation 23dB attenuation		42.4		dBm
Output 1dB Compression	$OP1dB_{MB1}$		***22.1***	23.3		dBm
	$OP1dB_{MB2}$	10dB attenuation		23.4		dBm
	$OP1dB_{MB3}$	23dB attenuation		23.4		dBm

[a] Items in min/max columns in ***bold italics*** are guaranteed by test.

[b] Items in min/max columns that are not bold/italics are guaranteed by design characterization.

Electrical Characteristics – High Band

See the schematic in Figure 41 for the applicable circuit. Specifications apply when operated with V_{DD} = +5.0V, T_{CASE} = +25°C, f_{RF} = 2.7GHz, STBY pin = LOW, Z_S = Z_L = 50Ω, maximum gain setting, output power = +8dBm/tone unless stated otherwise. Losses due to Evaluation Board traces and connectors are de-embedded.

Table 8. Electrical Characteristics – High Band

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
RF Input Return Loss	RL_{IN_HB}			13		dB
RF Output Return Loss	RL_{OUT_HB}			8		dB
Gain	G_{MAX_HB}		***11.7***[a]	12.8	***13.9***	dB
Gain Variation versus Temperature	G_{VAR_HB}	Over exposed paddle temperature and relative to +25°C		+0.5 / -0.4		dB
Gain Attenuated	G_{MIN_HB}	23dB attenuation	***-11.0***	-9.9	***-8.8***	dB
Gain Flatness	G_{FLAT_HB}	In any 400MHz BW from 2.1GHz to 3.0GHz		0.9		dB
Step Error	$ERROR_{S\_HB}$	Max error between adjacent attenuation steps		-0.21 / +0.10		dB
Absolute Error	$ERROR_{A\_HB}$	Over attenuation range referenced to max gain state		-0.28 / +0.18		dB
Phase Deviation	θ_{DEV_HB}	Worse-case adjacent state		3.5		deg
Noise Figure	NF_{HB}	0dB attenuation		4.5		dB
		T_{case} = +105°C		4.9		dB
		23dB attenuation		27.0		dB
Output Third Order Intercept Point	$OIP3_{HB1}$	5MHz tone separation	38[b]	42		dBm
	$OIP3_{HB2}$	5MHz tone separation 10dB attenuation		41.9		dBm
	$OIP3_{HB3}$	Pout = 0dBm/tone 5MHz tone separation 23dB attenuation		41.6		dBm
Output 1dB Compression	$OP1dB_{HB1}$		***22.0***	23.1		dBm
	$OP1dB_{HB2}$	10dB attenuation		23.1		dBm
	$OP1dB_{HB3}$	23dB attenuation		23.1		dBm

[a] Items in min/max columns in ***bold italics*** are guaranteed by test.

[b] Items in min/max columns that are not bold/italics are guaranteed by design characterization.

Thermal Characteristics

Table 9. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	θ_{JA}	40	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	θ_{JC}	8.3	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOCs)

Unless otherwise stated the typical operating graphs in the next sections were measured under the following conditions:

- TOCs taken on existing Evaluation Board PCB including matching network
- V_{DD} = 5.0V
- $Z_L = Z_S$ = 50Ω single ended with matching networks
- f_{RF} = 0.7GHz, 2GHz, 2.7GHz
- T_{CASE} = +25°C
- STBY = LOW or open
- 5MHz tone spacing
- Gain setting = maximum gain
- All temperatures are referenced to the exposed paddle
- Pout = +8dBm/tone unless otherwise specified for multi-tone tests

Typical Performance Characteristics

Figure 3. Maximum Gain versus Frequency

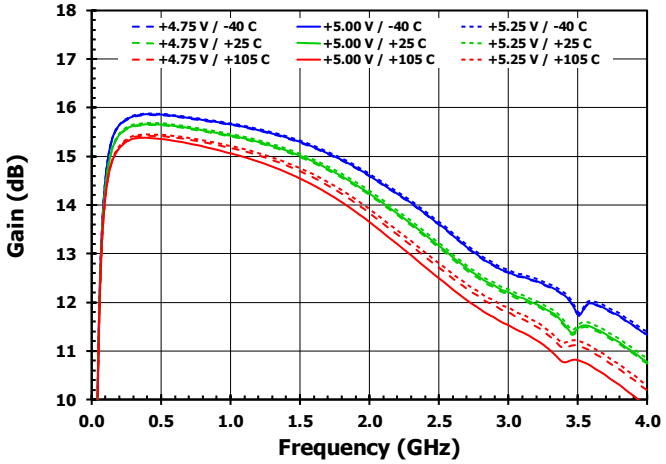


Figure 4. Gain versus Attenuation [2.0 GHz]

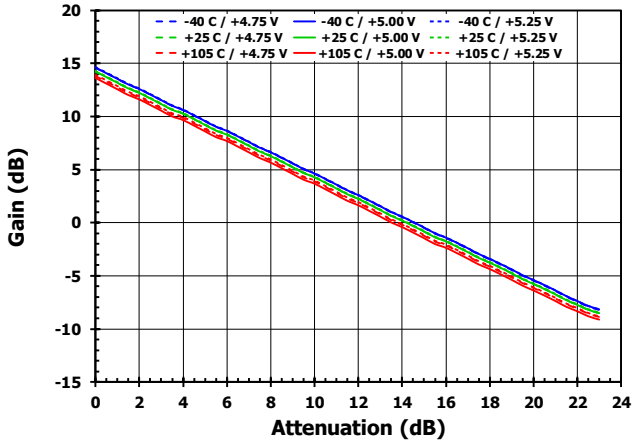


Figure 5. Gain versus Frequency [+25°C, all states]

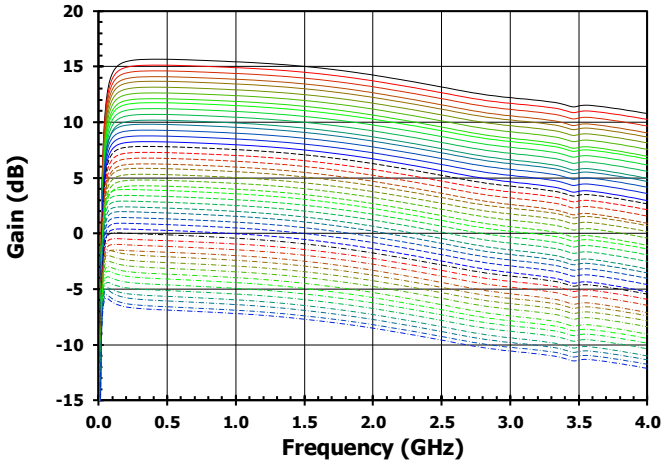


Figure 6. Gain versus Attenuation [+25°C]

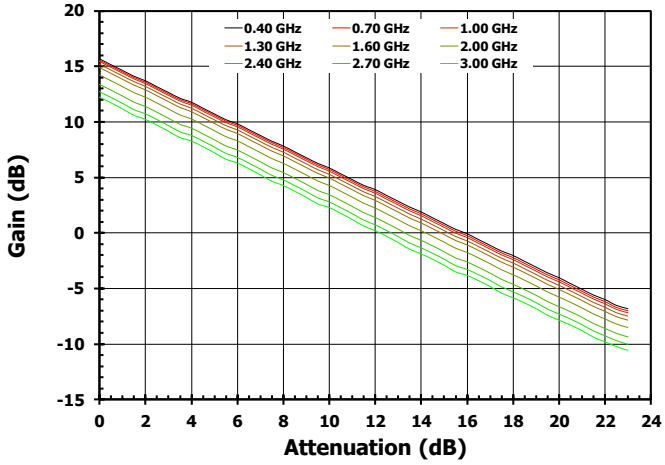


Figure 7. Reverse Isolation versus Frequency [+25°C, all states]

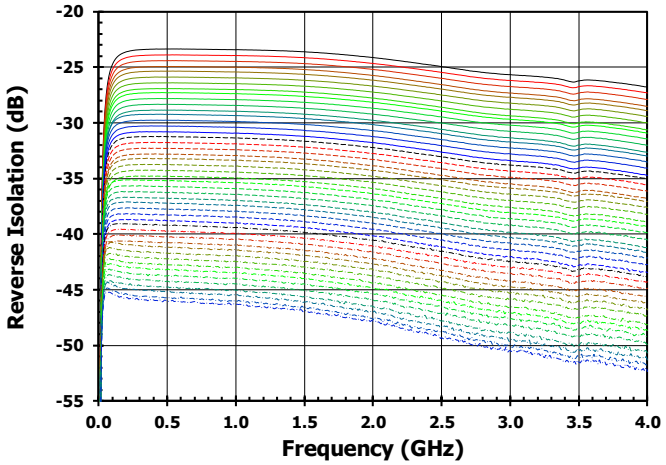


Figure 8. Reverse Isolation versus Attenuation [+25°C]

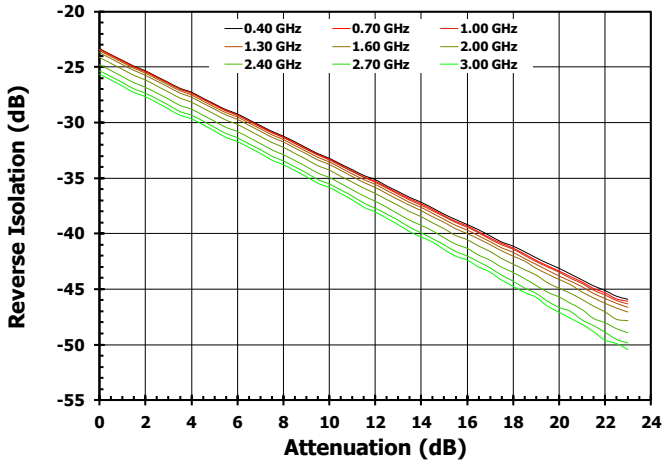


Figure 9. Input Return Loss versus Frequency [+25°C, all states]

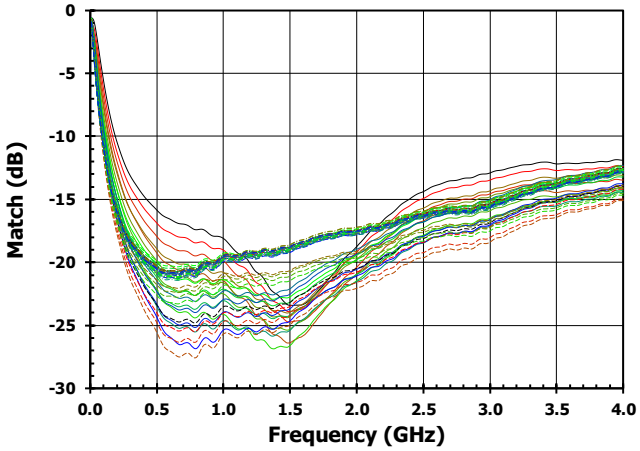


Figure 10. Input Return Loss versus Attenuation [+25°C]

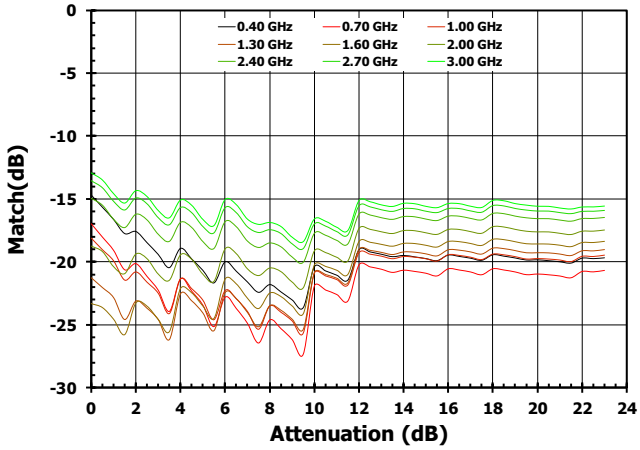


Figure 11. Output Return Loss versus Frequency [+25°C, all states]

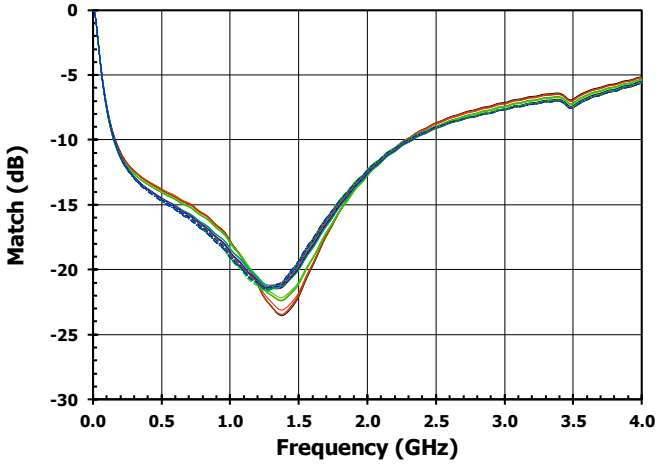


Figure 12. Output Return Loss versus Attenuation [+25°C]

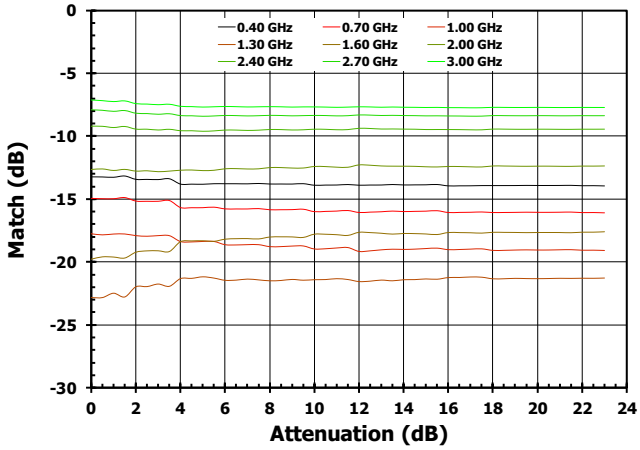


Figure 13. Relative Insertion Phase versus Frequency [+25°C, all states]

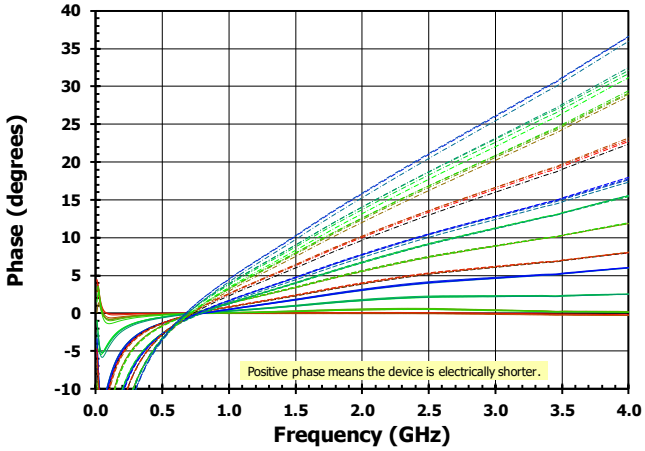


Figure 14. Relative Insertion Phase versus Attenuation [+25°C]

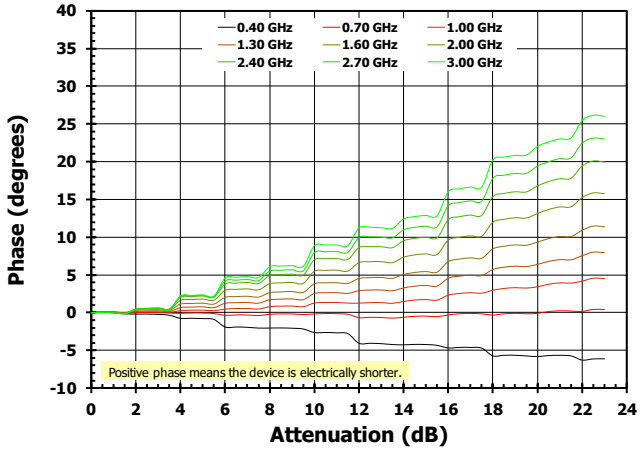


Figure 15. Worse Case Attenuator Accuracy versus Frequency

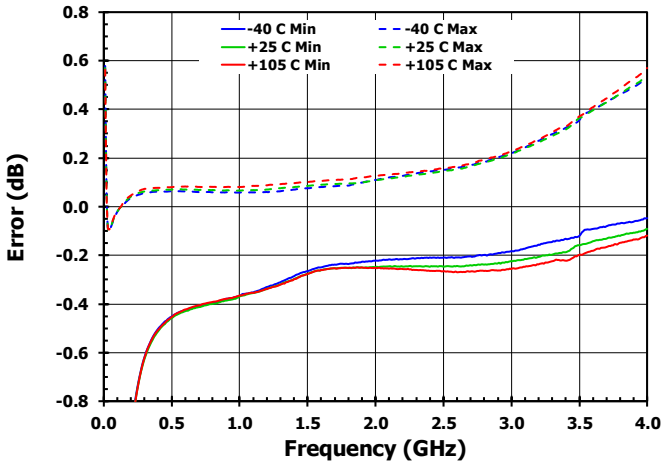


Figure 16. Attenuator Accuracy versus Attenuation

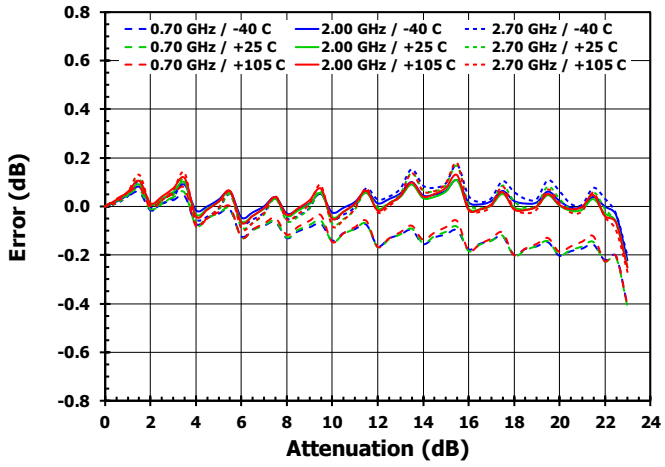


Figure 17. Worse Case Step Accuracy versus Frequency

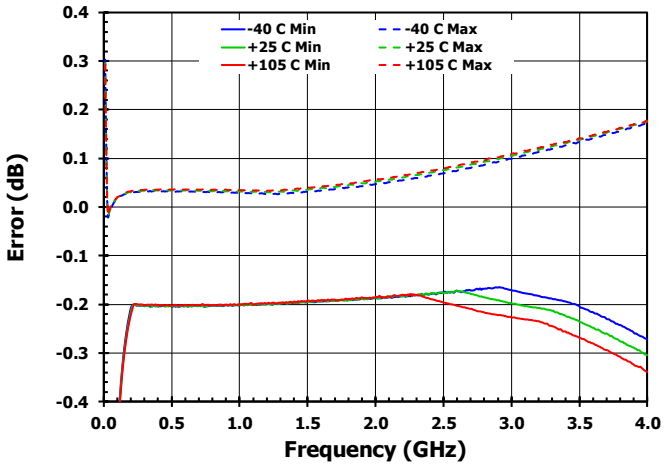


Figure 18. Step Accuracy versus Attenuation

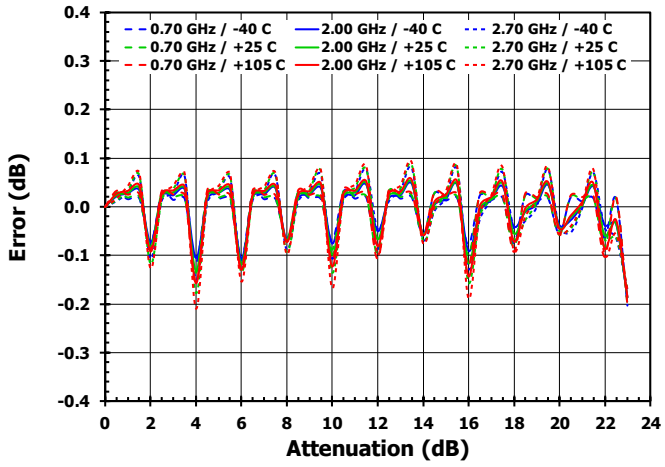


Figure 19. Output P1dB versus Frequency [Attenuation = 0dB]

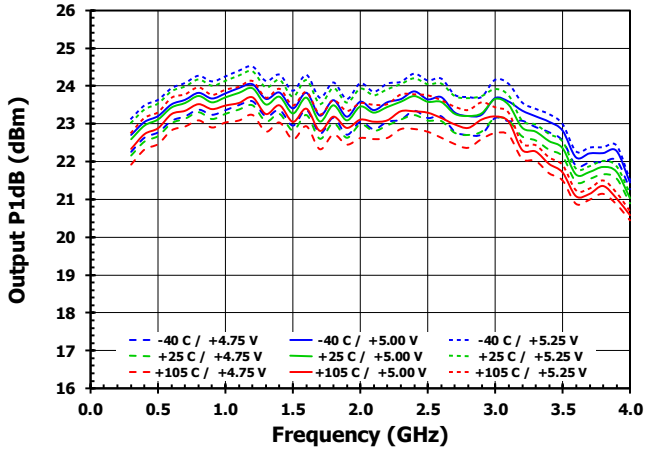


Figure 20. Output IP3 versus Frequency [Attenuation = 0dB]

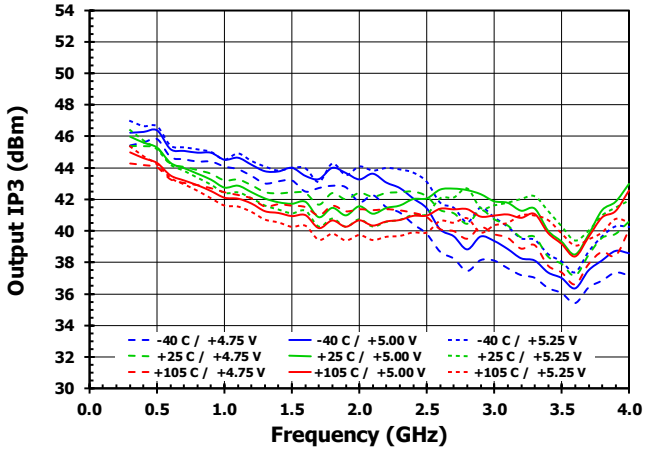


Figure 21. Output P1dB versus Frequency [Attenuation = 10dB]

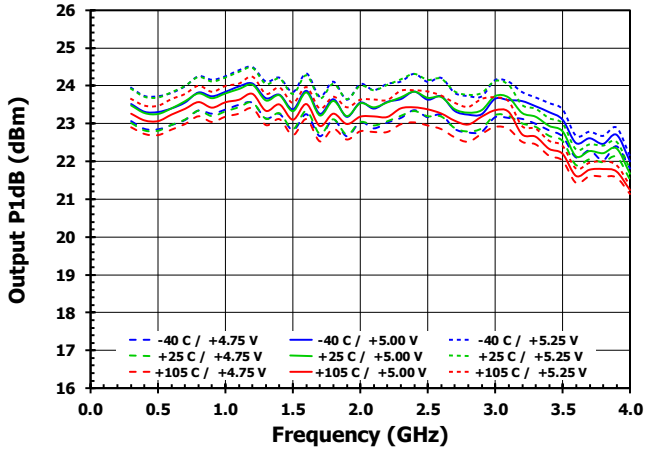


Figure 22. Output IP3 versus Frequency [Attenuation = 10dB]

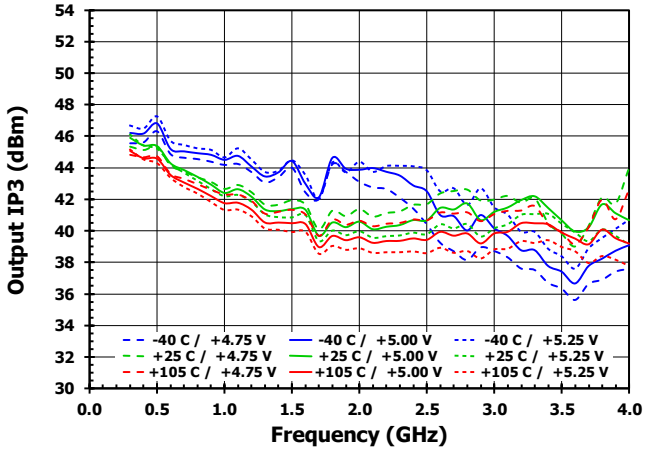


Figure 23. Output P1dB versus Frequency [Attenuation = 23dB]

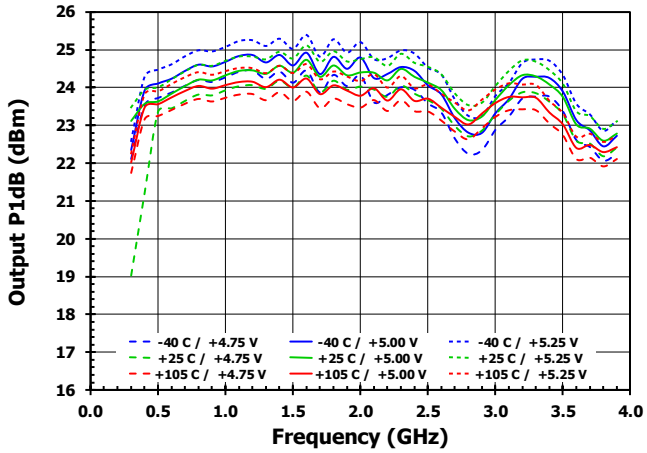


Figure 24. Output IP3 versus Frequency [Attenuation = 23dB]

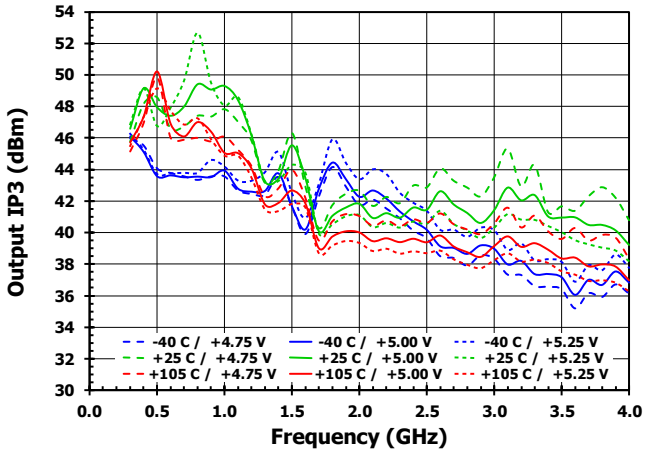


Figure 25. Compression versus Input Power [0.7GHz, Attenuation = 0dB]

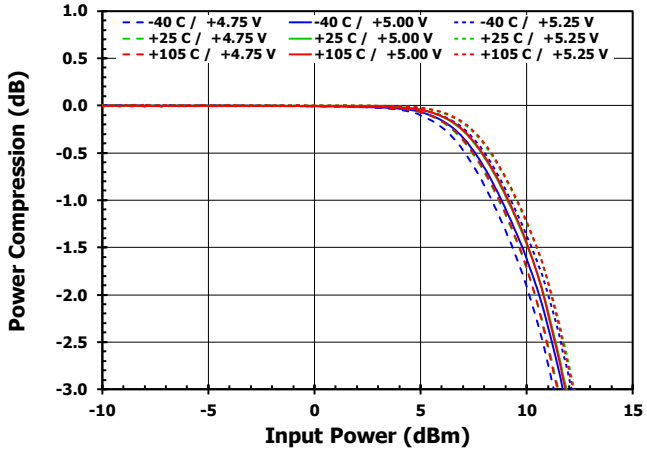


Figure 26. Phase Compression versus Input Power [0.7GHz, Attenuation = 0dB]

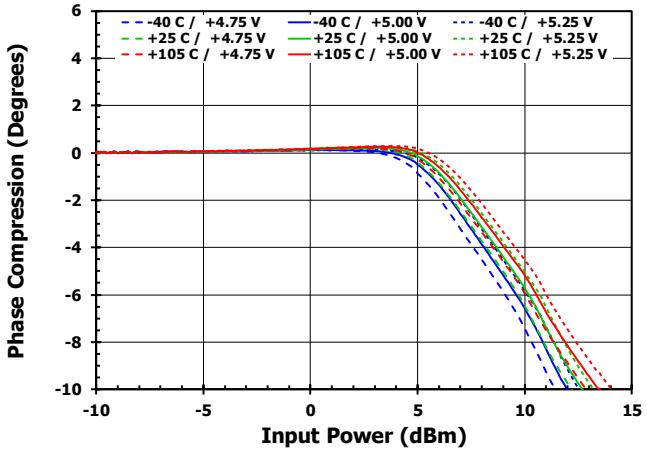


Figure 27. Compression versus Input Power [2.0GHz, Attenuation = 0dB]

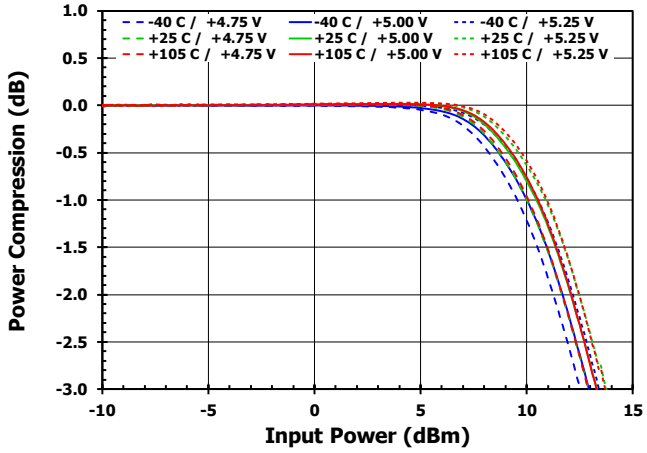


Figure 28. Phase Compression versus Input Power [2.0GHz, Attenuation = 0dB]

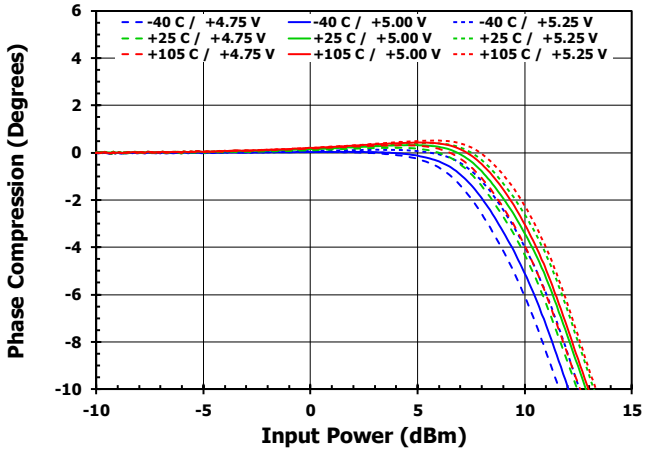


Figure 29. Compression versus Input Power [2.7GHz, Attenuation = 0dB]

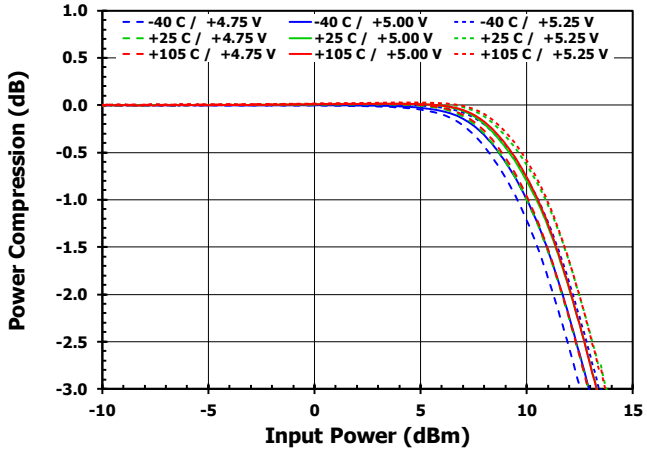


Figure 30. Phase Compression versus Input Power [2.7GHz, Attenuation = 0dB]

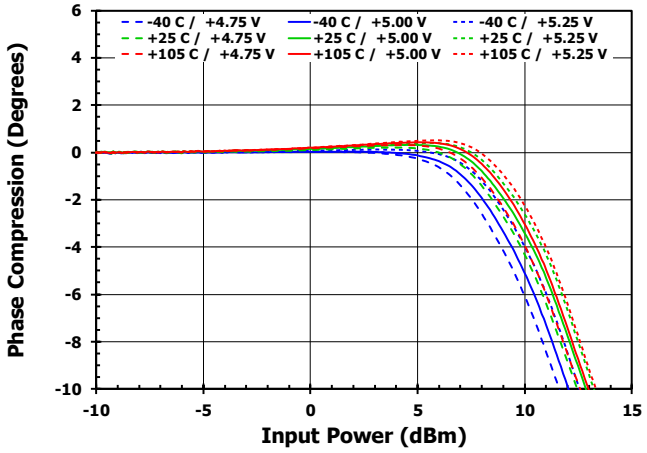


Figure 31. Noise Figure versus Frequency [Attenuation = 0dB]

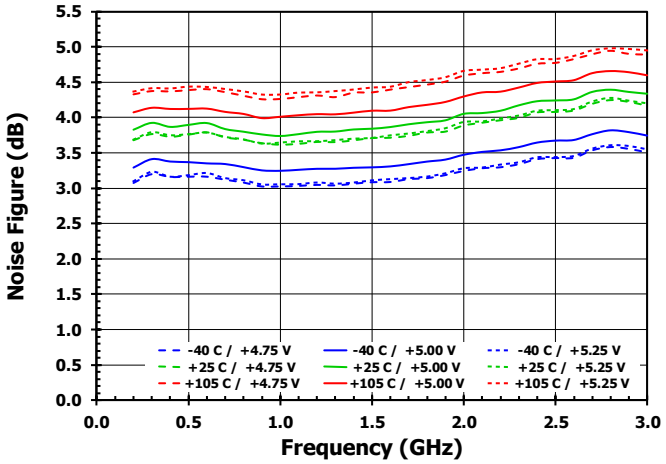


Figure 32. Noise Figure versus Attenuation [2.0GHz]

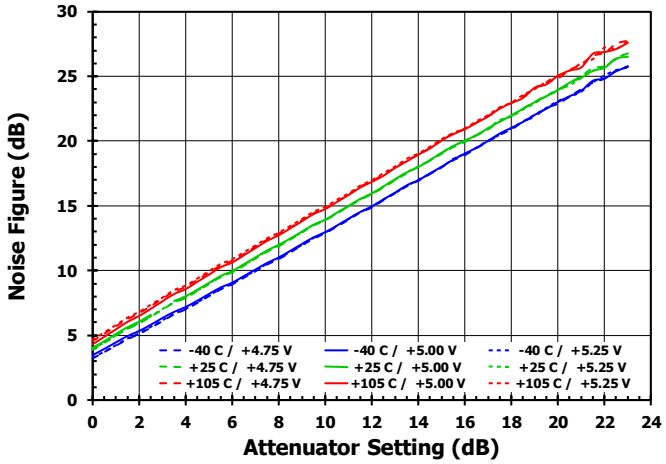


Figure 33. Switching Speed 0 to 23dB

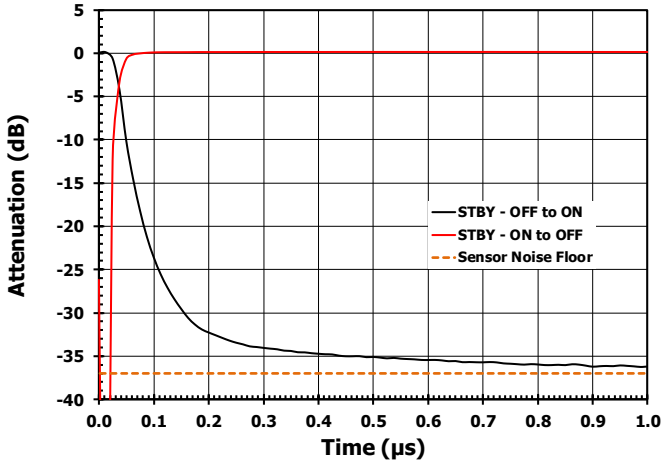


Figure 34. Switching Speed [Maximum Glitch]

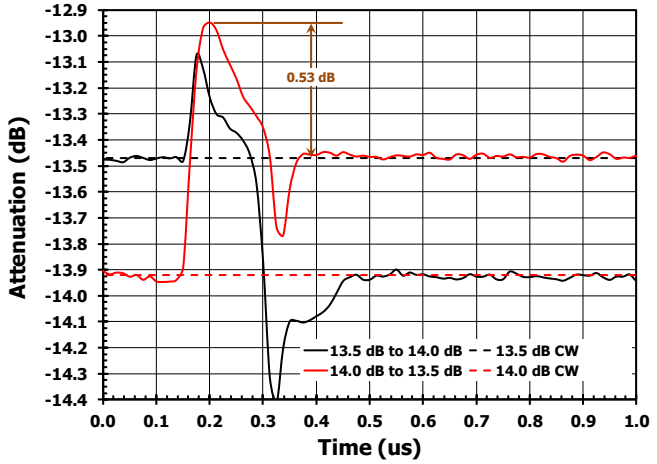


Figure 35. Stability versus Frequency

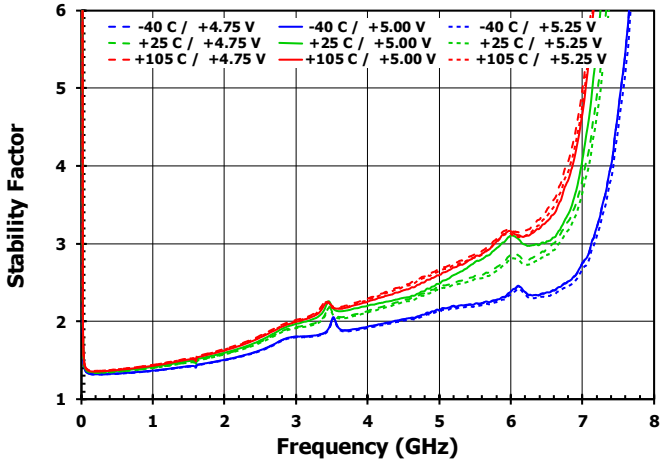
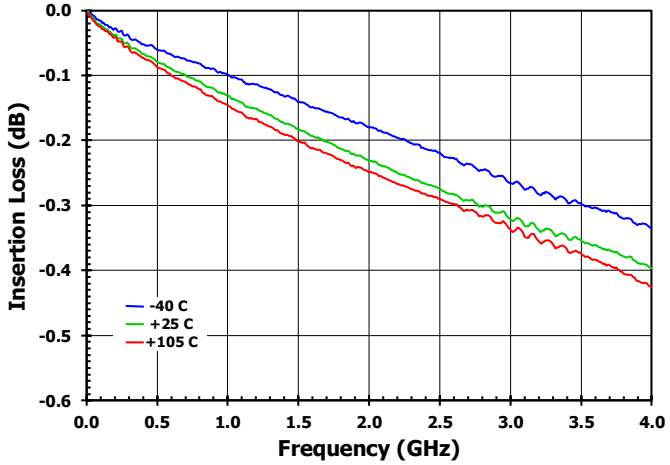


Figure 36. Evaluation Board Insertion Loss versus Frequency



Programming

Serial Control Mode

Data is clocked in with the least significant bit, LSB, first via serial mode. See the timing diagram in Figure 37. The SPI is built with an 8-bit word where 6 bits are used for the attenuation setting per Table 11. Attenuation cannot be set greater than 23dB.

Note: The F1431B includes a CLK inhibit feature designed to minimize sensitivity to CLK bus noise when the device is not being programmed. When CSb is HIGH (> V_{IH}), the CLK input is disabled and serial data (DATA) is not clocked into the shift register. It is recommended that CSb be pulled HIGH (>V_{IH}) when the device is not being programmed.

Figure 37. Serial Register Timing Diagram

Note: The timing specification intervals are shown in blue.

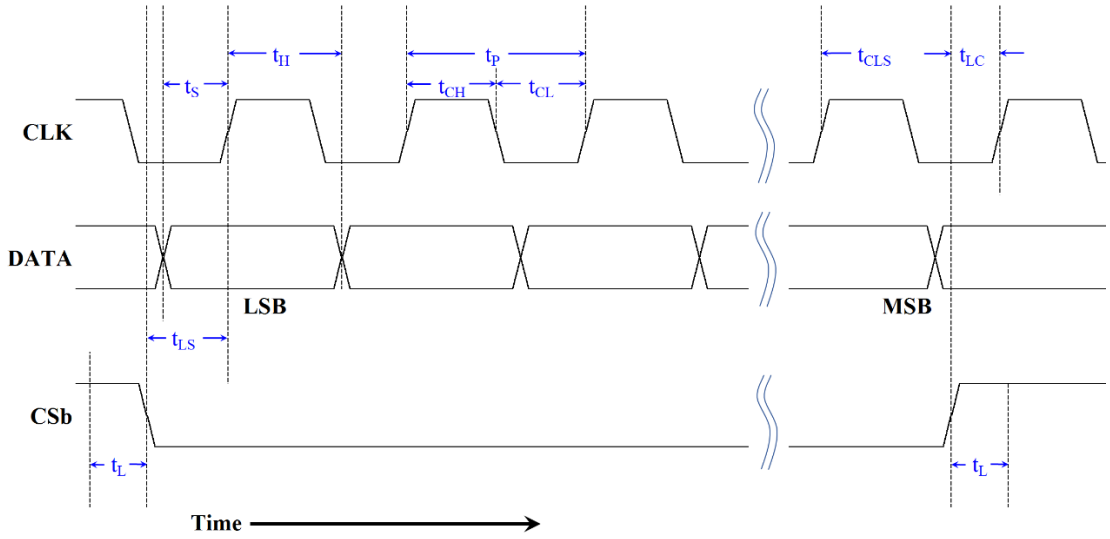


Table 10. SPI Timing Diagram Values for the Serial Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
CLK Frequency	f_C				25	MHz
CLK HIGH Duration Time	t_{CH}		20			ns
CLK LOW Duration Time	t_{CL}		20			ns
DATA to CLK Setup Time	t_S		10			ns
CLK Period [a]	t_P		40			ns
CLK to Data Hold Time	t_H		10			ns
Final CLK Rising Edge to CSb Rising Edge	t_{CLS}		10			ns
CSb to CLK Setup Time	t_{LS}		10			ns
CSb Trigger Pulse Width	t_L		10			ns
CSb Trigger to CLK Setup Time [b]	t_{LC}		10			ns

[a] $(t_{CH} + t_{CL}) \geq 1/f_C$.

[b] Once all desired data is clocked in, t_{LC} represents the time a CSb HIGH must occur before any subsequent CLK signals.

Table 11. F1431B DVGA Attenuation Word Truth Table

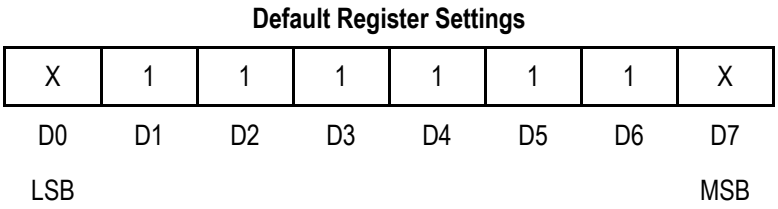
Atten. Setting (dB)	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
0.0	x	0	0	0	0	0	0	x
0.5	x	0	0	0	0	0	1	x
1.0	x	0	0	0	0	1	0	x
1.5	x	0	0	0	0	1	1	x
2.0	x	0	0	0	1	0	0	x
2.5	x	0	0	0	1	0	1	x
3.0	x	0	0	0	1	1	0	x
3.5	x	0	0	0	1	1	1	x
4.0	x	0	0	1	0	0	0	x
4.5	x	0	0	1	0	0	1	x
5.0	x	0	0	1	0	1	0	x
5.5	x	0	0	1	0	1	1	x
6.0	x	0	0	1	1	0	0	x
6.5	x	0	0	1	1	0	1	x
7.0	x	0	0	1	1	1	0	x
7.5	x	0	0	1	1	1	1	x
8.0	x	0	1	0	0	0	0	x
8.5	x	0	1	0	0	0	1	x
9.0	x	0	1	0	0	1	0	x
9.5	x	0	1	0	0	1	1	x
10.0	x	0	1	0	1	0	0	x
10.5	x	0	1	0	1	0	1	x
11.0	x	0	1	0	1	1	0	x
11.5	x	0	1	0	1	1	1	x
12.0	x	0	1	1	0	0	0	x
12.5	x	0	1	1	0	0	1	x
13.0	x	0	1	1	0	1	0	x
13.5	x	0	1	1	0	1	1	x
14.0	x	0	1	1	1	0	0	x
14.5	x	0	1	1	1	0	1	x
15.0	x	0	1	1	1	1	0	x
15.5	x	0	1	1	1	1	1	x

Atten. Setting (dB)	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
16.0	x	1	0	0	0	0	0	x
16.5	x	1	0	0	0	0	1	x
17.0	x	1	0	0	0	1	0	x
17.5	x	1	0	0	0	1	1	x
18.0	x	1	0	0	1	0	0	x
18.5	x	1	0	0	1	0	1	x
19.0	x	1	0	0	1	1	0	x
19.5	x	1	0	0	1	1	1	x
20.0	x	1	0	1	0	0	0	x
20.5	x	1	0	1	0	0	1	x
21.0	x	1	0	1	0	1	0	x
21.5	x	1	0	1	0	1	1	x
22.0	x	1	0	1	1	0	0	x
22.5	x	1	0	1	1	0	1	x
23.0	x	1	0	1	1	1	0	x
23.0	x	1	0	1	1	1	1	x
23.0	x	1	1	0	0	0	0	x
23.0	x	1	1	0	0	0	1	x
23.0	x	1	1	0	0	1	0	x
23.0	x	1	1	0	0	1	1	x
23.0	x	1	1	0	1	0	0	x
23.0	x	1	1	0	1	0	1	x
23.0	x	1	1	0	1	1	0	x
23.0	x	1	1	0	1	1	1	x
23.0	x	1	1	1	0	0	0	x
23.0	x	1	1	1	0	0	1	x
23.0	x	1	1	1	0	1	0	x
23.0	x	1	1	1	0	1	1	x
23.0	x	1	1	1	1	0	0	x
23.0	x	1	1	1	1	0	1	x
23.0	x	1	1	1	1	1	0	x
23.0	x	1	1	1	1	1	1	x

Serial Mode Default Condition

When the device is first powered on, it will default to the maximum attenuation setting shown below:

Figure 38. Serial Mode Default Condition (Maximum Attenuation)



Standby Mode

The F1431B has a separate pin (STBY pin 6) that allows the device to be put in Standby Mode to reduce power consumption.

Table 12. STBY Logic Truth Table

Parameter	Level	Function
STBY	Logic LOW or Open Circuit	Powered On
	Logic HIGH	Powered Off

F1431B Evaluation Kit

Figure 39. Top View

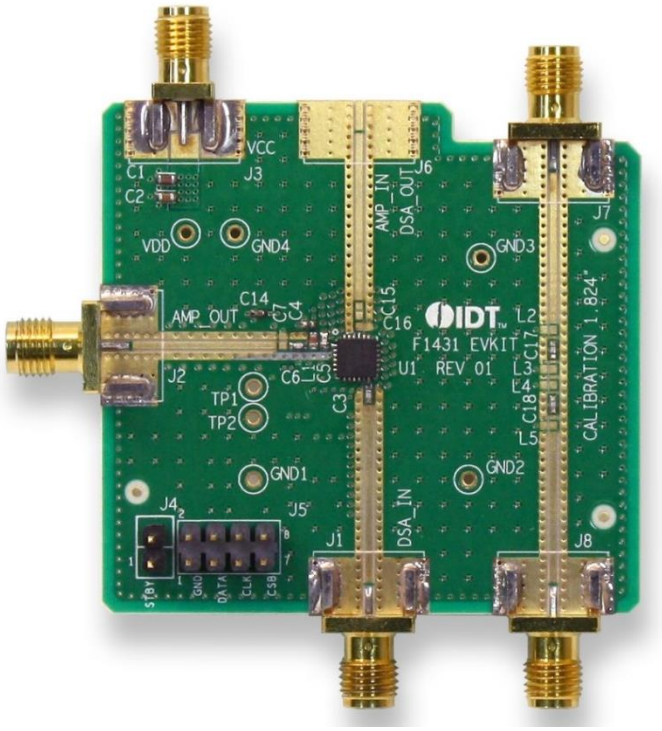
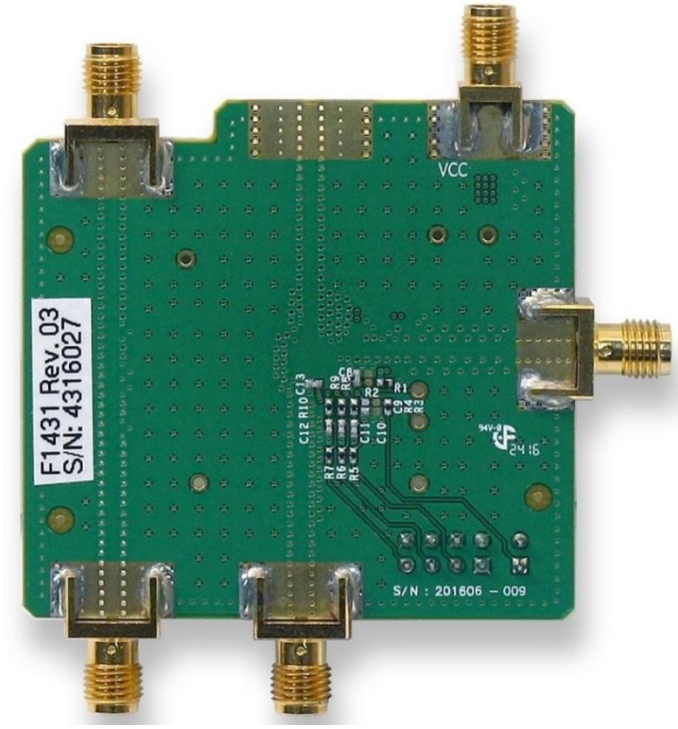


Figure 40. Bottom View



Evaluation Kit / Applications Circuit

Not all components are required for proper operation. See the BOM for components not required.

Figure 41. Electrical Schematic

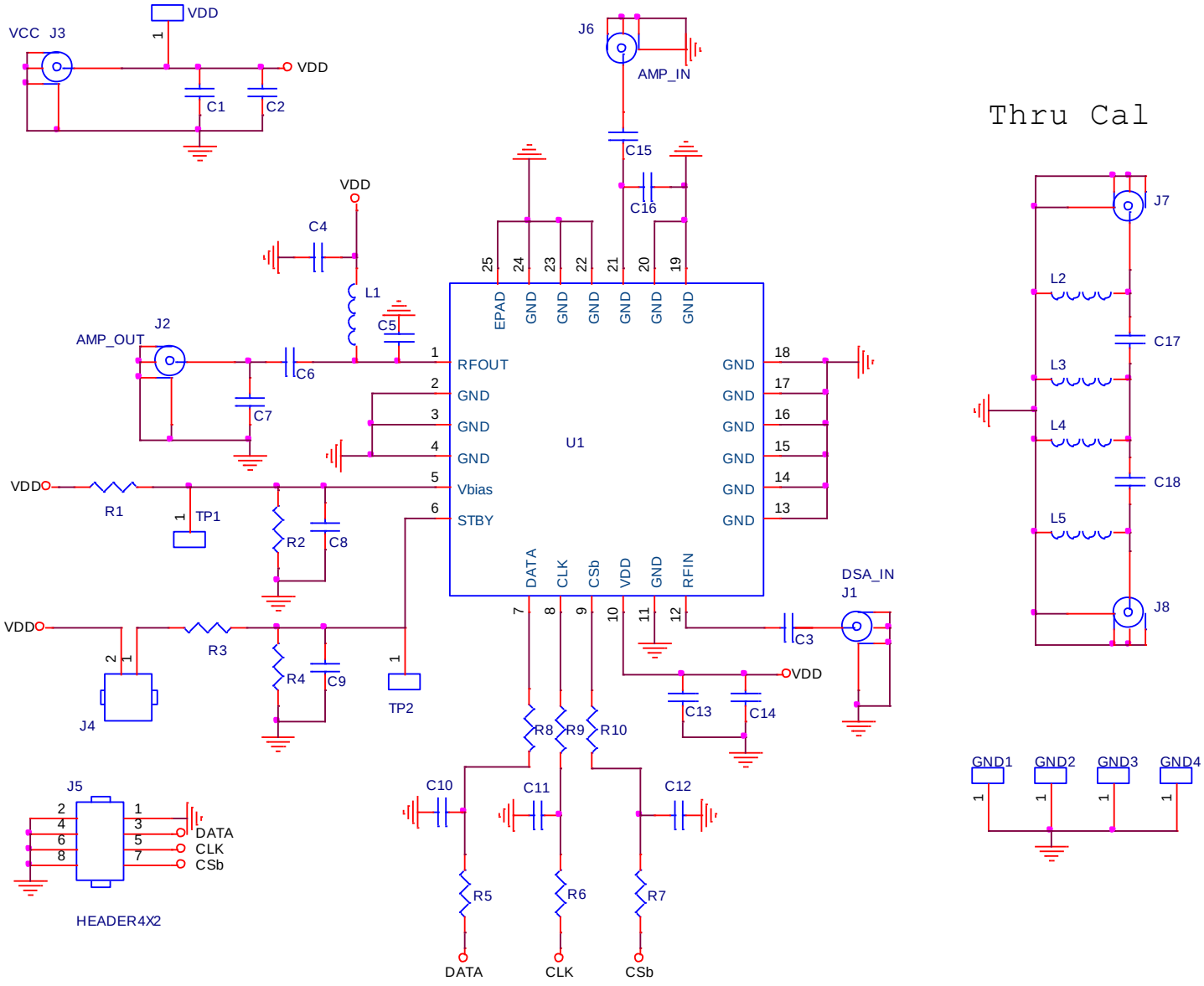


Table 13. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1	1	10µF ± 20%, 16V, X6S Ceramic Capacitor (0603)	GRM188C81C106M	MURATA
C2	1	1µF ± 10%, 16V, X7R Ceramic Capacitor (0603)	GRM188R71C105K	MURATA
C3, C6, C17, C18	4	100pF ± 5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	MURATA
C4	1	0.1µF ±10%, 16V, X7R Ceramic Capacitor (0402)	GRM155R71C104K	MURATA
C5	1	0.5pF ± 0.1pF, 50V, C0G Ceramic Capacitor (0402)	GJM1555C1HR50B	MURATA
C8, C13	2	1000pF ± 5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	MURATA
C10, C11, C12	3	2pF ±0.1pF, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H2R0B	MURATA
C14	1	100nF ± 10%, 50V, X7R Ceramic Capacitor (0402)	GRM155R71H104K	MURATA
R1, R3	2	390Ω ± 1%, 1/10W, Resistor (0402)	ERJ-2RKF3900X	PANASONIC
R5, R6, R7	3	4.7kΩ ± 1%, 1/10W, Resistor (0402)	ERJ-2RKF4701X	PANASONIC
R8, R9, R10	3	0Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
L1	1	100nH ±5%, 0.310A, Fixed Chip Inductor (0402)	0402HPH-R10XJL	COILCRAFT
J1, J2, J7, J8	4	Edge Launch SMA (0.375 inch pitch ground, tab)	142-0701-851	Emerson Johnson
J3	1	Edge Launch SMA (0.250 inch pitch ground, round)	142-0711-821	Emerson Johnson
J4	1	CONN HEADER VERT SGL 2 X 1 POS GOLD	961102-6404-AR	3M
J5	1	CONN HEADER VERT DBL 4 X 2 POS GOLD	67997-108HLF	FCI
U1	1	AMP-DSA	F1431NBGK	IDT
	1	Printed Circuit Board	F1431 EVKIT Rev 01	IDT
C7, C9, C15, C16, R2, R4, J6		DNP		

Evaluation Kit Operation

The F1431B has been optimized for use in high performance RF applications from 0.35GHz to 3.0GHz.

RF Matching and Critical Component Placement

Component placement of the output matching components C5, L1, and C6 is critical (see Figure 41), and these components should be placed as close to pin 1 of the F1431B as possible. IDT recommends the customer seek guidance for board layout. IDT will provide Evaluation Board PCB Gerber files upon request.

STBY

The STBY control pin allows power saving when the device is not in use. Setting the STBY pin to a logic LOW, or leaving the pin open will put the device in Normal Operation Mode. The STBY pin has an internal 400kΩ resistor to ground. Applying logic HIGH to this pin will put the part in Standby Mode. A voltage should not be applied to the STBY pin without V_{DD} present.

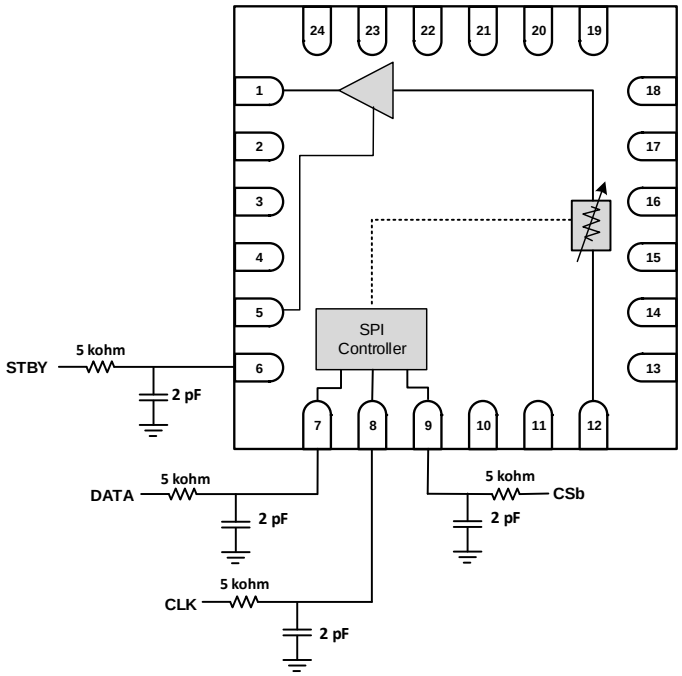
Power Supplies

A common V_{DD} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade the noise figure and fast transients can trigger ESD clamps and cause the clamps to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µs. All control pins should remain at 0V (±0.3V) while the supply voltage ramps up or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the circuit shown in Figure 42 is recommended at the input of each control pin. This applies to all SPI pins and the STBY pin. Note the recommended resistor and capacitor values do not necessarily match the Evaluation Board BOM for the case of poor control signal integrity.

Figure 42. Control Pin Interface



Package Outline Drawings

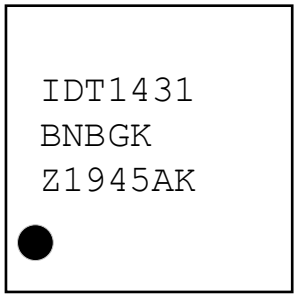
The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

https://www.idt.com/document/psc/nbnbg24-package-outline-40-x-40-mm-bodyepad-270mm-sq-050-mm-pitch-qfn

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F1431BNBGK	4 x 4 x 0.75 mm 24-QFN	1	Tray	-40° to +105°C
F1431BNBGK8	4 x 4 x 0.75 mm 24-QFN	1	Tape and Reel	-40° to +105°C
F1431BEVBK	Evaluation Board			

Marking Diagram

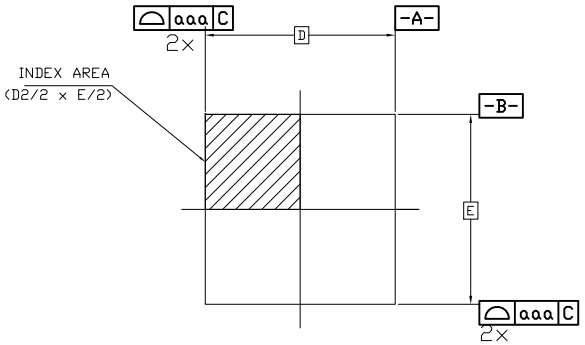


1. Lines 1 and 2 are the part number.
2. Line 3 “Z” is for device assembly stepping.
3. Line 3 “yyww” = “1945” is two digits for the year and two digit week that the part was assembled.
4. Line 3 “AK” denotes the assembly site.

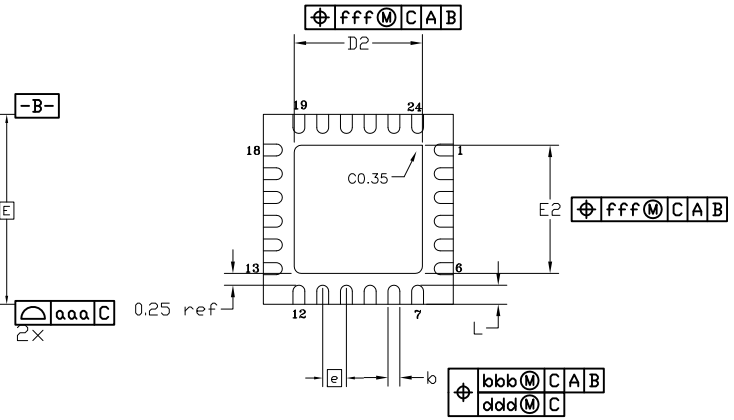
Revision History

Revision Date	Description of Change
April 17, 2020	Initial release.

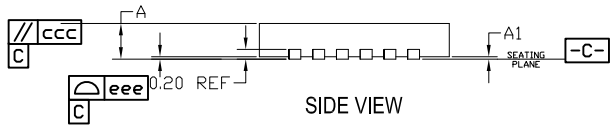
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/11/16	JH



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSION

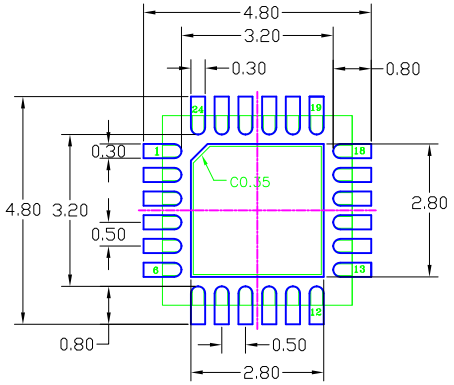
SYMBOL	DIMENSION		
	MIN	NOM	MAX
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
L	0.30	0.40	0.50
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	.20	.25	.30
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

TOLERANCES UNLESS SPECIFIED DECIMAL X± .1 XX± .05 XXX± .030 ANGULAR ±1°		IDT™ www.IDT.com	6024 SILVER CREEK VALLEY ROAD. SAN JOSE, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572
APPROVALS	DATE	TITLE NB/NBG24 PACKAGE OUTLINE 4.0 x 4.0 mm BODY,EPAD 2.70mm SQ 0.50 mm PITCH QFN	
DRAWN RAC	5/11/16		
CHECKED			
		SIZE C / DRAWING No. PSC-4313-03	REV 00
		DO NOT SCALE DRAWING	SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/11/16	JH



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWN FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X± .1 ±1° XX± .05 XXX± .030		IDT™ www.IDT.com	6024 SILVER CREEK VALLEY ROAD. SAN JOSE, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572
APPROVALS	DATE	TITLE NB/NBG24 PACKAGE OUTLINE 4.0 x 4.0 mm BODY,EPAD 2.70mm SQ 0.50 mm PITCH QFN	
DRAWN RAC	5/11/16		
CHECKED			
		SIZE C / DRAWING No. PSC-4313-03	REV 00
		DO NOT SCALE DRAWING	SHEET 2 OF 2

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.