

LM290xLV-Q1 工业标准、低电压车用运算放大器

1 特性

- 适用于成本敏感型系统的业界通用放大器
- 低输入失调电压： $\pm 1\text{mV}$
- 共模电压范围包括接地
- 单位带宽增益积： 1MHz
- 低宽带噪声： $40\text{nV}/\sqrt{\text{Hz}}$
- 低静态电流： $90\mu\text{A}/\text{通道}$
- 单位增益稳定
- 可在 2.7V 至 5.5V 的电源电压下运行
- 提供双通道和四通道型号
- 严格的 ESD 规格： 2kV HBM、 1kV CDM
- 扩展工作温度范围： -40°C 至 125°C

2 应用

- 针对 AEC-Q100 1 级应用进行了优化
- 信息娱乐系统与仪表组
- 被动安全
- 车身电子装置和照明
- 混合动力汽车/电动汽车逆变器和电机控制
- 车载充电器 (OBC) 和无线充电器
- 动力总成电流传感器
- 高级驾驶辅助系统 (ADAS)
- 单电源、低侧、单向电流感应电路

3 说明

LM290xLV-Q1 系列包括双路 LM2904LV-Q1 和四路 LM2902LV-Q1 运算放大器。这些器件可在 2.7V 至 5.5V 的电源电压范围下工作。

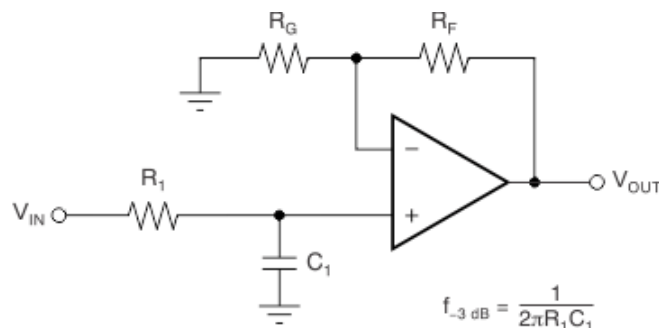
在对成本敏感的低压应用中，这些运算放大器可作为 LM2904-Q1 和 LM2902-Q1 的替代产品。LM290xLV-Q1 器件可在低电压下可提供比 LM290x-Q1 器件更佳的性能，并且功耗更低。这些运算放大器具有单位增益稳定性，并且在过驱情况下不会出现相位反转。ESD 设计为 LM290xLV-Q1 系列提供 2kV 的 HBM 规格。

LM290xLV-Q1 系列采用业界通用封装。可用的封装包括 SOIC、VSSOP 和 TSSOP 封装。

器件信息

器件型号 (1)	封装	封装尺寸 (标称值)
LM2902LV-Q1	SOIC (14)	$8.65\text{mm} \times 3.91\text{mm}$
	TSSOP (14)	$4.40\text{mm} \times 5.00\text{mm}$
	SOT23 (14)	$4.20\text{mm} \times 1.90\text{mm}$
LM2904LV-Q1	SOIC (8)	$3.91\text{mm} \times 4.90\text{mm}$
	VSSOP (8)	$3.00\text{mm} \times 3.00\text{mm}$

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1C_1}\right)$$

单极低通滤波器



Table of Contents

1 特性	1	8 Application and Implementation	16
2 应用	1	8.1 Application Information.....	16
3 说明	1	8.2 Typical Application.....	16
4 Revision History	2	9 Power Supply Recommendations	18
5 Pin Configuration and Functions	3	9.1 Input and ESD Protection.....	18
6 Specifications	5	10 Layout	19
6.1 Absolute Maximum Ratings.....	5	10.1 Layout Guidelines.....	19
6.2 ESD Ratings.....	5	10.2 Layout Example.....	19
6.3 Recommended Operating Conditions.....	5	11 Device and Documentation Support	21
6.4 Thermal Information: LM2904LV-Q1.....	5	11.1 Documentation Support.....	21
6.5 Thermal Information: LM2902LV-Q1.....	6	11.2 Related Links.....	21
6.6 Electrical Characteristics.....	7	11.3 接收文档更新通知.....	21
6.7 Typical Characteristics.....	9	11.4 支持资源.....	21
7 Detailed Description	14	11.5 Trademarks.....	21
7.1 Overview.....	14	11.6 Electrostatic Discharge Caution.....	21
7.2 Functional Block Diagram.....	14	11.7 术语表.....	21
7.3 Feature Description.....	14	12 Mechanical, Packaging, and Orderable Information	22
7.4 Device Functional Modes.....	15		

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (April 2021) to Revision B (October 2021)	Page
• 删除了器件信息表中 TSSOP (14) 和 SOT-23 (14) 封装的预发布说明.....	1
• Updated PW package thermal information in <i>Thermal Information: LM2902LV-Q1</i> table.....	6
Changes from Revision * (August 2020) to Revision A (April 2021)	Page
• 删除了器件信息表中 TSSOP (8) 封装信息。.....	1
• 删除了器件信息表中 VSSOP (8) 封装信息的预发布说明。.....	1
• Deleted PW package from <i>Pin Configuration and Functions</i> section.....	3
• Added note 5 to the differential input voltage in <i>Absolute Maximum Ratings</i> table	5
• Updated DGK package thermal information in <i>Thermal Information: LM2904LV-Q1</i> table.....	5
• Updated DYY package thermal information in <i>Thermal Information: LM2902LV-Q1</i> table.....	6

5 Pin Configuration and Functions

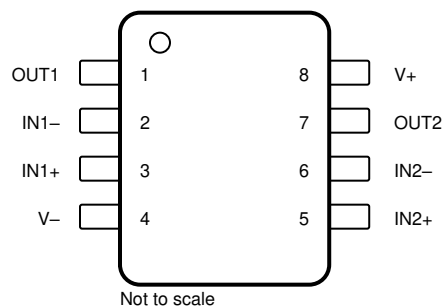
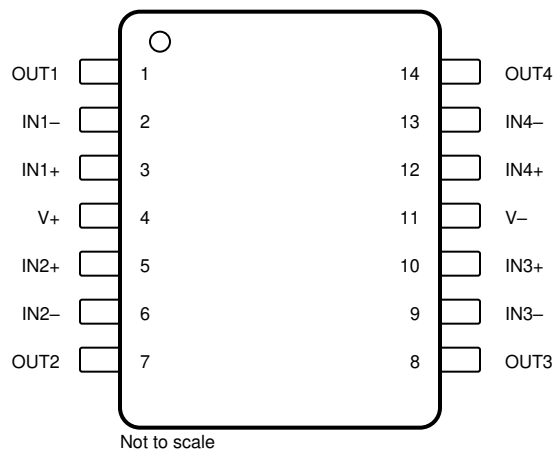


图 5-1. LM2904LV-Q1 D and DGK Packages
8-Pin SOIC and VSSOP
Top View

表 5-1. Pin Functions: LM2904LV-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1 -	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2 -	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V -	4	—	Negative (low) supply or ground (for single-supply operation)
V+	8	—	Positive (high) supply



**图 5-2. LM2902LV-Q1 D, PW, DYY Packages
14-Pin SOIC, TSSOP, SOT-23
Top View**

表 5-2. Pin Functions: LM2902LV-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1 -	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2 -	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3 -	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4 -	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V -	11	—	Negative (low) supply or ground (for single-supply operation)
V+	4	—	Positive (high) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Supply voltage, ([V+] - [V -])			0	6	V
Signal input pins	Voltage ⁽²⁾	Common-mode	(V -) - 0.5	(V+) + 0.5	V
		Differential ⁽⁵⁾	(V+) - (V -) + 0.2		V
	Current ⁽²⁾		- 10	10	mA
Output short-circuit ^{(3) (4)}			Continuous		
Operating, T _A			- 55	125	°C
Operating junction temperature, T _J				150	°C
Storage temperature, T _{stg}			- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.
- (4) Long term continuous current limit is determined by electromigration limits
- (5) Differential input voltages greater than 0.5 V applied continuously can result in a shift to the input offset voltage above the maximum specification of this parameter. The magnitude of this effect increases as the ambient operating temperature rises.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _S	Supply voltage [(V+) - (V-)]		2.7	5.5	V
V _{CM}	Input-pin voltage range		(V-) - 0.1	(V+) - 1	V
T _A	Specified temperature		- 40	125	°C

6.4 Thermal Information: LM2904LV-Q1

THERMAL METRIC ⁽¹⁾		LM2904LV-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	151.9	196.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	92.0	86.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	95.4	118.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	40.2	23.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	94.7	116.7	°C/W

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

6.5 Thermal Information: LM2902LV-Q1

THERMAL METRIC ⁽¹⁾	LM2902LV-Q1			UNIT
	D (SOIC)	DYY (SOT-23)	PW (TSSOP)	
	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	115.1	154.3	135.3	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	71.2	86.8	63.5	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	71.1	67.9	78.4	°C/W
ψ_{JT} Junction-to-top characterization parameter	29.6	10.1	13.6	°C/W
ψ_{JB} Junction-to-board characterization parameter	70.7	67.5	77.9	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

6.6 Electrical Characteristics

For $V_S = (V_+) - (V_-) = 2.7\text{ V to }5.5\text{ V}$ ($\pm 1.35\text{ V to } \pm 2.75\text{ V}$), $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, and $V_{CM} = V_{OUT} = V_S / 2$ (unless otherwise noted)

PARAMETER ⁽¹⁾		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V _{OS}	Input offset voltage	V _S = 5 V		±1	±3	mV
		V _S = 5 V, T _A = - 40°C to 125°C			±5	
dV _{OS} /dT	V _{OS} vs temperature	T _A = - 40°C to 125°C		±4		μV/°C
PSRR	Power-supply rejection ratio	V _S = 2.7 V to 5.5 V, V _{CM} = (V -)	80	100		dB
INPUT VOLTAGE RANGE						
V _{CM}	Common-mode voltage range	No phase reversal	(V -) - 0.1		(V+) - 1	V
CMRR	Common-mode rejection ratio	V _S = 2.7 V, (V -) - 0.1 V < V _{CM} < (V+) - 1 V T _A = - 40°C to 125°C		84		dB
		V _S = 5.5 V, (V -) - 0.1 V < V _{CM} < (V+) - 1 V T _A = - 40°C to 125°C	63	92		
INPUT BIAS CURRENT						
I _B	Input bias current	V _S = 5 V		±15		pA
I _{OS}	Input offset current			±5		pA
NOISE						
E _n	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz, V _S = 5 V		5.1		μV _{PP}
e _n	Input voltage noise density	f = 1 kHz, V _S = 5 V		40		nV/ √ Hz
INPUT CAPACITANCE						
C _{ID}	Differential			2		pF
C _{IC}	Common-mode			5.5		pF
OPEN-LOOP GAIN						
A _{OL}	Open-loop voltage gain	V _S = 2.7 V, (V -) + 0.15 V < V _O < (V+) - 0.15 V, R _L = 2 k Ω		110		dB
		V _S = 5.5 V, (V -) + 0.15 V < V _O < (V+) - 0.15 V, R _L = 2 k Ω		125		
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V _S = 5 V		1		MHz
ϕ _m	Phase margin	V _S = 5.5 V, G = +1		75		°
SR	Slew rate	V _S = 5 V, G = +1		1.5		V/μs
t _S	Settling time	To 0.1%, V _S = 5 V, 2-V step, G = 1, C _L = 100 pF		4		μs
		To 0.01%, V _S = 5 V, 2-V step, G = 1, C _L = 100 pF		5		
t _{OR}	Overload recovery time	V _S = 5 V, V _{IN} × gain > V _S		1		μs
THD+N	Total harmonic distortion + noise	V _S = 5.5 V, V _{CM} = 2.5 V, V _O = 1 V _{RMS} , G = 1, f = 1 kHz, 80-kHz measurement BW		0.005%		
OUTPUT						
V _{OH}	Voltage output swing from positive supply	R _L ≥ 2 k Ω, T _A = - 40°C to 125°C		1		V
V _{OL}	Voltage output swing from negative supply	R _L ≤ 10 k Ω, T _A = - 40°C to 125°C		40	75	mV
I _{SC}	Short-circuit current	V _S = 5.5 V		±40		mA
Z _O	Open-loop output impedance	V _S = 5 V, f = 1 MHz		1200		Ω

6.6 Electrical Characteristics (continued)

For $V_S = (V^+) - (V^-) = 2.7\text{ V to } 5.5\text{ V}$ ($\pm 1.35\text{ V to } \pm 2.75\text{ V}$), $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, and $V_{CM} = V_{OUT} = V_S / 2$ (unless otherwise noted)

PARAMETER ⁽¹⁾		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Specified voltage range		2.7 (± 1.35)		5.5 (± 2.75)	V
I_Q	Quiescent current per amplifier	$I_O = 0\text{ mA}$, $V_S = 5.5\text{ V}$		90	150	μA
		$I_O = 0\text{ mA}$, $V_S = 5.5\text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$			160	

(1) Overtemperature limits are assured by characterization.

6.7 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

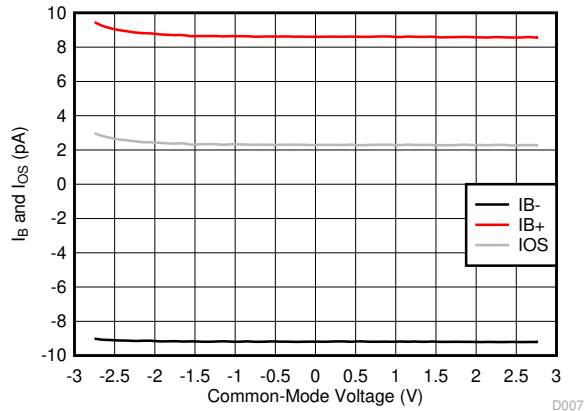


图 6-1. I_B and I_{OS} vs Common-Mode Voltage

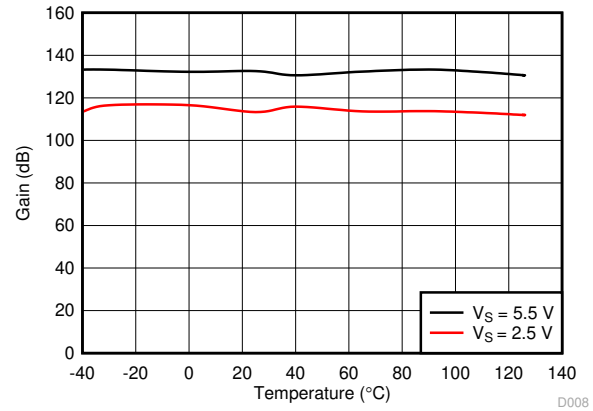


图 6-2. Open-Loop Gain vs Temperature

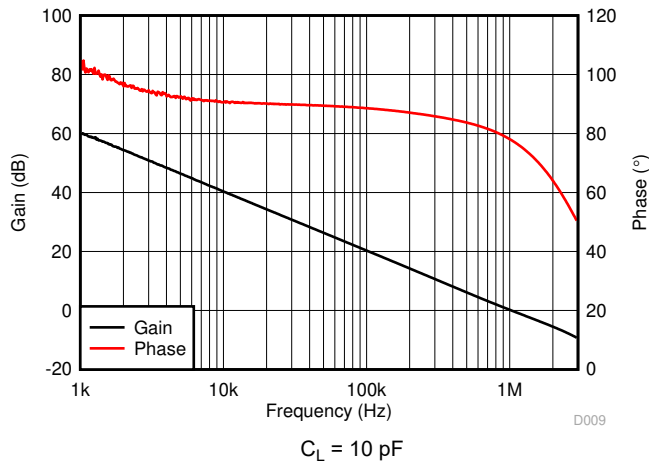


图 6-3. Open-Loop Gain and Phase vs Frequency

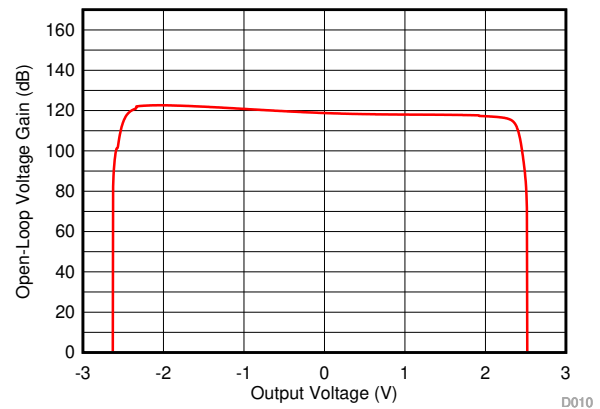


图 6-4. Open-Loop Gain vs Output Voltage

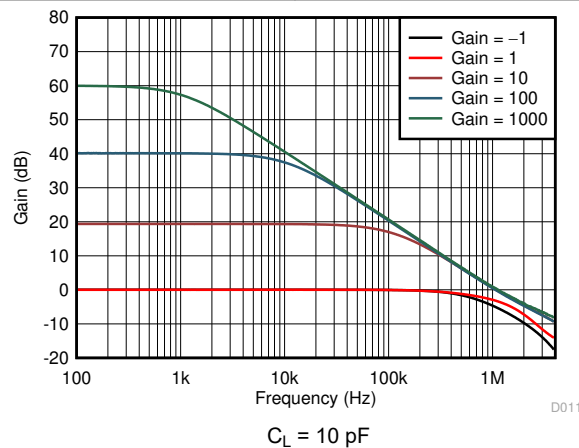


图 6-5. Closed-Loop Gain vs Frequency

6.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

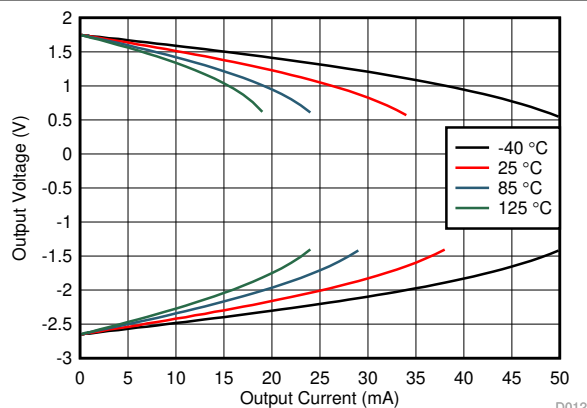


图 6-6. Output Voltage vs Output Current (Claw)

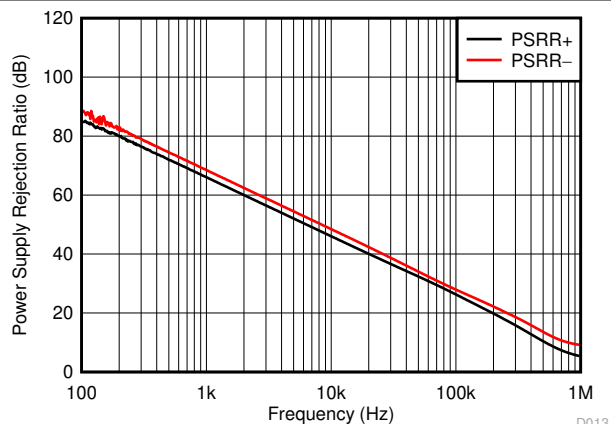


图 6-7. PSRR vs Frequency

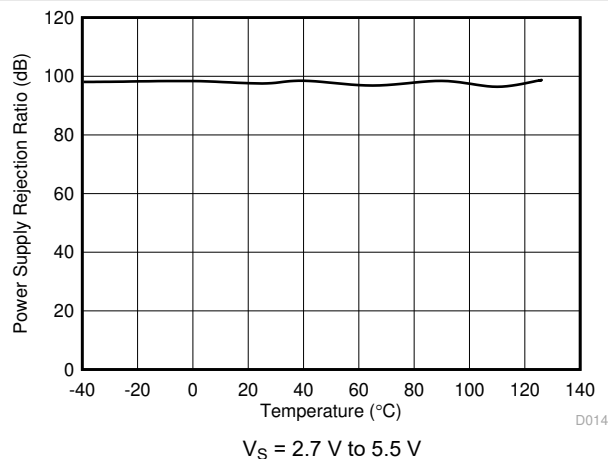


图 6-8. DC PSRR vs Temperature

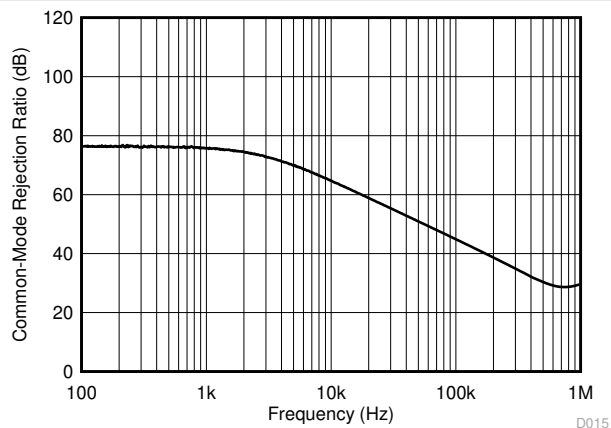


图 6-9. CMRR vs Frequency

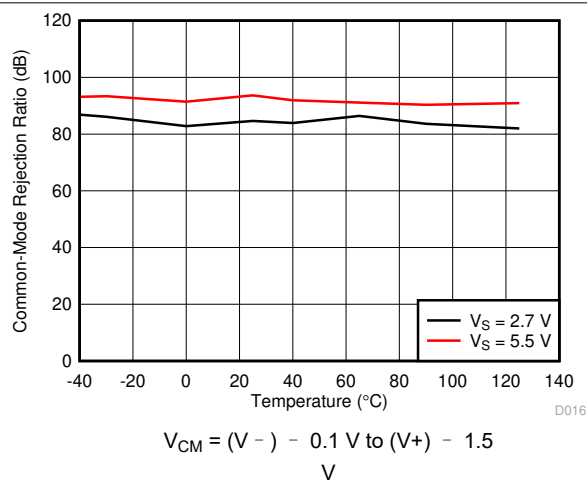


图 6-10. DC CMRR vs Temperature

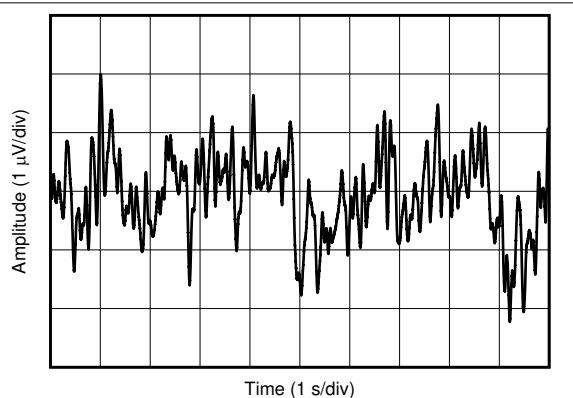


图 6-11. 0.1-Hz to 10-Hz Integrated Voltage Noise

6.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

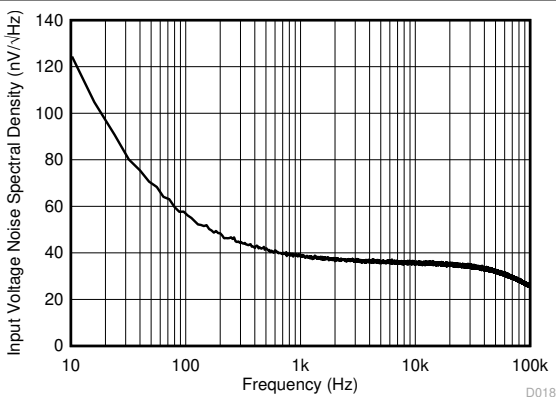


图 6-12. Input Voltage Noise Spectral Density

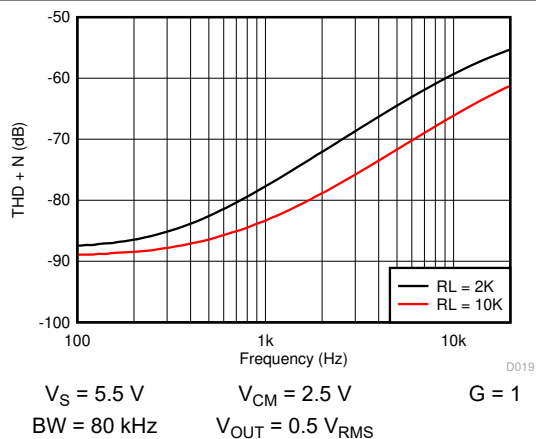


图 6-13. THD + N vs Frequency

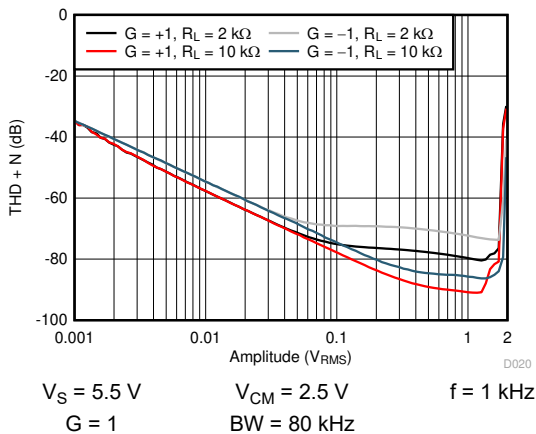


图 6-14. THD + N vs Amplitude

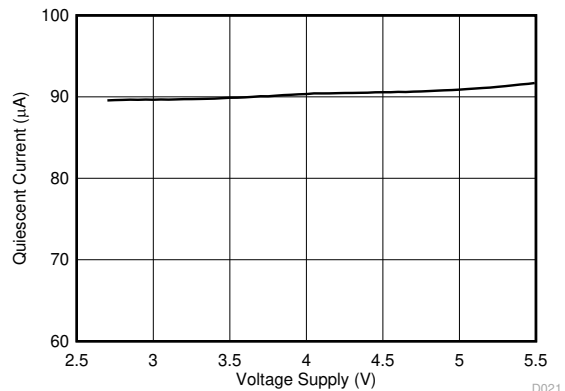


图 6-15. Quiescent Current vs Supply Voltage

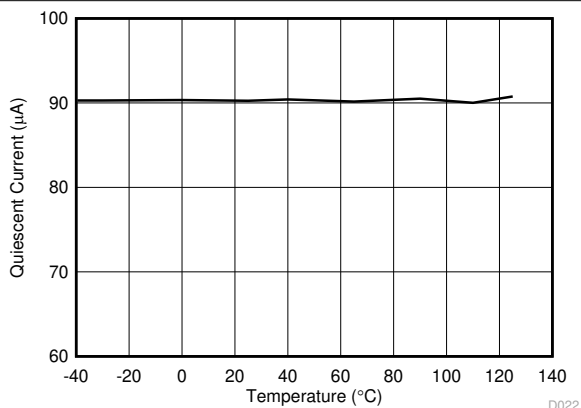


图 6-16. Quiescent Current vs Temperature

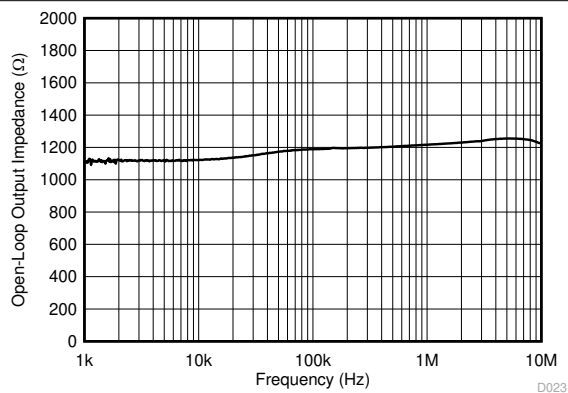


图 6-17. Open-Loop Output Impedance vs Frequency

6.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

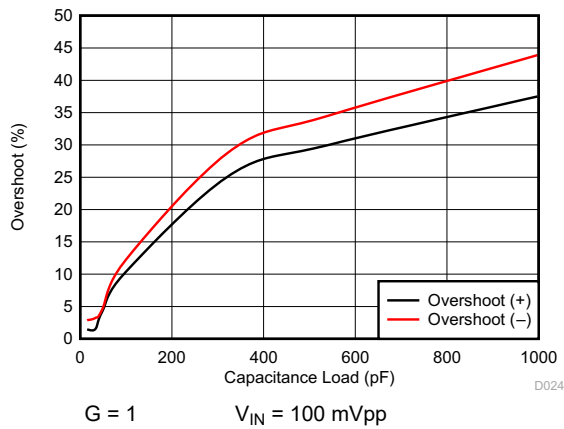


图 6-18. Small Signal Overshoot vs Capacitive Load

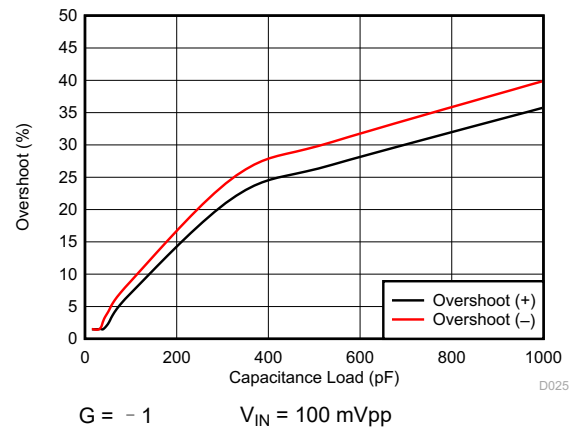


图 6-19. Small Signal Overshoot vs Capacitive Load

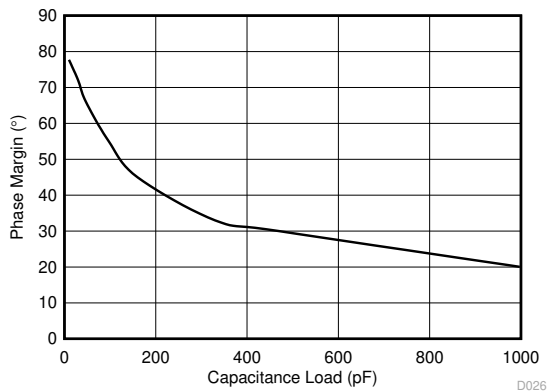


图 6-20. Phase Margin vs Capacitive Load

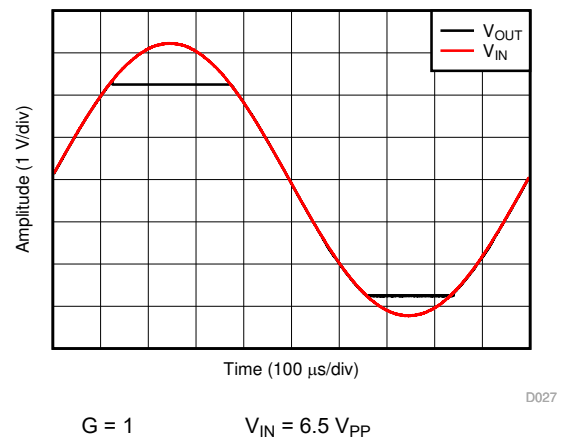


图 6-21. No Phase Reversal

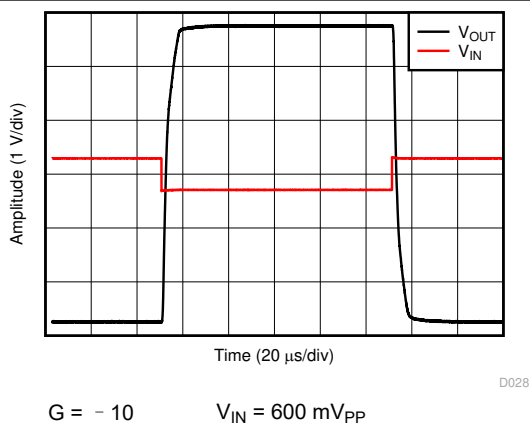


图 6-22. Overload Recovery

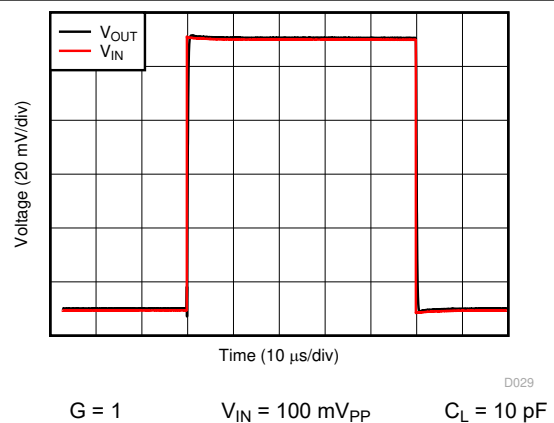


图 6-23. Small-Signal Step Response

6.7 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_+ = 2.75\text{ V}$, $V_- = -2.75\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

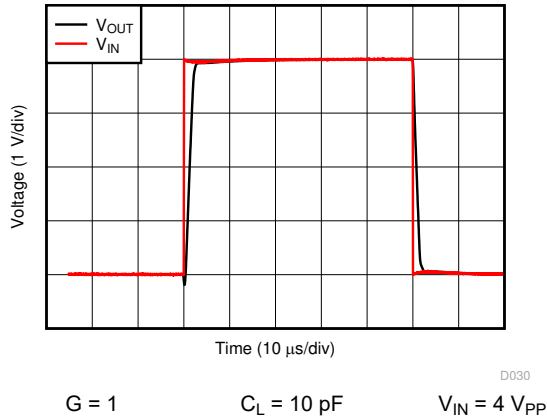


图 6-24. Large-Signal Step Response

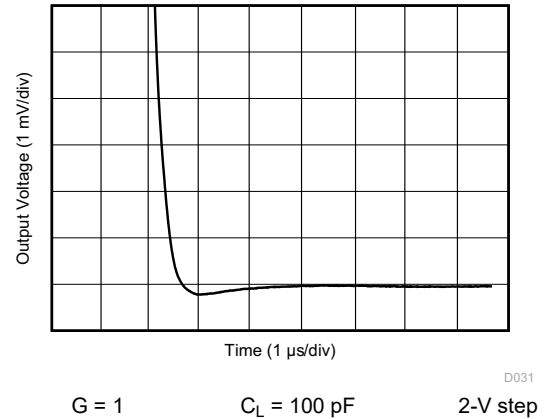


图 6-25. Large-Signal Settling Time (Negative)

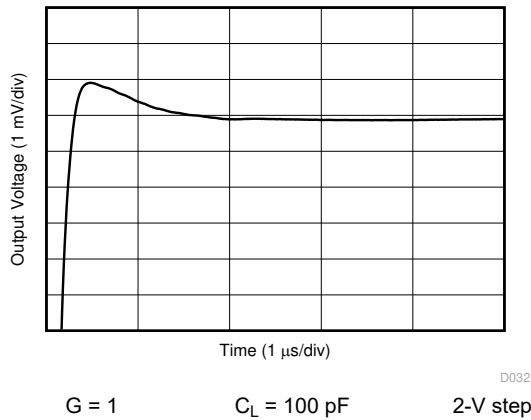


图 6-26. Large-Signal Settling Time (Positive)

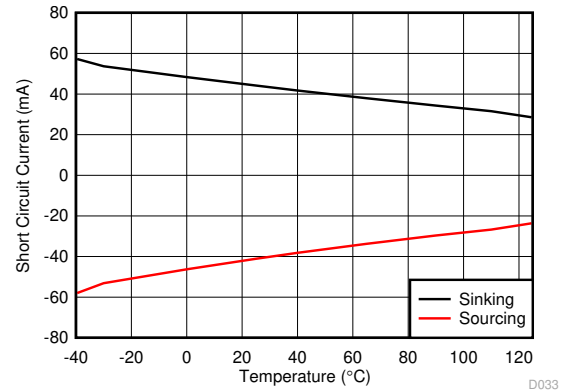


图 6-27. Short-Circuit Current vs Temperature

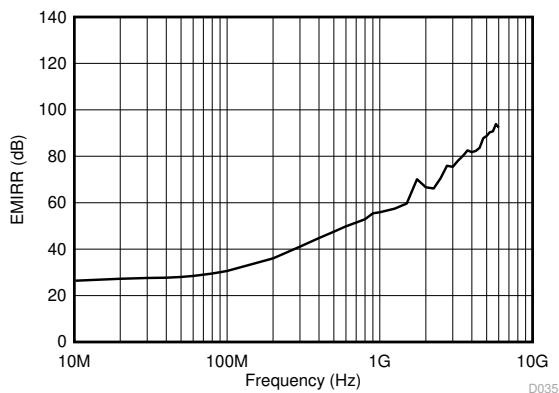


图 6-28. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

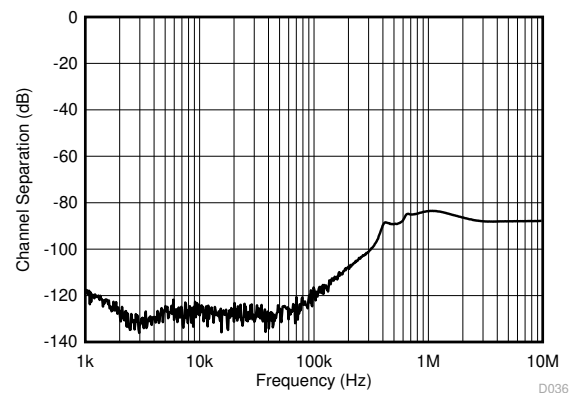


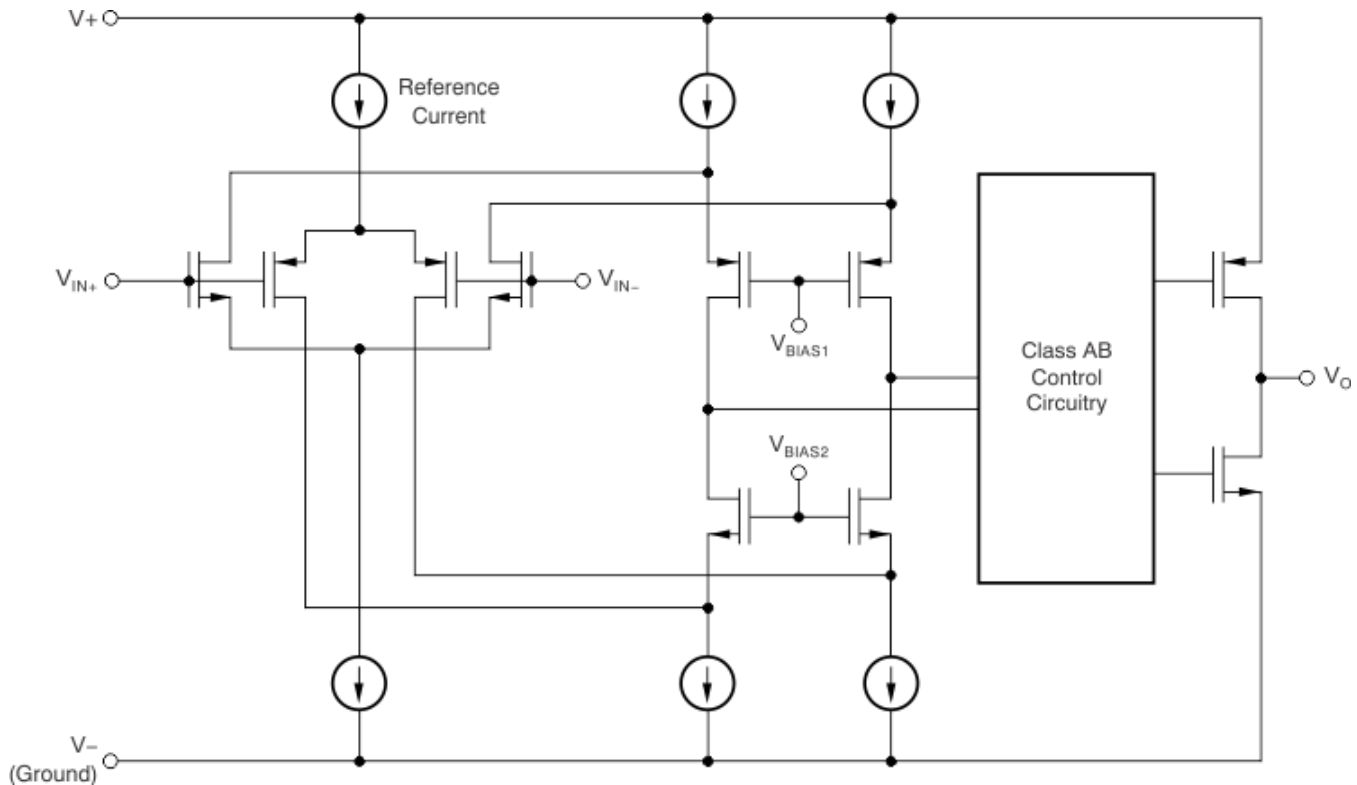
图 6-29. Channel Separation

7 Detailed Description

7.1 Overview

The LM290xLV-Q1 family of low-power op amps is intended for cost-optimized systems. These devices operate from 2.7 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose automotive applications. The input common-mode voltage range includes the negative rail and allows the LM290xLV-Q1 family to be used in many single-supply applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The LM290xLV-Q1 family of op amps is specified for operation from 2.7 V to 5.5 V. In addition, many specifications apply from -40°C to 125°C . Parameters that vary significantly with operating voltages or temperature are shown in the [Electrical Characteristics](#) section.

7.3.2 Common-Mode Input Range Includes Ground

The input common-mode voltage range of the LM290xLV-Q1 family extends to the negative supply rail and within 1 V below the positive rail for the full supply voltage range of 2.7 V to 5.5 V. This performance is achieved with a P-channel differential pair, as shown in the [Functional Block Diagram](#). Additionally, a complementary N-channel differential pair has been included in parallel to eliminate issues with phase reversal that are common with previous generations of op amps. However, the N-channel pair is not optimized for operation, and significant performance degradation occurs while this pair is operational. TI recommends limiting any voltage applied at the inputs to at least 1 V below the positive supply rail ($V+$) to ensure that the op amp conforms to the specifications detailed in the [Electrical Characteristics](#) section.

7.3.3 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output transistors of the operational amplifier enter a saturation region when the output voltage exceeds the specified output voltage swing, because of the high input voltage or the high gain.

After the device enters the saturation region, the charge carriers in the output transistors require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the LM290xLV-Q1 family is typically 1 μ s.

7.3.4 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can also involve the supply voltage pins. Each of these different pin functions has electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 图 7-1 shows the ESD circuits contained in the LM290xLV-Q1. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

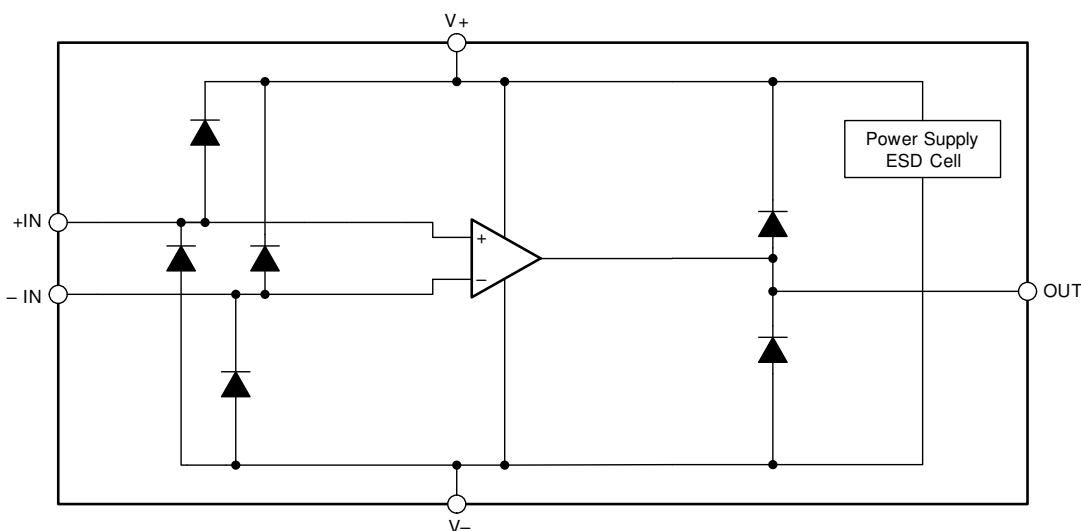


图 7-1. Equivalent Internal ESD Circuitry

7.3.5 EMI Susceptibility and Input Filtering

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The 图 6-28 plot illustrates the performance of the LM290xLV-Q1 family's EMI filters across a wide range of frequencies. For more detailed information, see [EMI Rejection Ratio of Operational Amplifiers](#) available for download from www.ti.com.

7.4 Device Functional Modes

The LM290xLV-Q1 family has a single functional mode. The devices are powered on as long as the power-supply voltage is between 2.7 V (± 1.35 V) and 5.5 V (± 2.75 V).

8 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The LM290xLV-Q1 devices are a family of low-power, cost-optimized operational amplifiers. The devices operate from 2.7 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose automotive applications. The input common-mode voltage range includes the negative rail, and allows the LM290xLV-Q1 to be used in any single-supply applications.

8.2 Typical Application

图 8-1 shows the LM290xLV-Q1 device configured in a low-side current sensing application.

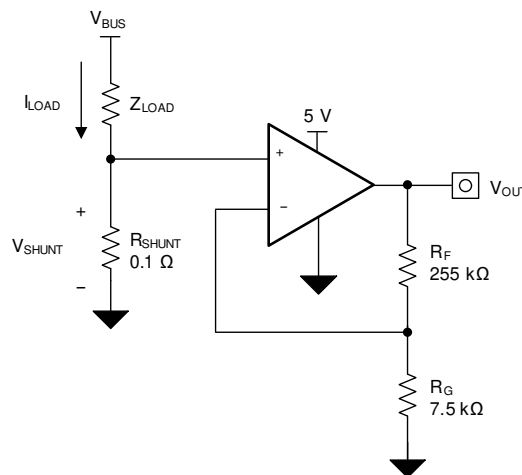


图 8-1. LM290xLV-Q1 Device in a Low-Side, Current-Sensing Application

8.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 3.5 V
- Maximum shunt voltage: 100 mV

8.2.2 Detailed Design Procedure

The transfer function of the circuit in 图 8-1 is given in 方程式 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest allowable shunt resistor is shown using Equation 2:

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100\text{mV}}{1\text{A}} = 100\text{m}\Omega \quad (2)$$

Using Equation 2, R_{SHUNT} is calculated to be $100\text{ m}\Omega$. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the LM290xLV-Q1 device to produce an output voltage of approximately 0 V to 3.5 V. The gain needed by the LM290xLV-Q1 to produce the necessary output voltage is calculated using Equation 3:

$$\text{Gain} = \frac{(V_{OUT_MAX} - V_{OUT_MIN})}{(V_{IN_MAX} - V_{IN_MIN})} \quad (3)$$

Using Equation 3, the required gain is calculated to be 35 V/V, which is set with resistors R_F and R_G . Equation 4 sizes the resistors R_F and R_G , to set the gain of the LM290xLV-Q1 device to 35 V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

8.2.3 Application Curve

Selecting R_F as $255\text{ k}\Omega$ and R_G as $7.5\text{ k}\Omega$ provides a combination that equals 35 V/V. 图 8-2 shows the measured transfer function of the circuit shown in 图 8-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system, you must choose an impedance that is ideal for your system parameters.

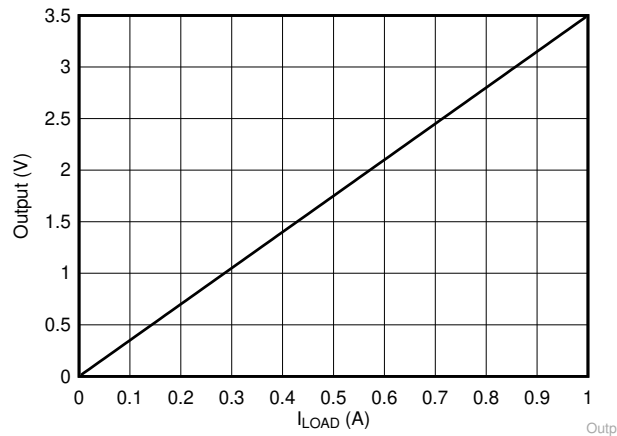


图 8-2. Low-Side, Current-Sense Transfer Function

9 Power Supply Recommendations

The LM290xLV-Q1 family is specified for operation from 2.7 V to 5.5 V (± 1.35 V to ± 2.75 V); many specifications apply from -40°C to 125°C . The [Electrical Characteristics](#) section presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V may permanently damage the device; see the [Absolute Maximum Ratings](#) section.

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout Guidelines](#) section.

9.1 Input and ESD Protection

The LM290xLV-Q1 family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as stated in the [Absolute Maximum Ratings](#) section. 图 9-1 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

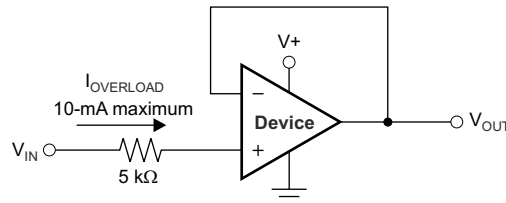


图 9-1. Input Current Protection

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds. Use thermal signatures or EMI measurement techniques to determine where the majority of the ground current is flowing and be sure to route this path away from sensitive analog circuitry.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90° angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in 图 10-2. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

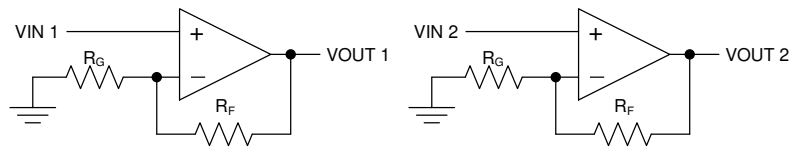


图 10-1. Schematic Representation

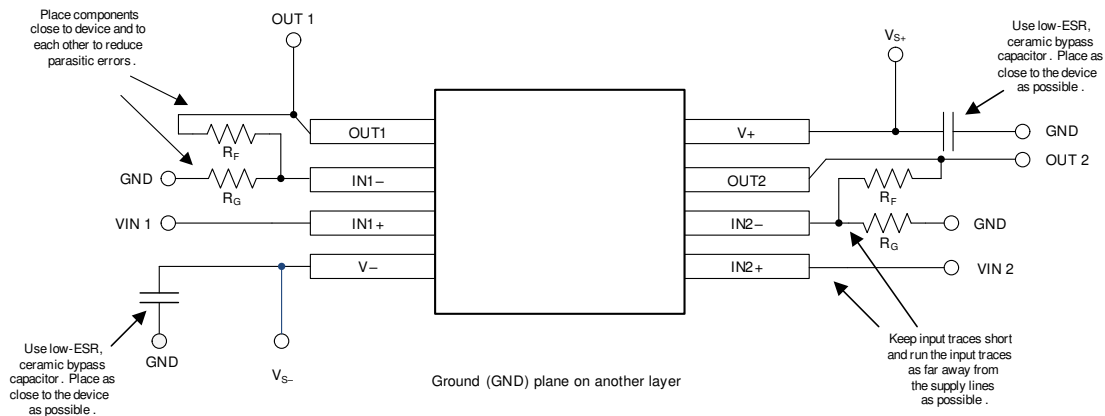


图 10-2. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers](#)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM2902LV-Q1	Click here	Click here	Click here	Click here	Click here
LM2904LV-Q1	Click here	Click here	Click here	Click here	Click here

11.3 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM2902LVQDRQ1	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM2902Q
LM2902LVQDRQ1.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM2902Q
LM2902LVQDYRQ1	Active	Production	SOT-23-THIN (DYY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902Q
LM2902LVQDYRQ1.A	Active	Production	SOT-23-THIN (DYY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902Q
LM2902LVQPWRQ1	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902
LM2902LVQPWRQ1.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902
LM2904LVQDGKRQ1	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27ET
LM2904LVQDGKRQ1.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27ET
LM2904LVQDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904Q
LM2904LVQDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2904Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

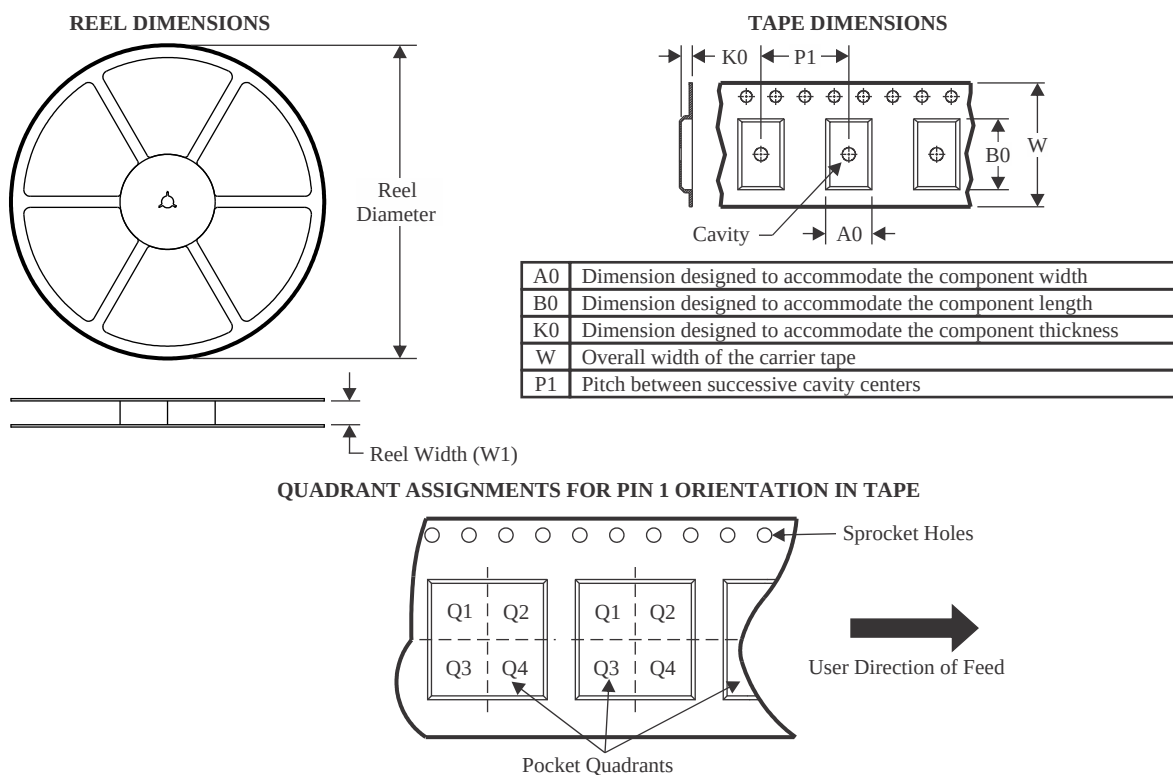
OTHER QUALIFIED VERSIONS OF LM2902LV-Q1, LM2904LV-Q1 :

- Catalog : [LM2902LV](#), [LM2904LV](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

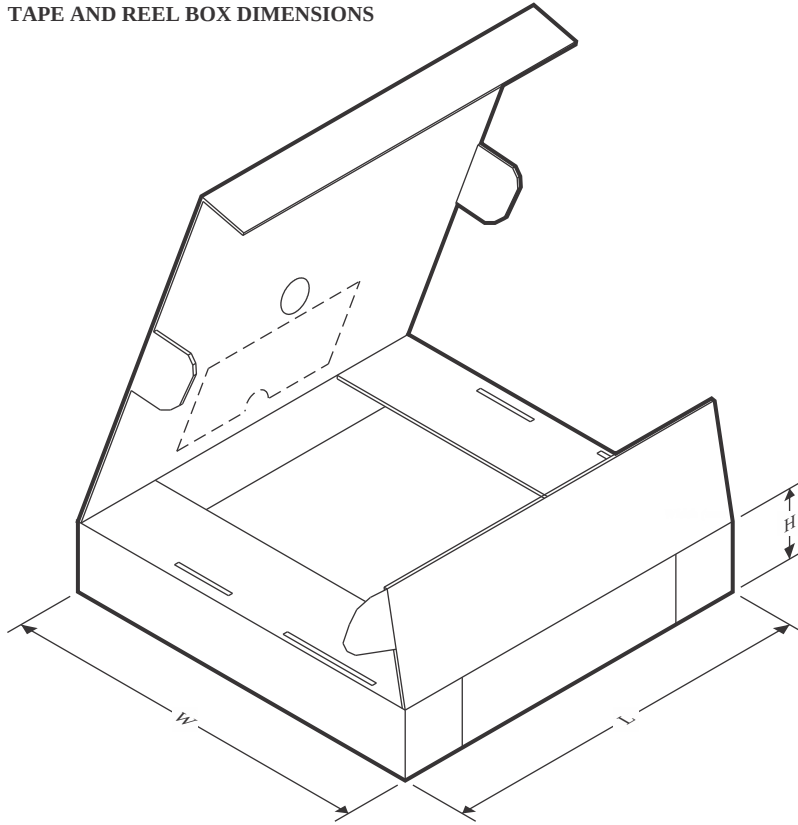
TAPE AND REEL INFORMATION



*All dimensions are nominal

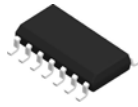
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2902LVQDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902LVQDYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
LM2902LVQPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2904LVQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2904LVQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
LM2904LVQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

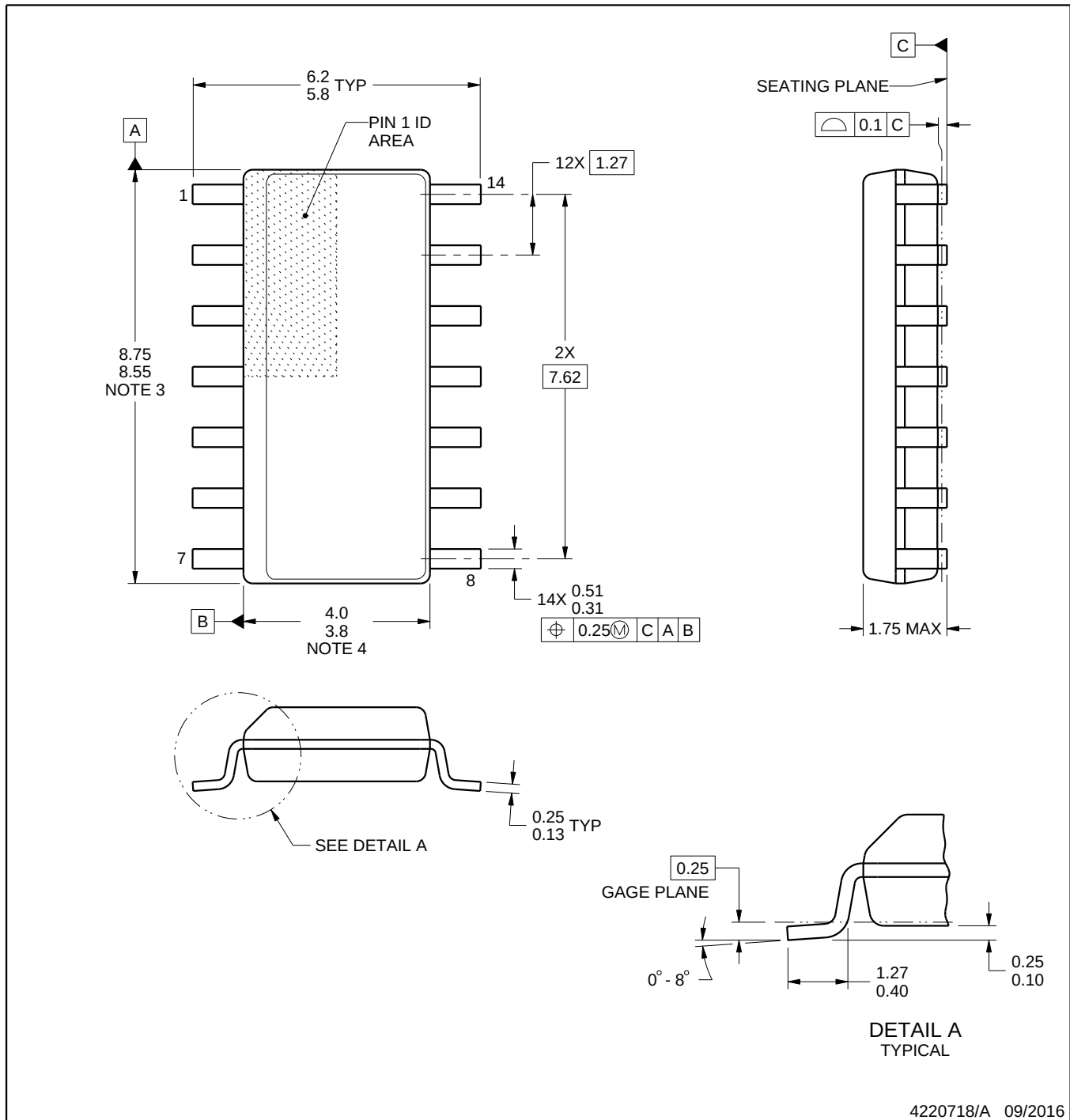


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2902LVQDRQ1	SOIC	D	14	2500	356.0	356.0	35.0
LM2902LVQDYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
LM2902LVQPWRQ1	TSSOP	PW	14	3000	356.0	356.0	35.0
LM2904LVQDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
LM2904LVQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2904LVQDRQ1	SOIC	D	8	2500	356.0	356.0	35.0

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

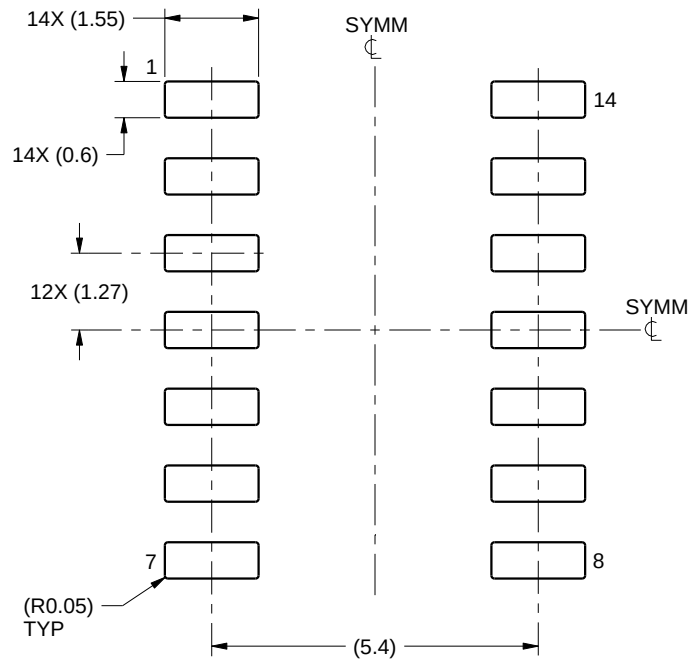
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

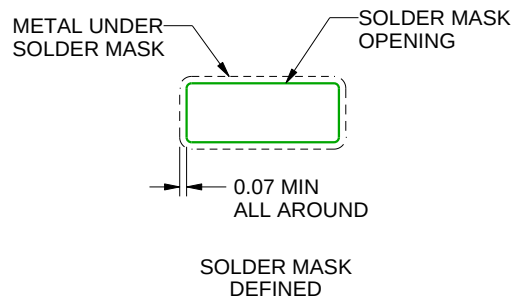
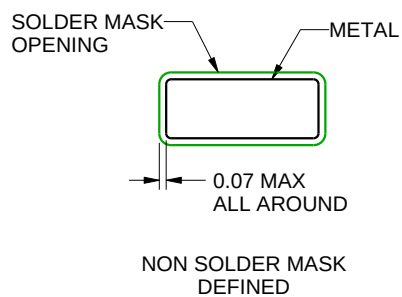
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

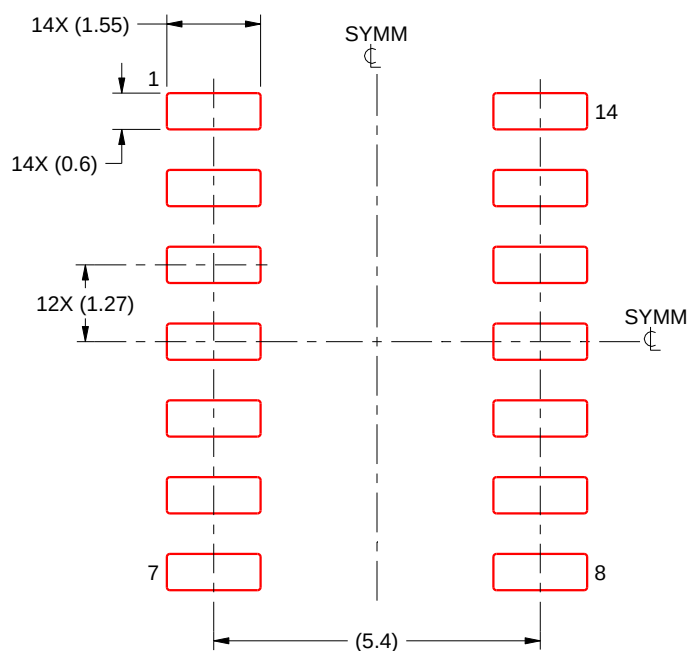
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



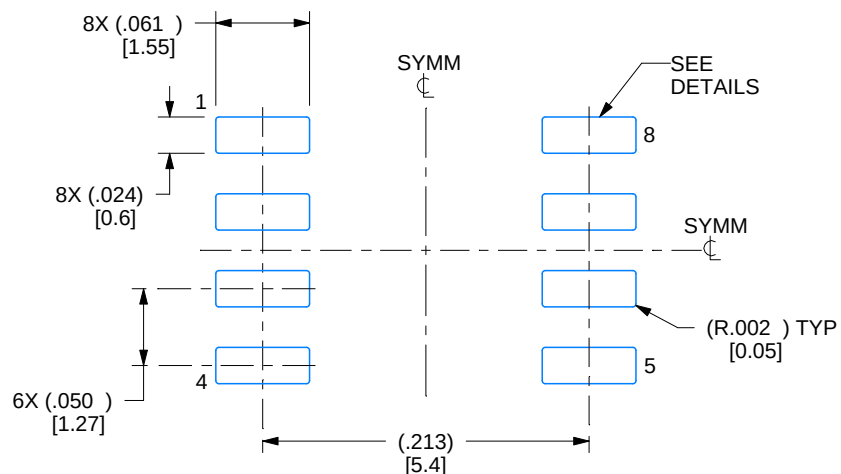
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

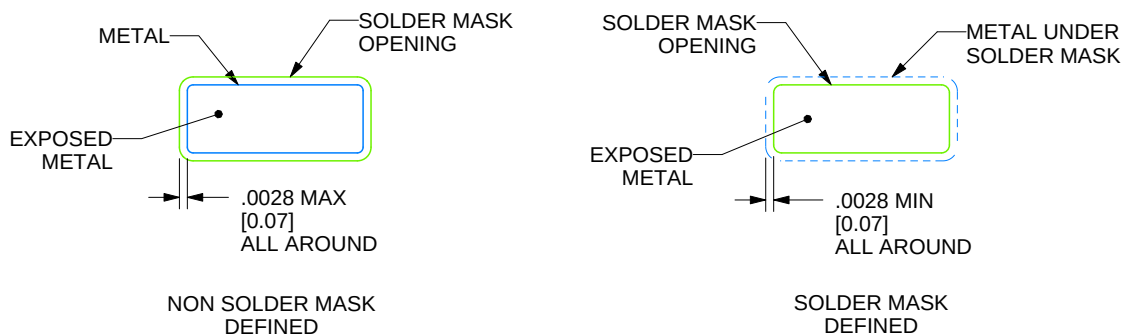
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

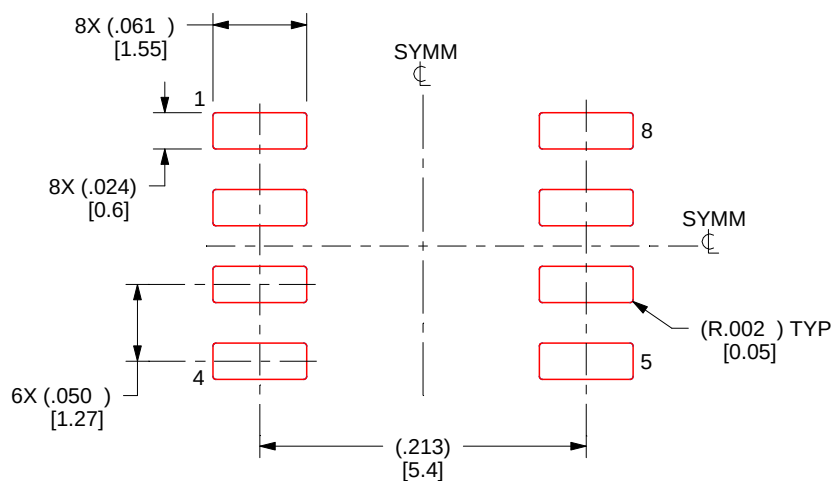
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

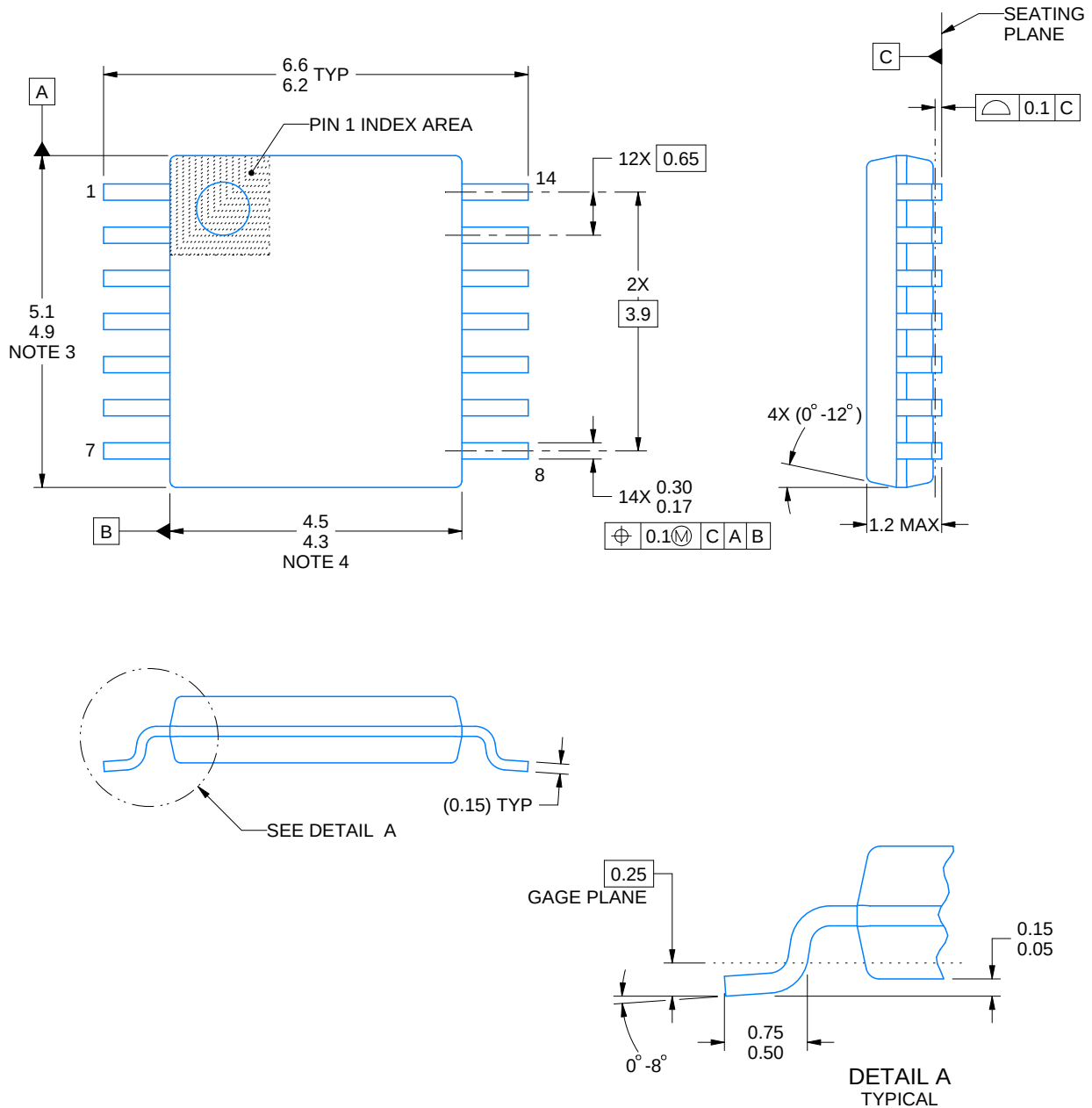
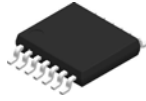


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

NOTES:

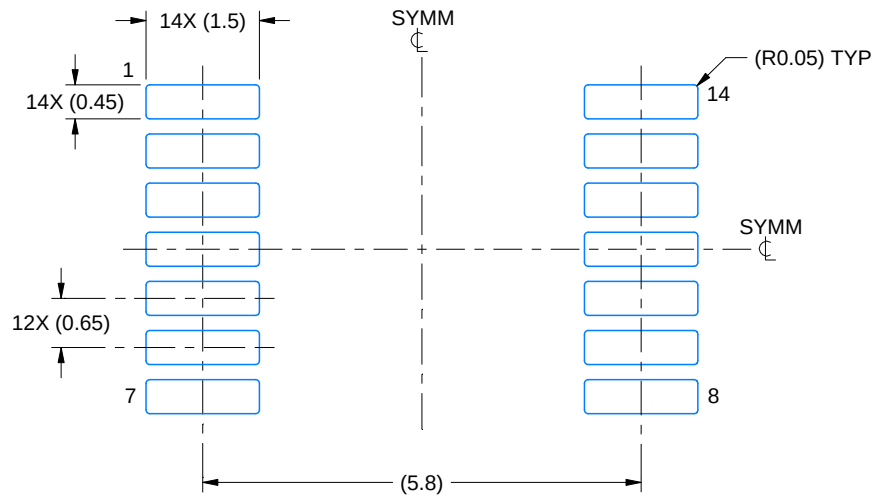
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

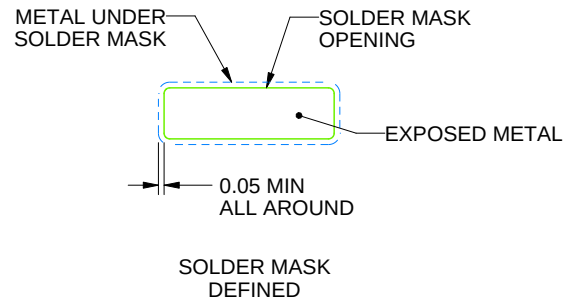
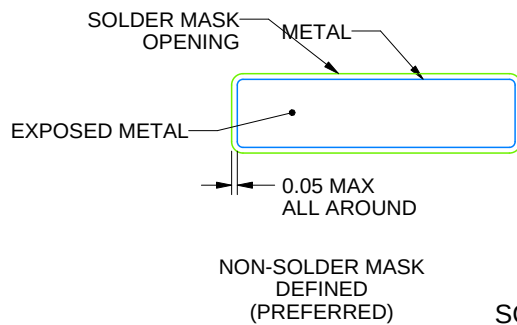
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

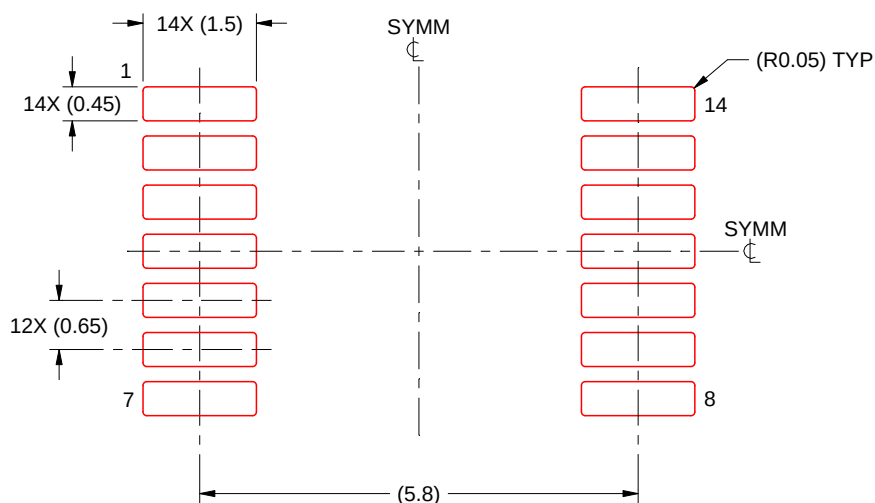
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



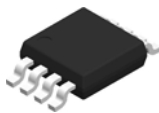
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

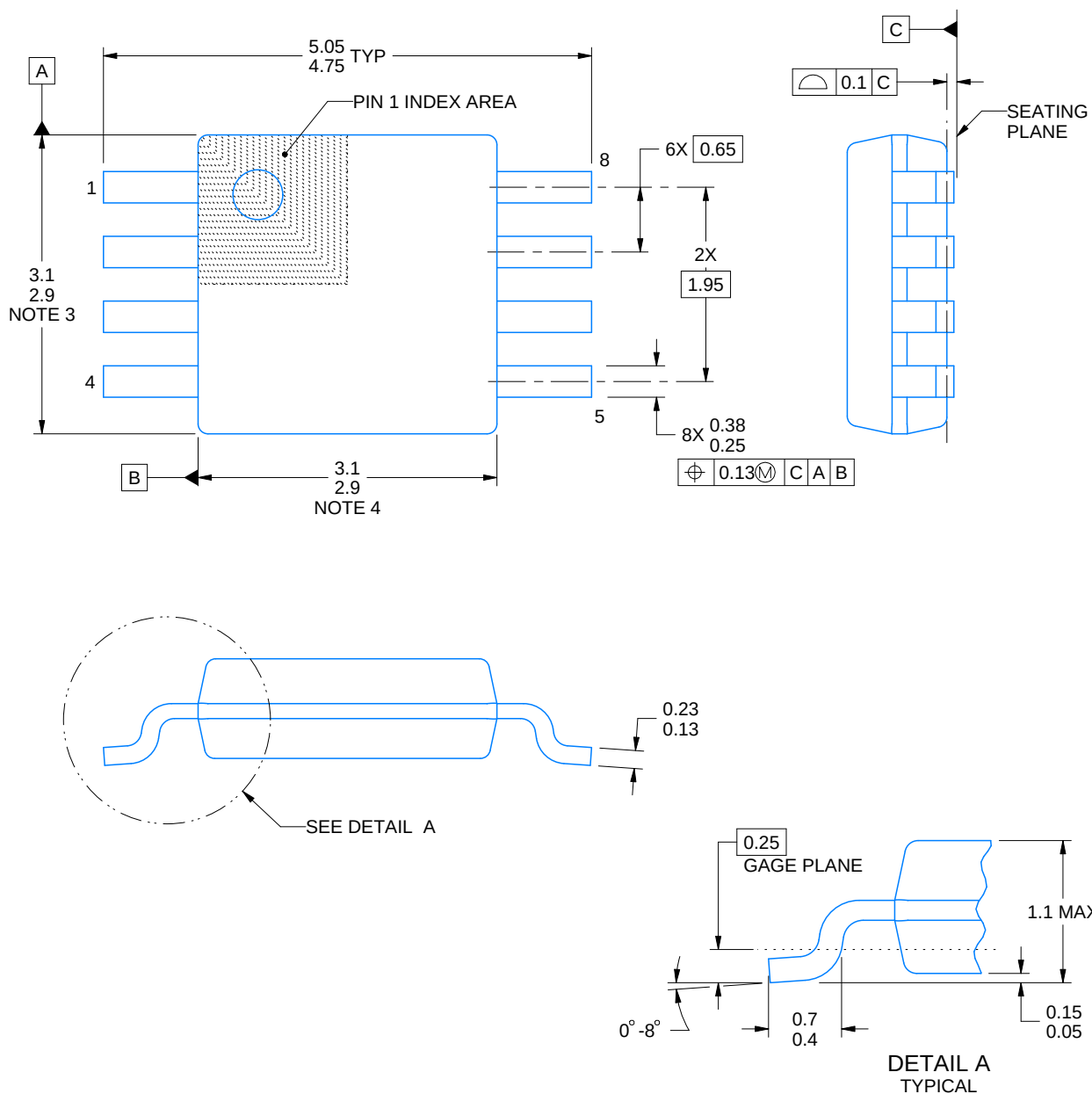
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

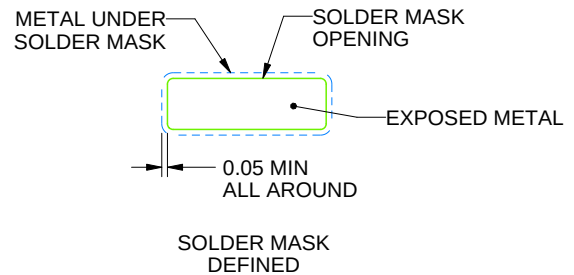
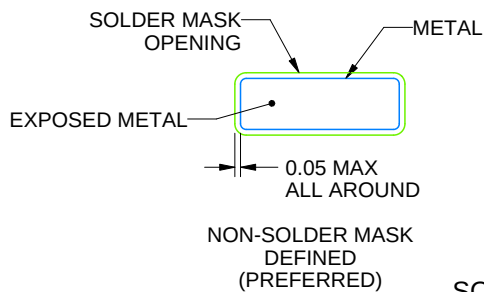
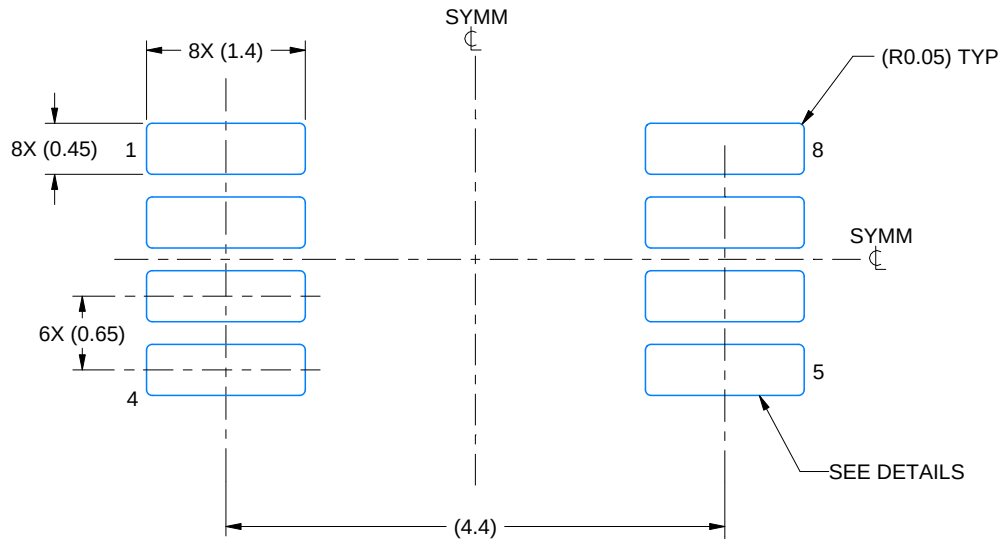
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

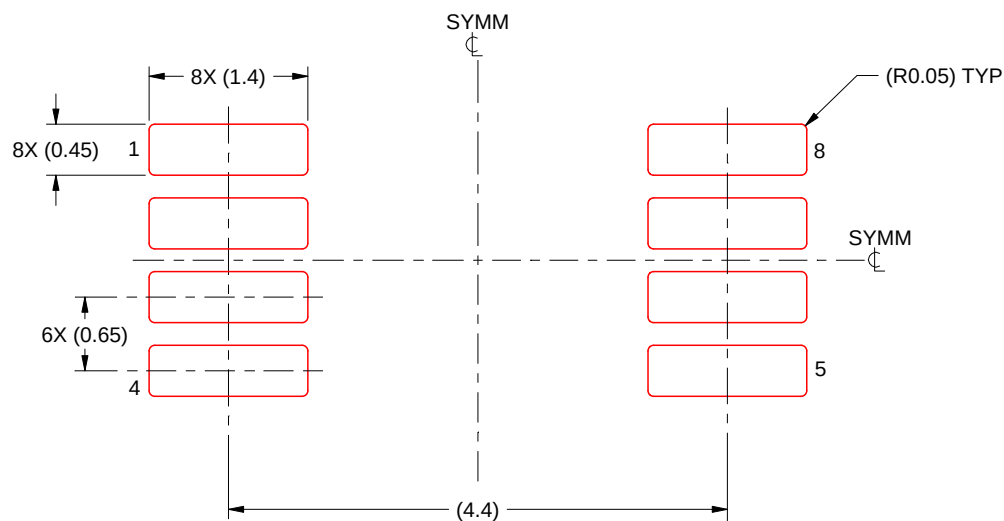
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

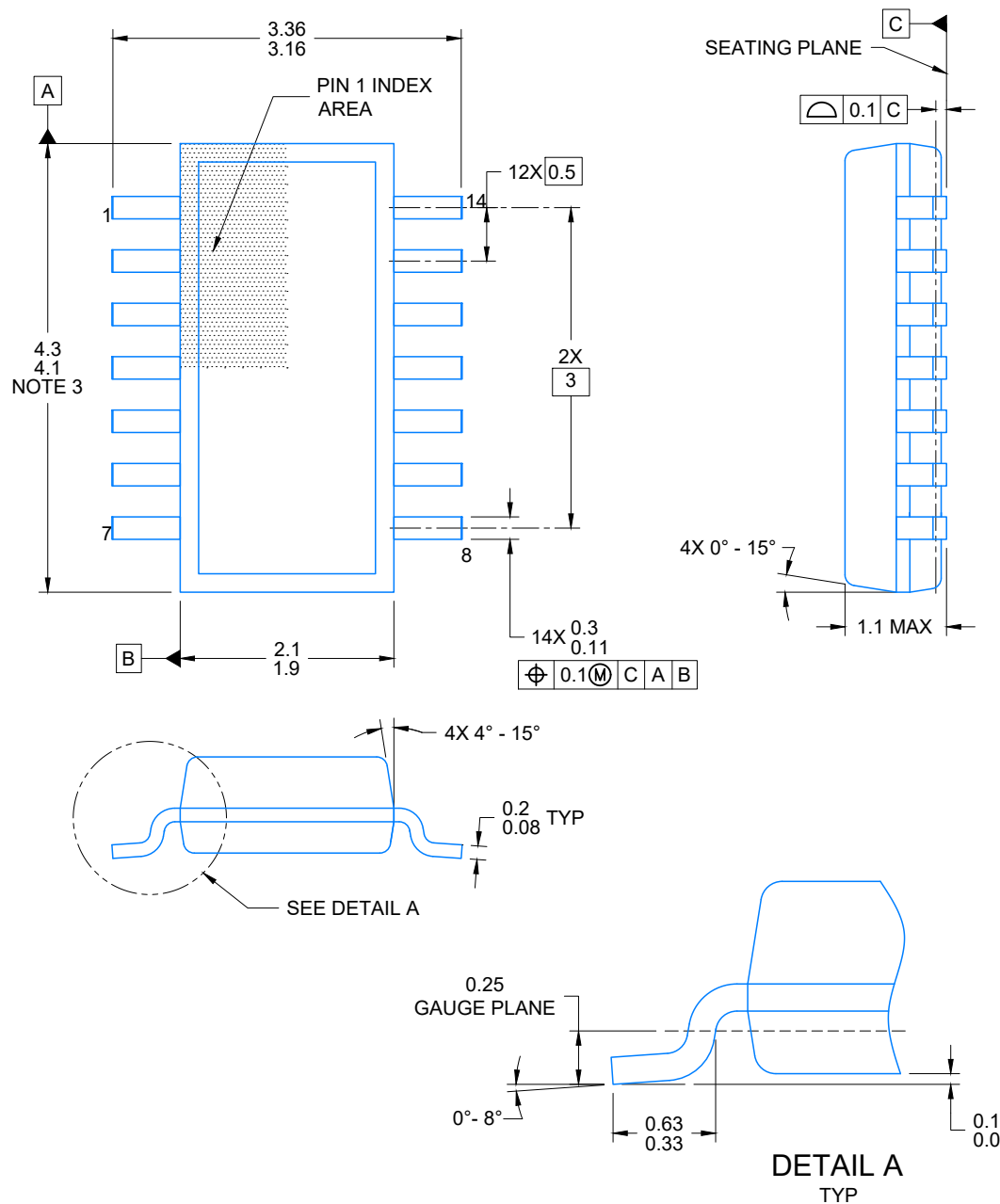


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

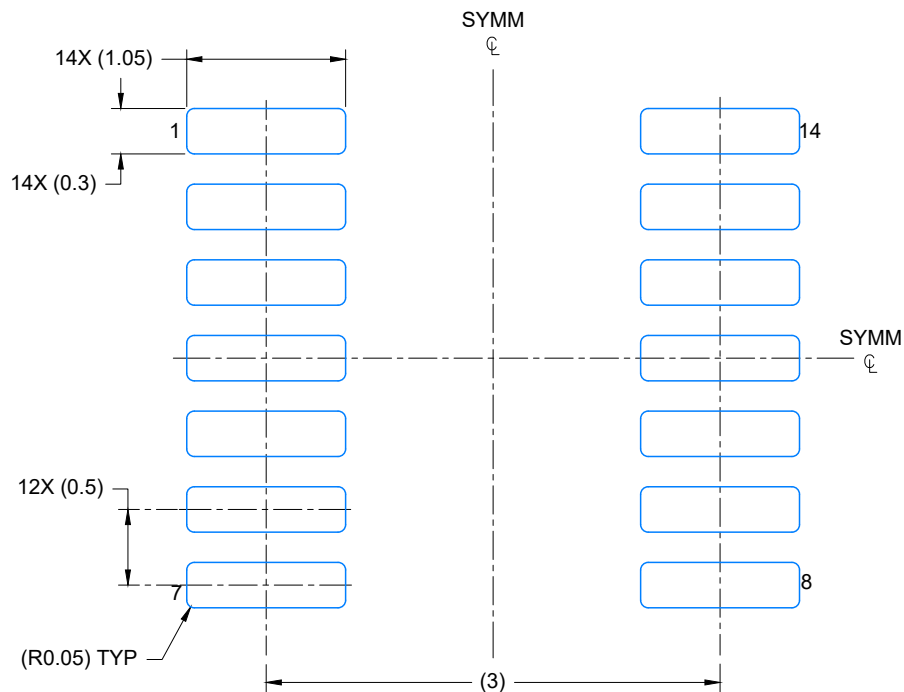
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



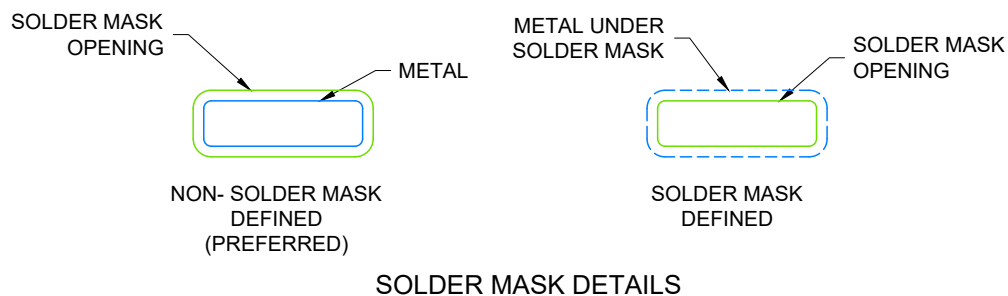
4224643/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



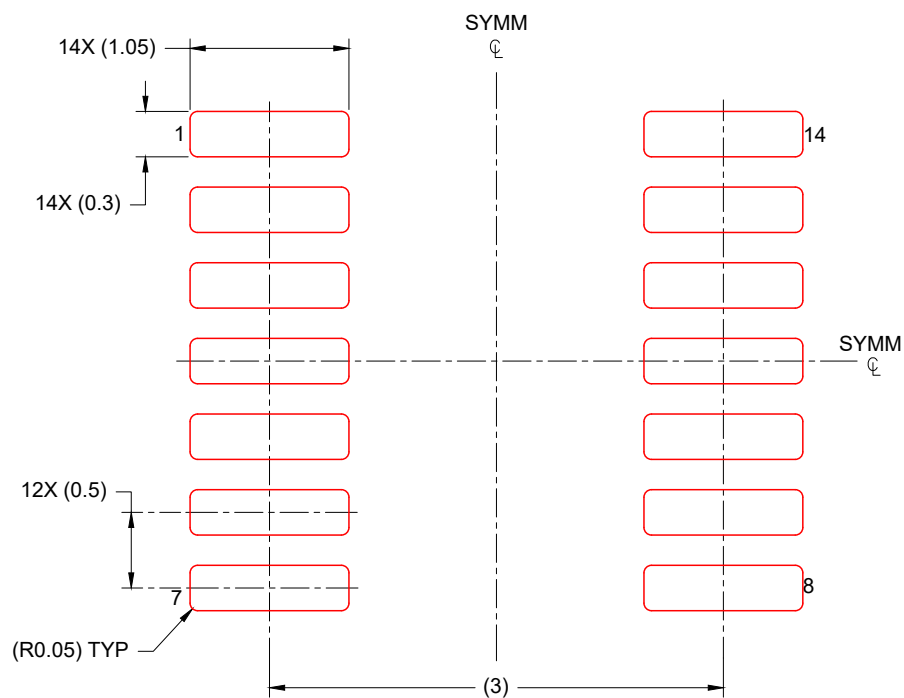
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
版权所有 © 2025，德州仪器 (TI) 公司