

用于并联充电应用的 bq25600C I²C 控制型 3.0A 单节电池 充电器

1 特性

- 在双充电器操作下，并联充电器提供快速充电
- 高效 1.5MHz 同步开关模式降压充电器
 - 在 2A 电流 (5V 输入) 下具有 92% 的充电效率
 - 针对 USB 电压输入 (5V) 进行了优化
 - 用于轻负载运行的低功耗脉冲频率调制 (PFM) 模式
- 单个输入，支持 USB 输入和高压适配器
 - 支持 3.9V 至 13.5V 输入电压范围，绝对最大输入电压额定值为 22V
 - 可编程输入电流限制 (100mA 至 3.2A，分辨率为 100mA)，支持 USB2.0、USB3.0 标准和高压适配器 (IINDPM)
 - 通过高达 5.4V 的输入电压限制 (VINDPM) 进行最大功率跟踪
 - VINDPM 阈值自动跟踪电池电压
- 采用 19.5mΩ 充电电流感应 MOSFET 实现高充电效率
- 窄 VDC (NVDC) 电源路径管理
 - 无需电池或深度放电的电池即可瞬时启动
 - 电池充电模式下的理想二极管运行
- 灵活的自主和 I²C 模式，可实现最优系统性能
- 高集成度，包括所有 MOSFET、电流感应和环路补偿

- 17μA 低电池泄漏电流
- 高精度
 - ±0.5% 充电电压调节
 - ±5% 1.5A 充电电流调节
 - ±6% 1.38A 充电电流调节
 - ±10% 0.9A 输入电流调节
- 用于快速充电的远程电池感应

2 应用

- 智能电话
- 平板电脑

3 说明

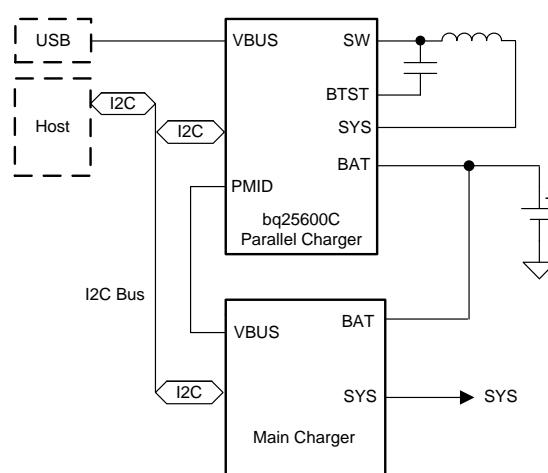
bq25600C 器件是高度集成的 3.0A 开关模式电池充电管理和系统电源路径管理器件，适用于单节锂离子和锂聚合物电池。低阻抗电源路径可优化开关模式运行效率并缩短电池充电时间。具有充电和系统设置的 I²C 串行接口使得此器件成为一个真正的灵活解决方案。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
bq25600C	DSBGA (30)	2.2mm × 2.59mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化电路原理图



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English Data Sheet: SLUSD36

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2017 年 9 月	*	初始发行版。

5 说明 (续)

bq25600C 是高度集成的 3.0A 开关模式电池充电管理和系统电源路径管理器件，适用于单节锂离子和锂聚合物电池。该器件通过高输入电压和高效率实现快速充电，支持用于各种智能手机、平板电脑和便携式设备的并联充电应用。bq25600C 具有与 bq25600 不同的 I²C 地址，因此在选择 bq25600 作为主充电器并选择 bq25600C 作为并联充电器时，仅需要单个 I²C 总线。其低阻抗电源路径可优化开关模式运行效率并缩短电池充电时间。其输入电压和电流调节以及电池远程感应可以为电池提供最大的充电功率。该解决方案在系统和电池之间高度集成输入反向阻断 FET (RBFET, Q1)、高侧开关 FET (HSFET, Q2)、低侧开关 FET (LSFET, Q3) 以及电池 FET (BATFET, Q4)。它还集成了自举二极管以进行高侧栅极驱动，从而简化系统设计。具有充电和系统设置的 I²C 串行接口使得此器件成为一个真正的灵活解决方案。

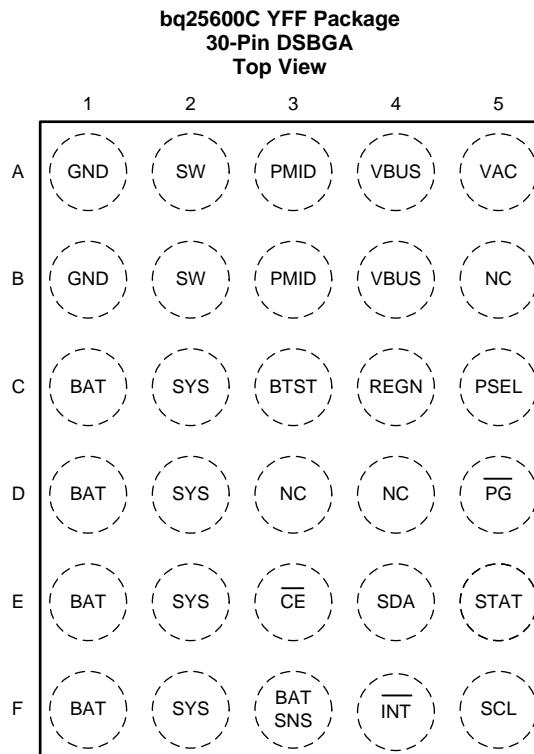
该器件支持多种输入源，包括标准 USB 主机端口、USB 充电端口以及兼容 USB 的高电压适配器。该器件根据内置 USB 接口设置默认输入电流限值。为了设置默认输入电流限值，器件使用内置 USB 接口或者从系统检测电路（如 USB PHY 器件）中获取结果。该器件符合 USB 2.0 和 USB 3.0 电源规范，具有输入电流和电压调节功能。

此器件在无需软件控制情况下启动并完成一个充电周期。它感应电池电压并通过三个阶段为电池充电：预充电、恒定电流和恒定电压。在充电周期的末尾，当充电电流低于预设限值并且电池电压高于再充电阈值时，充电器自动终止。如果已完全充电的电池降至再充电阈值以下，则充电器自动启动另一个充电周期。

此充电器提供针对电池充电和系统运行的多种安全特性，其中包括充电安全计时器以及过压和过流保护。当结温超过 110°C (可编程) 时，热调节会减小充电电流。STAT 输出报告充电状态和任何故障状况。其他安全特性包括热调节和热关断以及输入 UVLO 和过压保护。VBUS_GD 位指示电源是否正常。当发生故障时，INT 输出会立即通知主机。

这些器件采用 30 个焊球、2.0mm × 2.4mm WCSP 封装。

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
NC	B5	AO	No Connect. Must leave this pin floating.
BAT	C1	P	Battery connection point to the positive terminal of the battery pack. The internal current sensing resistor is connected between SYS and BAT. Connect a 10 μ F closely to the BAT pin.
	D1		
	E1		
	F1		
BATSNS	F3	AIO	Battery voltage sensing pin for charge current regulation. in order to minimize the parasitic trace resistance during charging, BATSNS pin is connected to the actual battery pack as close as possible.
BTST	C3	P	PWM high side driver positive supply. internally, the BTST is connected to the cathode of the boost-strap diode. Connect the 0.047- μ F bootstrap capacitor from SW to BTST.
CE	E3	DI	Charge enable pin. When this pin is driven low, battery charging is enabled.
GND	A1	—	
	B1		
INT	F4	DO	Open-drain interrupt Output. Connect the INT to a logic rail through 10-k Ω resistor. The INT pin sends active low, 256- μ s pulse to host to report charger device status and fault.
PG	D5	DO	Open drain active low power good indicator. Connect to the pull up rail through 10 k Ω resistor. LOW indicates a good input source if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and current limit is above 30 mA.
PMID	A3	DO	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Given the total input capacitance, put 1 μ F on VBUS to GND, and the rest capacitance on PMID to GND.
	B3		
PSEL	C5	DI	Power source selection input. High indicates 500 mA input current limit. Low indicates 2.4A input current limit. Once the device gets into host mode, the host can program different input current limit to IINDPM register.
REGN	C4	P	PWM low side driver positive supply output. internally, REGN is connected to the anode of the boost-strap diode. Connect a 4.7- μ F (10-V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC.

(1) AI = Analog input, AO = Analog Output, AIO = Analog input Output, DI = Digital input, DO = Digital Output, DIO = Digital input Output, P = Power

Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
SCL	F5	DI	I ² C interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	E4	DIO	I ² C interface data. Connect SDA to the logic rail through a 10-kΩ resistor.
STAT	E5	DO	Open-drain interrupt output. Connect the STAT pin to a logic rail via 10-kΩ resistor. The STAT pin indicates charger status. Charge in progress: LOW Charge complete or charger in SLEEP mode: HIGH Charge suspend (fault response): Blink at 1Hz
SW	A2 B2	P	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047-μF bootstrap capacitor from SW to BTST.
SYS	C2 D2 E2 F2	P	Converter output connection point. The internal current sensing resistor is connected between SYS and BAT. Connect a 20 μF closely to the SYS pin.
Thermal Pad	—	P	Ground reference for the device that is also the thermal pad used to conduct heat from the device. This connection serves two purposes. The first purpose is to provide an electrical ground connection for the device. The second purpose is to provide a low thermal-impedance path from the device die to the PCB. This pad should be tied externally to a ground plane.
NC	D3, D4	AI	No Connect. Leave this pin floating.
VAC	A5	AI	Input voltage sensing. This pin must be connected to VBUS.
VBUS	A4 B4	P	Charger input voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1-uF ceramic capacitor from VBUS to GND and place it as close as possible to IC.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage Range (with respect to GND)	VAC	-2	22	V
	VBUS (converter not switching) ⁽²⁾	-2	22	V
	BTST, PMID (converter not switching) ⁽²⁾	-0.3	22	V
	SW	-2	16	V
	BTST to SW	-0.3	7	V
	PSEL	-0.3	7	V
	BATSNS (converter not switching)	-0.3	7	V
	REGN, TS, CE, PG, BAT, SYS (converter not switching)	-0.3	7	V
	SDA, SCL, INT, STAT	-0.3	7	V
Output Sink Current	STAT, INT		6	mA
Operating junction temperature, T _J		-40	150	°C
Storage temperature, T _{stg}		-65	150	°C

(1) Stresses beyond those listed under Absolute maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

(2) VBUS is specified up to 22 V for a maximum of one hour at room temperature

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±250

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{BUS}	Input voltage	3.9		13.5 ⁽¹⁾	V
I _{in}	Input current (VBUS)			3.25	A
I _{SWOP}	Output current (SW)			3.25	A
V _{BATOP}	Battery voltage			4.624	V
I _{BATOP}	Fast charging current			3.0	A
I _{BATOP}	Discharging current (continuous)			6	A
T _A	Operating ambient temperature	-40		85	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum voltage rating on either the BTST or SW pins. A tight layout minimizes switching noise.

7.4 Thermal information

THERMAL METRIC		bq25600C	UNIT
		YFF (DSBGA)	
		30 Balls	
R _{θJA}	Junction-to-ambient thermal resistance	58.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	8.3	°C/W

Thermal information (continued)

THERMAL METRIC		bq25600C	UNIT
		YFF (DSBGA)	
		30 Balls	
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

7.5 Electrical Characteristics

$V_{VAC_UVLOZ} < V_{VAC} < V_{VAC_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, $T_J = -40^{\circ}\text{C}$ to 125°C and $T_J = 25^{\circ}\text{C}$ for typical values (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS					
I_{BAT}	$V_{BAT} = 4.5\text{ V}$, $V_{BUS} < V_{AC_UVLOZ}$, leakage between BAT and VBUS, $T_J < 85^{\circ}\text{C}$			5	µA
I_{BAT}	$V_{BAT} = 4.5\text{ V}$, HIZ Mode and OVPFET_DIS = 1 or No VBUS, I2C disabled, BATFET Disabled. $T_J < 85^{\circ}\text{C}$		17	33	µA
I_{BAT}	$V_{BAT} = 4.5\text{ V}$, HIZ Mode and OVPFET_DIS = 1 or No VBUS, I2C Disabled, BATFET Enabled. $T_J < 85^{\circ}\text{C}$		58	85	µA
I_{VAC_HIZ}	$V_{VAC} = 5\text{ V}$, HIZ Mode and OVPFET_DIS = 1, No battery		24	37	µA
I_{VAC_HIZ}	$V_{VAC} = 12\text{ V}$, HIZ Mode and OVPFET_DIS = 1, No battery		41	61	µA
$I_{VACVBUS_HIZ}$	$V_{VAC} = 5\text{ V}$, HIZ Mode and VBUS short) in buck mode		37	50	µA
$I_{VACVBUS_HIZ}$	$V_{VAC} = 12\text{ V}$, HIZ Mode and VBUS short) in buck mode		68	90	µA
I_{VBUS}	$V_{VBUS} = 12\text{ V}$, $V_{VBUS} > V_{VBAT}$, converter not switching		1.5	3	mA
I_{VBUS}	$V_{VBUS} > V_{UVLO}$, $V_{VBUS} > V_{VBAT}$, converter switching, $V_{BAT} = 3.8\text{V}$, $ISYS = 0\text{A}$		3		mA

VBUS, VAC AND BAT PIN POWER-UP

V_{BUS_OP}	VBUS operating range	V_{VBUS} rising	3.9		13.5	V
V_{VAC_UVLOZ}	VAC for active I ² C, no battery Sense VAC pin voltage	V_{VAC} rising		3.3	3.7	V
$V_{VAC_UVLOZ_HYS}$	I ² C active hysteresis	V_{VAC} falling from above V_{VAC_UVLOZ}		300		mV
$V_{VAC_PRESENT}$	VAC to turn on REGN	V_{VAC} rising		3.65	3.9	V
$V_{VAC_PRESENT_HYS}$	VAC to turn on REGN hysteresis	V_{VAC} falling		500		mV
V_{SLEEP}	Sleep mode falling threshold	$(V_{VAC} - V_{VBAT})$, $V_{BUSMIN_FALL} \leq V_{BAT} \leq V_{REG}$, VAC falling	15	60	131	mV
V_{SLEEPZ}	Sleep mode rising threshold	$(V_{VAC} - V_{VBAT})$, $V_{BUSMIN_FALL} \leq V_{BAT} \leq V_{REG}$, VAC rising	115	220	340	mV
$V_{VAC_OV_RISE}$	VAC 6.5-V Overvoltage rising threshold	VAC rising; OVP (REG06[7:6]) = '01'	6.1	6.42	6.75	V
$V_{VAC_OV_RISE}$	VAC 10.5-V Overvoltage rising threshold	VAC rising, OVP (REG06[7:6]) = '10'	10.35	11	11.5	V
$V_{VAC_OV_RISE}$	VAC 14-V Overvoltage rising threshold	VAC rising, OVP (REG06[7:6]) = '11'	13.5	14.2	15	V

Electrical Characteristics (continued)

$V_{VAC_UVLOZ} < V_{VAC} < V_{VAC_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, $T_J = -40^{\circ}\text{C}$ to 125°C and $T_J = 25^{\circ}\text{C}$ for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VAC_OV_HYS}$	VAC 6.5-V Overvoltage hysteresis	VAC falling, OVP (REG06[7:6]) = '01'		130		mV
$V_{VAC_OV_HYS}$	VAC 10.5-V Overvoltage hysteresis	VAC falling, OVP (REG06[7:6]) = '10'		250		mV
$V_{VAC_OV_HYS}$	VAC 14-V Overvoltage hysteresis	VAC falling, OVP (REG06[7:6]) = '11'		300		mV
V_{BAT_UVLOZ}	BAT for active $I^2\text{C}$, no adapter	V_{BAT} rising	2.5			V
$V_{BAT_DPL_FALL}$	Battery Depletion Threshold	V_{BAT} falling	2.18		2.62	V
$V_{BAT_DPL_RISE}$	Battery Depletion Threshold	V_{BAT} rising	2.34		2.86	V
$V_{BAT_DPL_HYST}$	Battery Depletion rising hysteresis	V_{BAT} rising		180		mV
V_{BUSMIN_FALL}	Bad adapter detection falling threshold	V_{BUS} falling	3.68	3.8	3.9	V
V_{BUSMIN_HYST}	Bad adapter detection hysteresis			180		mV
I_{BADSRC}	Bad adapter detection current source	Sink current from V_{BUS} to GND		30		mA
POWER-PATH						
V_{SYS_MIN}	System regulation voltage	$V_{VBAT} < \text{SYS_MIN}[2:0] = 101$, BATFET Disabled (REG07[5] = 1)	3.5	3.68		V
V_{SYS}	System Regulation Voltage	$I_{SYS} = 0 \text{ A}$, $V_{VBAT} > V_{SYSMIN}$, $V_{VBAT} = 4.400 \text{ V}$, BATFET disabled (REG07[5] = 1)		$V_{BAT} + 50 \text{ mV}$		V
V_{SYS_MAX}	Maximum DC system voltage output	$I_{SYS} = 0 \text{ A}$, Q4 off, $V_{VBAT} \leq 4.400 \text{ V}$, $V_{VBAT} > V_{SYSMIN} = 3.5\text{V}$	4.4	4.45	4.48	V
$R_{ON(RBFET)}$	Top reverse blocking MOSFET on-resistance between V_{BUS} and $\text{PMID} - Q1$	$-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$		35		$\text{m}\Omega$
$R_{ON(HSFET)}$	Top switching MOSFET on-resistance between PMID and $\text{SW} - Q2$	$V_{REGN} = 5 \text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$		55		$\text{m}\Omega$
$R_{ON(LSFET)}$	Bottom switching MOSFET on-resistance between SW and $\text{GND} - Q3$	$V_{REGN} = 5 \text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$		60		$\text{m}\Omega$
V_{FWD}	BATFET forward voltage in supplement mode			30		mV
$R_{ON(BAT-SYS)}$	SYS-BAT MOSFET on-resistance	Measured from BAT to SYS, $V_{BAT} = 4.2\text{V}$, $T_J = -40 - 125^{\circ}\text{C}$		19.5		$\text{m}\Omega$
BATTERY CHARGER						
V_{BATREG_RANGE}	Charge voltage program range		3.856		4.624	V
V_{BATREG_STEP}	Charge voltage step			32		mV
V_{BATREG}	Charge voltage setting	$V_{REG} (\text{REG04}[7:3]) = 4.208 \text{ V}$ (01011), V , $-40 \leq T_J \leq 85^{\circ}\text{C}$	4.187	4.208	4.229	V
		$V_{REG} (\text{REG04}[7:3]) = 4.352 \text{ V}$ (01111), V , $-40 \leq T_J \leq 85^{\circ}\text{C}$	4.330	4.352	4.374	V
V_{BATREG_ACC}	Charge voltage setting accuracy	$V_{BAT} = 4.208 \text{ V}$ or $V_{BAT} = 4.352 \text{ V}$, $-40 \leq T_J \leq 85^{\circ}\text{C}$	-0.5%		0.5%	
$I_{CHG_REG_RANGE}$	Charge current regulation range		0		3000	mA
$I_{CHG_REG_STEP}$	Charge current regulation step			60		mA
I_{CHG_REG}	Charge current regulation setting	$I_{CHG} = 240 \text{ mA}$, $V_{VBAT} = 3.1\text{V}$ or $V_{VBAT} = 3.8 \text{ V}$	0.214	0.24	0.26	A
$I_{CHG_REG_ACC}$	Charge current regulation accuracy	$I_{CHG} = 240 \text{ mA}$, $V_{VBAT} = 3.1 \text{ V}$ or $V_{VBAT} = 3.8 \text{ V}$	-11%		9%	

Electrical Characteristics (continued)

$V_{VAC_UVLOZ} < V_{VAC} < V_{VAC_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, $T_J = -40^\circ\text{C}$ to 125°C and $T_J = 25^\circ\text{C}$ for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CHG_REG}	Charge current regulation setting	$I_{CHG} = 720 \text{ mA}$, $V_{VBAT} = 3.1 \text{ V}$ or $V_{VBAT} = 3.8 \text{ V}$	0.68	0.720	0.76	A
I_{CHG_REG}	Charge current regulation accuracy	$I_{CHG_REG} = 720 \text{ mA}$, $V_{BAT} = 3.1 \text{ V}$ or $V_{BAT} = 3.8 \text{ V}$	-6%		6%	
I_{CHG_REG}	Charge current regulation setting	$I_{CHG} = 1.38 \text{ A}$, $V_{VBAT} = 3.1 \text{ V}$ or $V_{VBAT} = 3.8 \text{ V}$	1.30	1.380	1.45	A
$I_{CHG_REG_ACC}$	Charge current regulation accuracy	$I_{CHG} = 720 \text{ mA}$ or $I_{CHG} = 1.38 \text{ A}$, $V_{VBAT} = 3.1 \text{ V}$ or $V_{VBAT} = 3.8 \text{ V}$	-6%		6%	
$V_{BATLOWV_FALL}$	Battery LOWV falling threshold	$I_{CHG} = 240 \text{ mA}$	2.7	2.8	2.9	V
$V_{BATLOWV_RISE}$	Battery LOWV rising threshold	Pre-charge to fast charge	3	3.12	3.24	V
I_{PRECHG}	Precharge current regulation	$IPRECHG[3:0] = '0010' = 180 \text{ mA}$	150	170	190	mA
I_{PRECHG_ACC}	Precharge current regulation accuracy	$IPRECHG[3:0] = '0010' = 180 \text{ mA}$	-15		5	%
I_{TERM}	Termination current regulation	$I_{CHG} > 780 \text{ mA}$, $ITERM[3:0] = '0010'$ $= 180 \text{ mA}$, $V_{VBAT} = 4.208 \text{ V}$	145	180	215	mA
I_{TERM_ACC}	Termination current regulation accuracy	$I_{CHG} > 780 \text{ mA}$, $ITERM[3:0] = '0010'$ $= 180 \text{ mA}$, $V_{VBAT} = 4.208 \text{ V}$	-20%		20%	
I_{TERM}	Termination current regulation	$I_{CHG} \leq 780 \text{ mA}$, $ITERM[3:0] = '0000'$ $= 60 \text{ mA}$, $V_{VBAT} = 4.208 \text{ V}$	44	60	75	mA
I_{TERM_ACC}	Termination current regulation accuracy	$I_{CHG} \leq 780 \text{ mA}$, $ITERM[3:0] = '0000'$ $= 60 \text{ mA}$, $V_{VBAT} = 4.208 \text{ V}$	-27%		25%	
V_{SHORT}	Battery short voltage	V_{VBAT} falling	1.85	2	2.15	V
V_{SHORTZ}	Battery short voltage	V_{VBAT} rising	2.15	2.25	2.35	V
I_{SHORT}	Battery short current	$V_{VBAT} < V_{SHORTZ}$	50	90	117	mA
V_{RECHG}	Recharge Threshold below V_{BAT_REG}	V_{BAT} falling, $REG04[0] = 0$	90	120	150	mV
V_{RECHG}	Recharge Threshold below V_{BAT_REG}	V_{BAT} falling, $REG04[0] = 1$	200	230	265	mV
$I_{SYSLOAD}$	System discharge load current	$V_{SYS} = 4.2 \text{ V}$		30		mA
INPUT VOLTAGE AND CURRENT REGULATION						
V_{INDPM}	Input voltage regulation limit	V_{INDPM} ($REG06[3:0] = 0000$) = 3.9 V	3.78	3.95	4.1	V
V_{INDPM_ACC}	Input voltage regulation accuracy	V_{INDPM} ($REG06[3:0] = 0000$) = 3.9 V	-4.5%		4%	
V_{INDPM}	Input voltage regulation limit	V_{INDPM} ($REG06[3:0] = 0110$) = 4.4 V	4.268	4.4	4.532	V
V_{INDPM_ACC}	Input voltage regulation accuracy	V_{INDPM} ($REG06[3:0] = 0110$) = 4.4 V	-3%		3%	
V_{DPM_VBAT}	Input voltage regulation limit tracking V_{BAT}	$V_{INDPM} = 3.9 \text{ V}$, $V_{DPM_VBAT_TRACK} = 300 \text{ mV}$, $V_{BAT} = 4.0 \text{ V}$	4.17	4.3	4.46	V
$V_{DPM_VBAT_ACC}$	Input voltage regulation accuracy tracking V_{BAT}	$V_{INDPM} = 3.9 \text{ V}$, $V_{DPM_VBAT_TRACK} = 300 \text{ mV}$, $V_{BAT} = 4.0 \text{ V}$	-3%		4%	
I_{INDPM}	USB input current regulation limit	$V_{VBUS} = 5 \text{ V}$, current pulled from SW, I_{INDPM} ($REG[4:0] = 00100$) = 500 mA, $-40 \leq T_J \leq 85^\circ\text{C}$	450		500	mA
		$V_{VBUS} = 5 \text{ V}$, current pulled from SW, I_{INDPM} ($REG[4:0] = 01000$) = 900 mA, $-40 \leq T_J \leq 85^\circ\text{C}$	750		900	mA
		$V_{VBUS} = 5 \text{ V}$, current pulled from SW, I_{INDPM} ($REG[4:0] = 01110$) = 1.5 A, $-40 \leq T_J \leq 85^\circ\text{C}$	1.28		1.5	A
I_{IN_START}	Input current limit during system start-up sequence			200		mA
BAT PIN OVERVOLTAGE PROTECTION						

Electrical Characteristics (continued)

$V_{VAC_UVLOZ} < V_{VAC} < V_{VAC_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, $T_J = -40^{\circ}\text{C}$ to 125°C and $T_J = 25^{\circ}\text{C}$ for typical values (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BATOVP_RISE}	V_{BAT} rising, as percentage of V_{BAT_REG}	103	104	105	%
$V_{BATOVP_Fall_HYS}$	V_{BAT} falling, as percentage of V_{BAT_REG}		2		%

Electrical Characteristics (continued)

$V_{VAC_UVLOZ} < V_{VAC} < V_{VAC_OV}$ and $V_{VAC} > V_{BAT} + V_{SLEEP}$, $T_J = -40^\circ\text{C}$ to 125°C and $T_J = 25^\circ\text{C}$ for typical values (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
THERMAL REGULATION AND THERMAL SHUTDOWN						
$T_{JUNCTION_REG}$	Junction Temperature Regulation Threshold	Temperature Increasing, TREG (REG05[1] = 1) = 110°C		110	$^\circ\text{C}$	
$T_{JUNCTION_REG}$	Junction Temperature Regulation Threshold	Temperature Increasing, TREG (REG05[1] = 0) = 90°C		90	$^\circ\text{C}$	
T_{SHUT}	Thermal Shutdown Rising Temperature	Temperature Increasing		160	$^\circ\text{C}$	
T_{SHUT_HYST}	Thermal Shutdown Hysteresis			30	$^\circ\text{C}$	
CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
I_{BATFET_OCP}	System over load threshold		6.0		A	
PWM						
f_{SW}	PWM switching frequency	Oscillator frequency, buck mode	1320	1500	1680	kHz
D_{MAX}	Maximum PWM duty cycle ⁽¹⁾			97%		
REGN LDO						
V_{REGN}	REGN LDO output voltage	$V_{VBUS} = 9\text{V}$, $I_{REGN} = 40\text{mA}$	5.6	6	6.65	V
V_{REGN}	REGN LDO output voltage	$V_{VBUS} = 5\text{V}$, $I_{REGN} = 20\text{mA}$	4.58	4.7	4.8	V
LOGIC I/O PIN CHARACTERISTICS (\overline{CE}, $PSEL$, SCL, SDA, \overline{INT})						
V_{ILO}	Input low threshold \overline{CE}				0.4	V
V_{IH}	Input high threshold \overline{CE}		1.3			V
I_{BIAS}	High-level leakage current \overline{CE}	Pull up rail 1.8 V			1	μA
V_{ILO}	Input low threshold PSEL				0.4	V
V_{IH}	Input high threshold PSEL		1.3			V
I_{BIAS}	High-level leakage current PSEL	Pull up rail 1.8V			1	μA
LOGIC I/O PIN CHARACTERISTICS (\overline{PG}, $STAT$)						
V_{OL}	Low-level output voltage				0.4	V

(1) Specified by design. Not production tested.

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
VBUS/BAT POWER UP						
t_{ACOV}	VAC OVP reaction time	VAC rising above ACOV threshold to turn off Q2		200		ns
t_{BADSRC}	Bad adapter detection duration			30		ms
BATTERY CHARGER						
t_{TERM_DGL}	Deglitch time for charge termination			250		ms
t_{RECHG_DGL}	Deglitch time for recharge			250		ms
$t_{SYSOVLD_DGL}$	System over-current deglitch time to turn off Q4			100		μs
t_{BATOVP}	Battery over-voltage deglitch time to disable charge			1		μs
t_{SAFETY}	Typical Charge Safety Timer Range		8	10	12	hr
t_{TOP_OFF}	Typical Top-Off Timer Range	TOP_OFF_TIMER[1:0] = 10 (30 min)	24	30	36	min
DIGITAL CLOCK AND WATCHDOG TIMER						
t_{WDT}	REG05[4]=1	REGN LDO disabled		40		s
f_{LPDIG}	Digital Low Power Clock	REGN LDO disabled		30		kHz
f_{DIG}	Digital Clock	REGN LDO enabled		500		kHz
f_{SCL}	SCL clock frequency				400	kHz

7.7 Typical Characteristics

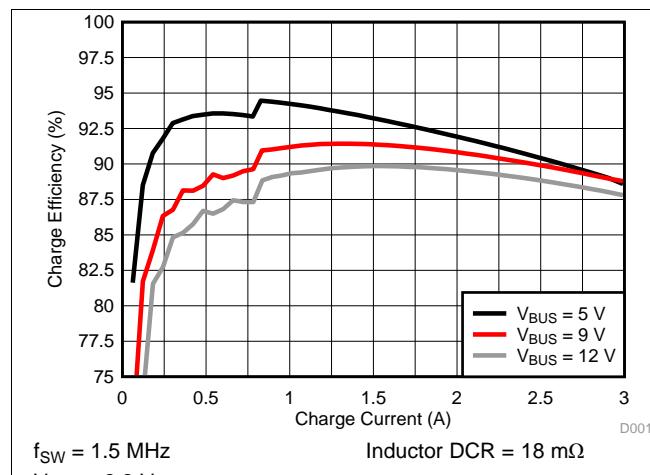


图 1. Charge Efficiency vs. Charge Current

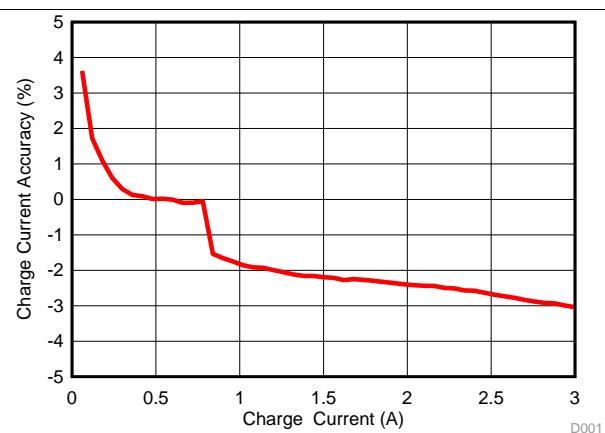


图 2. Charge Current Accuracy

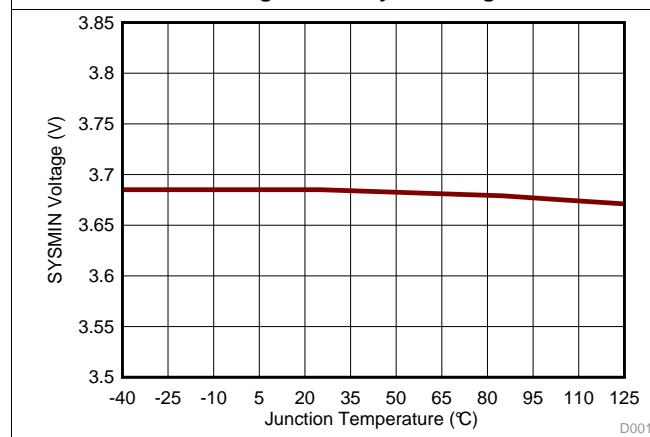


图 3. SYSMIN Voltage vs. Junction Temperature

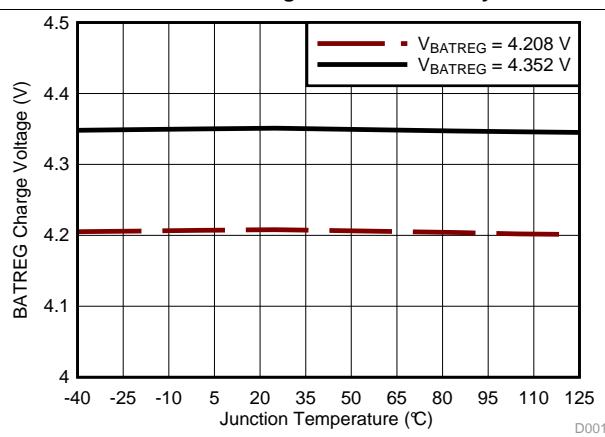


图 4. BATREG Charge Voltage vs. Junction Temperature

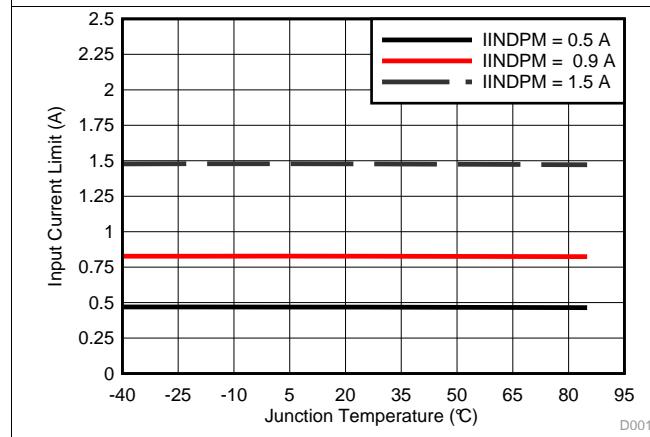


图 5. Input Current Limit vs. Junction Temperature

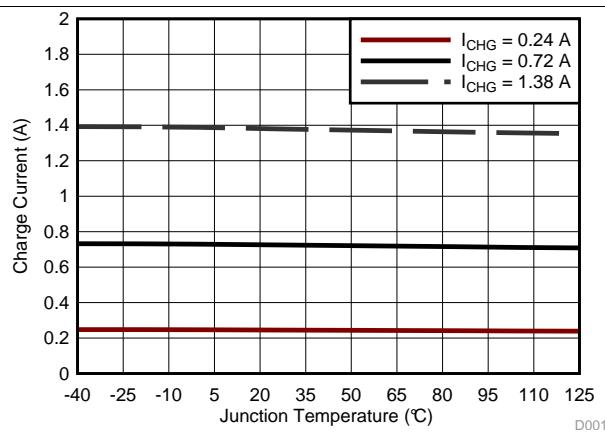


图 6. Charge Current vs. Junction Temperature

Typical Characteristics (接下页)

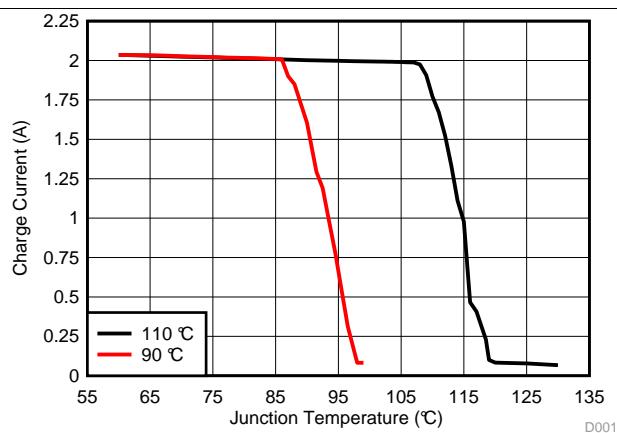


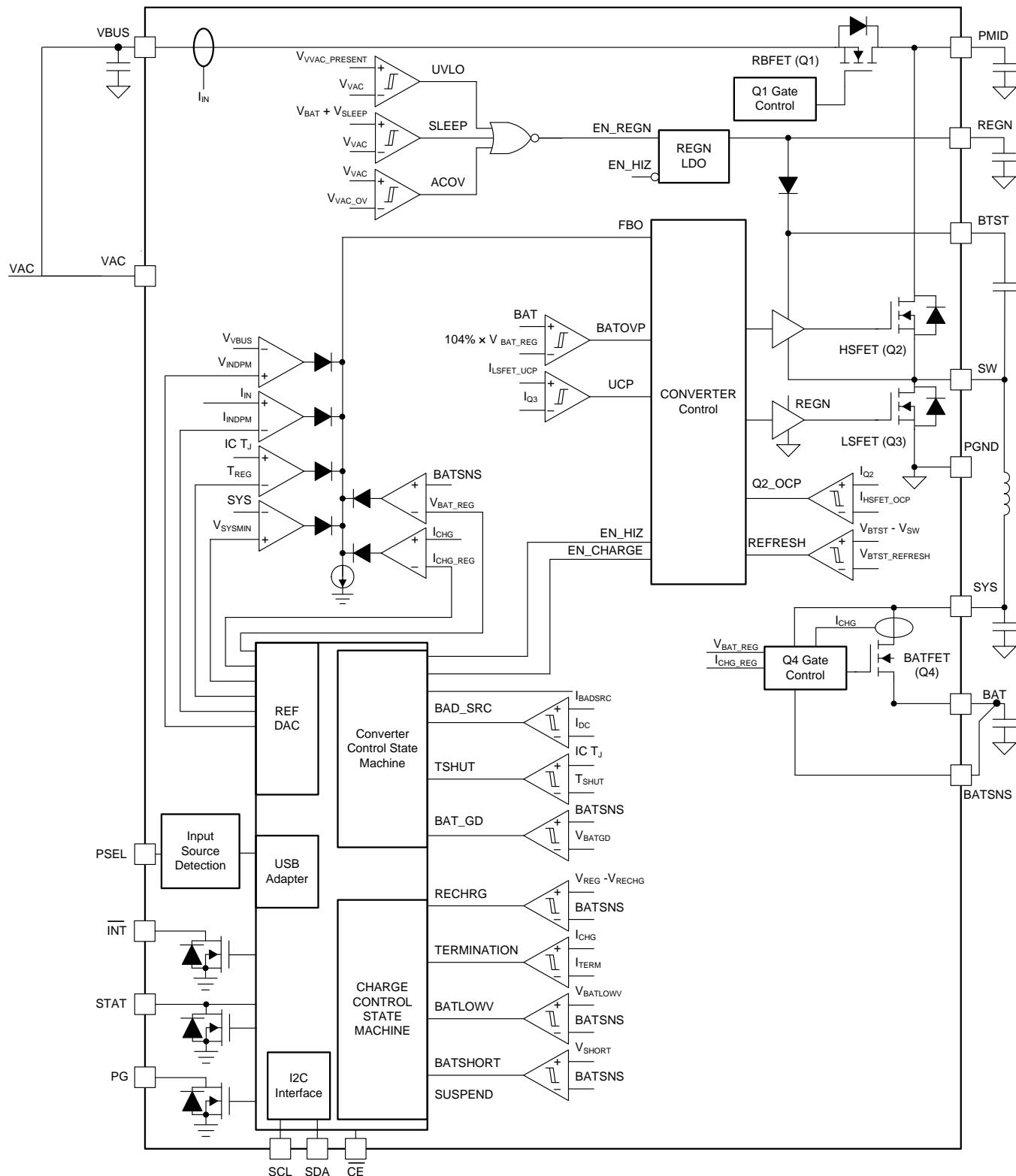
图 7. Charge Current vs. Junction Temperature Under Thermal Regulation

8 Detailed Description

8.1 Overview

The bq25600C device is a highly integrated 3.0-A switch-mode battery charger for single cell Li-Ion and Li-polymer battery. It includes the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4), and bootstrap diode for the high-side gate drive.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Power-On-Reset (POR)

The device powers internal bias circuits from the higher voltage of VBUS and BAT. When VBUS rises above V_{VBUS_UVLOZ} or BAT rises above V_{BAT_UVLOZ} , the sleep comparator, battery depletion comparator and BATFET driver are active. I²C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

8.3.2 Device Power Up from Battery without Input Source

If only battery is present and the voltage is above depletion threshold ($V_{BAT_DPL_RISE}$), the BATFET turns on and connects battery to system. The REGN stays off to minimize the quiescent current. The low RDSON of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

8.3.3 Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. Power Up REGN LDO
2. Poor Source Qualification
3. *Input Source Type Detection* is based on PSEL to set default input current limit (IINDPM) register or input source type.
4. Input Voltage Limit Threshold Setting (VINDPM threshold)
5. Converter Power-up

8.3.3.1 Power Up REGN Regulation

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid:

- above $V_{VAC_PRESENT}$
- V_{VAC} above $V_{BAT} + V_{SLEEPZ}$ in buck mode
- After 220-ms delay is completed

If any one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than IVBUS_HIZ from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

8.3.3.2 Poor Source Qualification

After REGN LDO powers up, the device confirms the current capability of the input source. The input source must meet both of the following requirements in order to start the buck converter.

- voltage below V_{VAC_OV}
- VBUS voltage above $V_{VBUSMIN}$ when pulling I_{BADSRC} (typical 30 mA)

Once the input source passes all the conditions above, the status register bit VBUS_GD is set high and the INT pin is pulsed to signal to the host. If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

8.3.3.3 Input Source Type Detection

After the VBUS_GD bit is set and REGN LDO is powered, the device runs input source detection through PSEL pin. The bq25600C sets input current limit through PSEL pins.

After input source type detection is completed, an INT pulse is asserted to the host. in addition, the following registers and pin are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit
2. PG_STAT bit is set
3. VBUS_STAT bit is updated to indicate USB or other input source

Feature Description (接下页)

The host can over-write IINDPM register to change the input current limit if needed. The charger input current is always limited by the IINDPM register.

8.3.3.3.1 PSEL Pins Sets Input Current Limit in bq25600C

The bq25600C has PSEL pin for input current limit setting to interface with USB PHY. It directly takes the USB PHY device output to decide whether the input is USB host or charging port. When the device operates in host-control mode, the host needs to IINDET_EN bit to read the PSEL value and update the IINDPM register. When the device is in default mode, PSEL value updates IINDPM in real time.

表 1. Input Current Limit Setting from PSEL

Input Detection	PSEL Pin	INPUT CURRENT LIMIT (ILIM)	VBUS_STAT
USB SDP	High	500 mA	001
Adapter	Low	2.4 A	011

8.3.3.4 Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device supports wide range of input voltage limit (3.9 V – 5.4 V) for USB. The device's VINDPM is set at 4.5 V. The device supports dynamic VINDPM tracking settings which tracks the battery voltage. This function can be enabled via the VDPM_BAT_TRACK[1:0] register bits. When enabled, the actual input voltage limit will be the higher of the VINDPM register and VBAT + VDPM_BAT_TRACK offset.

8.3.3.5 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when system rail is ramped up. When the system rail is below 2.2 V, the input current is limited to is to the lower of 200 mA or IINDPM register setting. After the system rises above 2.2 V, the device limits input current to the value set by IINDPM register.

As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

The device switches to PFM control at light load or when battery is below minimum system voltage setting or charging is disabled. The PFM_DIS bit can be used to prevent PFM operation in either buck configuration.

8.3.4 Host Mode and Standalone Power Management

8.3.4.1 Host Mode and Default Mode in bq25600C

The bq25600C is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WATCHDOG_FAULT bit is HIGH. When the charger is in host mode, WATCHDOG_FAULT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings. During default mode, any change on PSEL pin will make real time IINDPM register changes.

In default mode, the device keeps charging the battery with default 10-hour fast charging safety timer. At the end of the 10-hour, the charging is stopped and the buck converter continues to operate to supply system load.

Writing a 1 to the WD_RST bit transitions the charger from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WATCHDOG_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer expires (WATCHDOG_FAULT bit = 1), the device returns to default mode and all registers are reset to default values except IINDPM, VINDPM, BATFET_RST_EN, BATFET_DLY, and BATFET_DIS bits.

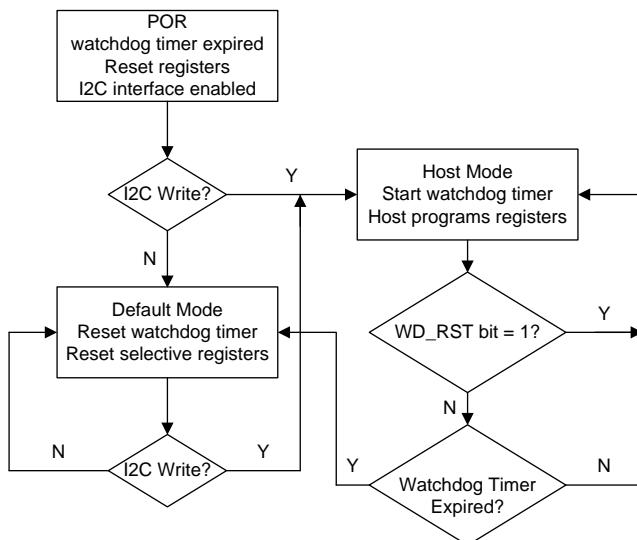


图 8. Watchdog Timer Flow Chart

8.3.5 Power Path Management

The device accommodates a wide range of input sources from USB, wall adapter, to car charger. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

8.3.6 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 3.0-A charge current for high capacity tablet battery. The 19.5-mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

8.3.6.1 Autonomous Charging Cycle

With battery charging is enabled (CHG_CONFIG bit = 1 and \overline{CE} pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in 表 2. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I²C.

表 2. Charging Parameter Default Setting

PARAMETER	SETTING
Charging voltage	4.208 V
Charging current	2.048 A
Pre-charge current	180 mA
Termination current	180 mA
Safety timer	10 hours

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled (CHG_CONFIG bit = 1 and I_{CHG} register is not 0 mA and \overline{CE} is low)
- No safety timer fault
- BATFET is not forced to turn off (BATFET_DIS bit = 0)

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM mode or thermal regulation. When a fully charged battery is discharged below recharge threshold (selectable through VRECHG bit), the device automatically starts a new charging cycle. After the charge is done, toggle \overline{CE} pin or CHG_CONFIG bit can initiate a new charging cycle.

The STAT output indicates the charging status: charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting EN_ICHG_MON bits = 11. in addition, the status register (CHRG_STAT) indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is completed, an INT is asserted to notify the host.

8.3.6.2 Battery Charging Profile

The device charges the battery in five phases: battery short, preconditioning, constant current, constant voltage and top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

表 3. Charging Current Setting

V_{BAT}	CHARGING CURRENT	REGISTER DEFAULT SETTING	CHRG_STAT
< 2.2 V	I_{SHORT}	100 mA	01
2.2 V to 3 V	I_{PRECHG}	180 mA	01
> 3 V	I_{CHG}	2.048 A	10

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. in this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

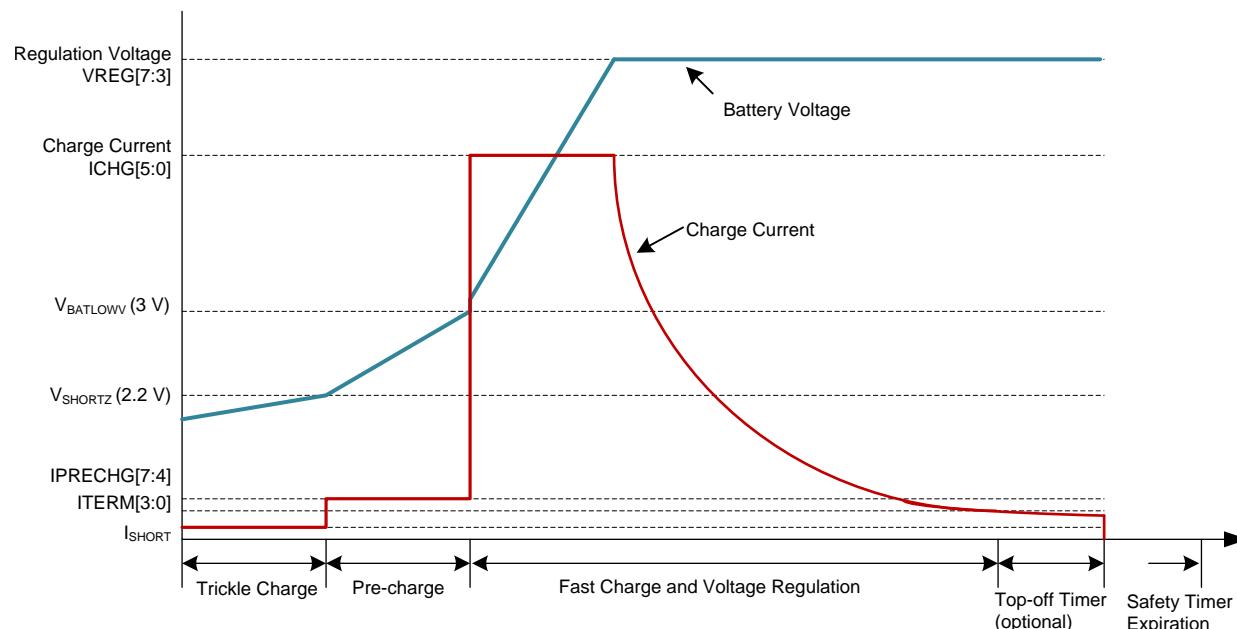


图 9. Battery Charging Profile

8.3.6.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage Supplement Mode.

When termination occurs, the status register CHRG_STAT is set to 11, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be disabled by writing 0 to EN_TERM bit prior to charge termination.

At low termination currents (25 mA-50 mA), due to the comparator offset, the actual termination current may be 10 mA-20 mA higher than the termination target. in order to compensate for comparator offset, a programmable top-off timer can be applied after termination is detected. The termination timer will follow safety timer constraints, such that if safety timer is suspended, so will the termination timer. Similarly, if safety timer is doubled, so will the termination timer. TOPOFF_ACTIVE bit reports whether the top off timer is active or not. The host can read CHRG_STAT and TOPOFF_ACTIVE to find out the termination status.

Top off timer gets reset at one of the following conditions:

1. Charge disable to enable
2. Termination status low to high
3. REG_RST register bit is set

The top-off timer settings are read in once termination is detected by the charger. Programming a top-off timer value after termination will have no effect unless a recharge cycle is initiated. An INT is asserted to the host when entering top-off timer segment as well as when top-off timer expires.

8.3.6.4 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 2 hours when the battery is below $V_{BATLOWV}$ threshold and 10 hours when the battery is higher than $V_{BATLOWV}$ threshold.

The user can program fast charge safety timer through I²C (CHG_TIMER bits). When safety timer expires, the fault register CHRG_FAULT bits are set to 11 and an INT is asserted to the host. The safety timer feature can be disabled through I²C by setting EN_TIMER bit

During input voltage, current, or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IDPM_STAT = 1) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This half clock rate feature can be disabled by writing 0 to TMR2X_EN bit.

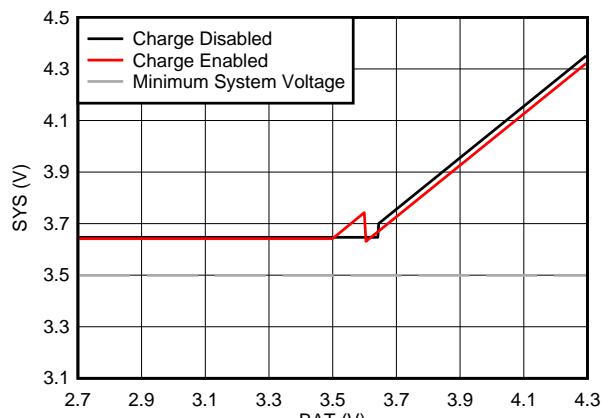
During the fault, timer is suspended. Once the fault goes away, fault resumes. If user stops the current charging cycle, and start again, timer gets reset (toggle CE pin or CHRG_CONFIG bit).

8.3.6.5 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by SYS_Min bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage.

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 180 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the VDS of BATFET.

When the battery charging is disabled and above minimum system voltage setting or charging is terminated, the system is always regulated at typically 50mV above battery voltage. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.



Plot1

图 10. System Voltage vs Battery Voltage

8.3.7 Shipping Mode

8.3.7.1 BATFET Disable Mode (Shipping Mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current. When the host set BATFET_DIS bit, the charger can turn off BATFET immediately or delay by t_{SM_DLY} as configured by BATFET_DLY bit.

8.3.7.2 BATFET Enable (Exit Shipping Mode)

When the BATFET is disabled (in shipping mode) and indicated by setting BATFET_DIS, one of the following events can enable BATFET to restore system power:

1. Plug in adapter
2. Clear BATFET_DIS bit
3. Set REG_RST bit to reset all registers including BATFET_DIS bit to default (0)

8.3.8 Status Outputs (\overline{PG} , STAT)

8.3.8.1 Power Good indicator (\overline{PG} Pin and PG_STAT Bit)

The PG_STAT bit goes HIGH and \overline{PG} pin goes LOW to indicate a good input source when:

- V_{BUS} above V_{VBUS_UVLO}
- V_{BUS} above battery (not in sleep)
- V_{BUS} below V_{VAC_OV} threshold
- V_{BUS} above V_{VBUSMin} (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- Completed *input Source Type Detection*

8.3.8.2 Charging Status indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED. The STAT pin function can be disabled by setting the EN_ICHG_MON bits = 11.

表 4. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH

表 4. STAT Pin State (接下页)

CHARGING STATE	STAT INDICATOR
Charge suspend (input overvoltage, TS fault, timer fault or system overvoltage)	Blinking at 1 Hz

8.3.8.3 Interrupt to Host (\overline{INT})

In some applications, the host does not always monitor the charger operation. The INT pulse notifies the system on the device operation. The following events will generate 256- μ s INT pulse.

- USB/adapter source identified (through PSEL or DPDM detection)
- Good input source detected
 - VBUS above battery (not in sleep)
 - VBUS below V_{VAC_OV} threshold
 - VBUS above $V_{VBUSMin}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- input removed
- Charge Complete
- Any FAULT event in REG09
- VINDPM / IINDPM event detected (maskable)

When a fault occurs, the charger device sends out INT and keeps the fault state in REG09 until the host reads the fault register. Before the host reads REG09 and all the faults are cleared, the charger device would not send any INT upon new faults. To read the current fault status, the host has to read REG09 two times consecutively. The first read reports the pre-existing fault register status and the second read reports the current fault register status.

8.3.9 Protections

8.3.9.1 Voltage and Current Monitoring in Converter Operation

The device closely monitors the input and system voltage, as well as internal FET currents for safe buck mode operation.

8.3.9.1.1 Voltage and Current Monitoring in Buck Mode

8.3.9.1.1.1 Input Overvoltage (ACOV)

This device integrates the functionality of an overvoltage protector. The input voltage is sensed via the VAC pin. The OVP threshold defaults to 6.2V, but can be programmed at 5.5V, 6.2V, 10.5V, or 14.3V via OVP register bits. The ACOV circuit has a reaction time of $t_{AC_OV_FLT}$.

During input overvoltage event (ACOV), the fault register CHRG_FAULT bits are set to 01. An INT pulse is asserted to the host. The device will automatically resume normal operation once the input voltage drops back below the OVP threshold.

8.3.9.2 Thermal Regulation and Thermal Shutdown

8.3.9.2.1 Thermal Protection in Buck Mode

The bq25600C device monitors the internal junction temperature T_J to avoid overheat the chip and limits the device surface temperature in buck mode. When the internal junction temperature exceeds thermal regulation limit (110°C), the device lowers down the charge current. During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when device surface temperature exceeds T_{SHUT} (160°C). The fault register CHRG_FAULT is set to 1 and an INT is asserted to the host. The BATFET and converter is enabled to recover when IC temperature is T_{SHUT_HYS} (30°C) below T_{SHUT} (160°C).

8.3.9.3 Battery Protection

8.3.9.3.1 Battery overvoltage Protection (BATOVP)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charging. The fault register BAT_FAULT bit goes high and an INT is asserted to the host.

8.3.10 Serial interface

The device uses I²C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I²CTM is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6AH, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG0B. Register read beyond REG0B (0x0B) returns 0xFF. The I²C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

8.3.10.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

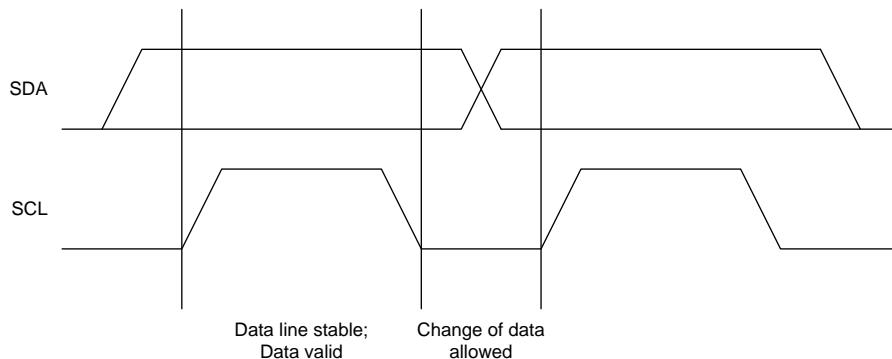


Figure 11. Bit Transfer on the I²C Bus

8.3.10.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the mAstEr. The bus is considered busy after the START condition, and free after the STOP condition.

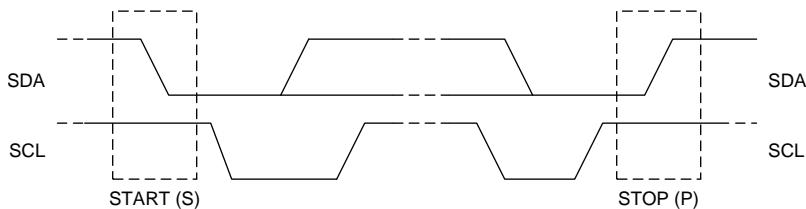


Figure 12. TS START and STOP conditions

8.3.10.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the mAster into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

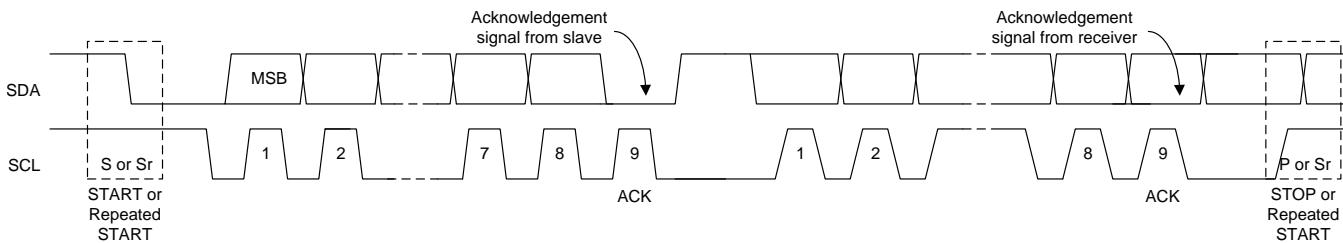


Figure 13. Data Transfer on the I²C Bus

8.3.10.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge ninth clock pulse, are generated by the mAster. The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the ninth clock pulse, this is the Not Acknowledge signal. The mAster can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

8.3.10.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

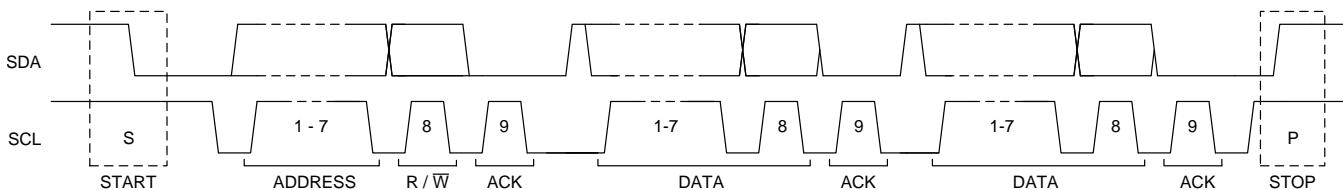


Figure 14. Complete Data Transfer

8.3.10.6 Single Read and Write

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

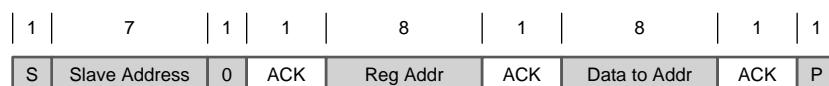


Figure 15. Single Write

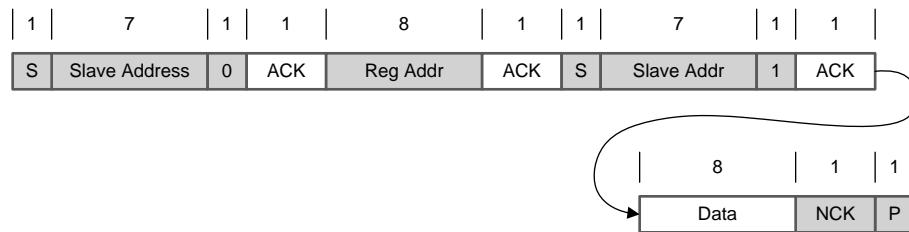


Figure 16. Single Read

8.3.10.7 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG0B.

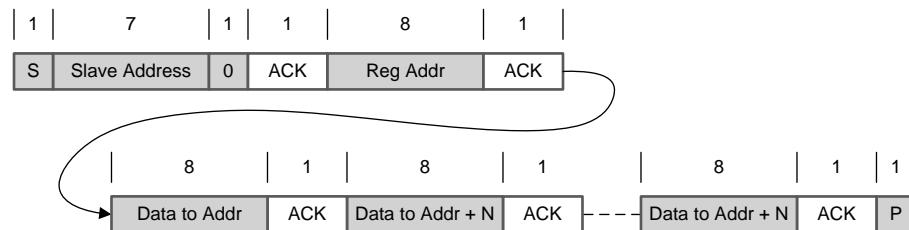


Figure 17. Multi-Write

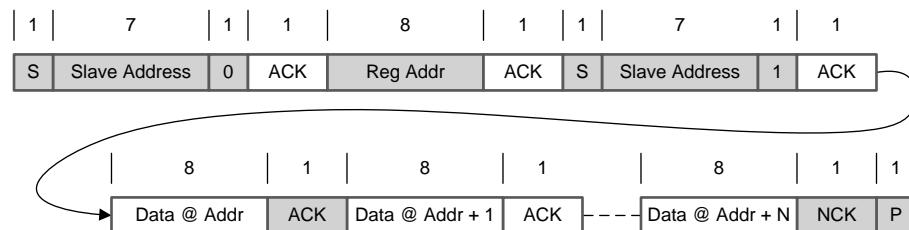


Figure 18. Multi-Read

REG09 is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG09 reports the fault when it is read the first time, but returns to normal when it is read the second time. In order to get the fault information at present, the host has to read REG09 for the second time. The only exception is NTC_FAULT which always reports the actual condition on the TS pin. In addition, REG09 does not support multi-read and multi-write.

8.4 Register Maps

I²C Slave Address: 6AH

8.4.1 REG00

表 5. REG00 Field Descriptions

Bit	Field	POR	Type	Reset	Description	Comment
7	EN_HIZ	0	R/W	by REG_RST by Watchdog	0 – Disable, 1 – Enable	Enable HIZ Mode 0 – Disable (default) 1 – Enable
6	Reserved					
5	Reserved					
4	IINDPM[4]	1	R/W	by REG_RST	1600 mA	Input Current Limit Offset: 100 mA Range: 100 mA (000000) – 3.2 A (1111) Default: maximum input current limit, not typical.
3	IINDPM[3]	0	R/W	by REG_RST	800 mA	
2	IINDPM[2]	1	R/W	by REG_RST	400 mA	
1	IINDPM[1]	1	R/W	by REG_RST	200 mA	
0	IINDPM[0]	1	R/W	by REG_RST	100 mA	IINDPM bits are changed automatically after input source detection is completed bq25600C PSEL = Hi = 500 mA PSEL = Lo = Host can over-write IINDPM register bits after input source detection is completed.

LEGEND: R/W = Read/Write; R = Read only

8.4.2 REG01

表 6. REG01 Field Descriptions

Bit	Field	POR	Type	Reset	Description	Comment
7	PFM_DIS	0	R/W	by REG_RST	0 – Enable PFM 1 – Disable PFM	Default: 0 - Enable
6	WD_RST	0	R/W	by REG_RST by Watchdog	I ² C Watchdog Timer Reset 0 – Normal ; 1 – Reset	Default: Normal (0) Back to 0 after watchdog timer reset
5	Reserved					
4	CHG_CONFIG	1	R/W	by REG_RST by Watchdog	0 - Charge Disable 1- Charge Enable	Default: Charge Battery (1) Note: 1. Charge is enabled when both CE pin is pulled low AND CHG_CONFIG bit is 1.
3	SYS_Min[2]	1	R/W	by REG_RST	System Minimum Voltage	000: 2.6 V
2	SYS_Min[1]	0	R/W	by REG_RST		001: 2.8 V
1	SYS_Min[0]	1	R/W	by REG_RST		010: 3 V
0	Reserved					011: 3.2 V 100: 3.4 V 101: 3.5 V 110: 3.6 V 111: 3.7 V Default: 3.5 V (101)

LEGEND: R/W = Read/Write; R = Read only

8.4.3 REG02

表 7. REG02 Field Descriptions

Bit	Field	POR	Type	Reset	Description	Comment
7	Reserved					
6	Q1_FULLON	0	R/W	by REG_RST	0 – Use higher Q1 RDSON when programmed IINDPM < 700mA (better accuracy) 1 – Use lower Q1 RDSON always (better efficiency)	
5	ICHG[5]		R/W	by REG_RST by Watchdog		Fast Charge Current Default: 2040mA (100010) Range: 0 mA (0000000) – 3000 mA (110010) Note: $I_{CHG} = 0$ mA disables charge. $I_{CHG} > 3000$ mA (110010) clamped to register value 3000 mA (110010))
4	ICHG[4]	0	R/W	by REG_RST by Watchdog		
3	ICHG[3]		R/W	by REG_RST by Watchdog		
2	ICHG[2]		R/W	by REG_RST by Watchdog		
1	ICHG[1]	1	R/W	by REG_RST by Watchdog		
0	ICHG[0]		R/W	by REG_RST by Watchdog		

LEGEND: R/W = Read/Write; R = Read only

8.4.4 REG03

表 8. REG03 Field Descriptions

Bit	Field	POR	Type	Reset	Description	Comment
7	IPRECHG[3]	0	R/W	by REG_RST by Watchdog		Precharge Current Default: 180 mA (0010) Offset: 60 mA Note: IPRECHG > clamped to (1100)
6	IPRECHG[2]	0	R/W	by REG_RST by Watchdog		
5	IPRECHG[1]		R/W	by REG_RST by Watchdog		
4	IPRECHG[0]		R/W	by REG_RST by Watchdog		
3	ITERM[3]	0	R/W	by REG_RST by Watchdog		Termination Current Default: 180 mA (0010) Offset: 60 mA Note: ITERM > 780 mA clamped to (1100)
2	ITERM[2]	0	R/W	by REG_RST by Watchdog		
1	ITERM[1]		R/W	by REG_RST by Watchdog		
0	ITERM[0]		R/W	by REG_RST by Watchdog		

LEGEND: R/W = Read/Write; R = Read only

8.4.5 REG04

表 9. REG04 Field Descriptions

Bit	Field	POR	Type	Reset	Description	Comment
7	VREG[4]	0	R/W	by REG_RST by Watchdog	512 mV	Charge Voltage Offset: 3.856 V
6	VREG[3]	1	R/W	by REG_RST by Watchdog	256 mV	Range: 3.856 V to 4.624 V (11000)
5	VREG[2]	0	R/W	by REG_RST by Watchdog	128 mV	Default: 4.208 V (01011)
4	VREG[1]	1	R/W	by REG_RST by Watchdog	64 mV	Special Value: (01111): 4.352 V
3	VREG[0]	1	R/W	by REG_RST by Watchdog	32 mV	Note: Value above 11000 (4.624 V) is clamped to register value 11000 (4.624 V)
2	Reserved					
1	Reserved					
0	VRECHG	0	R/W	by REG_RST by Watchdog	0 – 100 mV 1 – 200 mV	Recharge threshold Default: 100mV (0)

LEGEND: R/W = Read/Write; R = Read only

8.4.6 REG05

表 10. REG05 Field Descriptions

Bit	Field	POR	Type	Reset	Description	Comment
7	EN_TERM	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Enable	Default: Enable termination (1)
6	OVPFET_DIS	0	R/W	by REG_RST by Watchdog	0 – Enable OVPFET 1 – Disable OVPFET	Default: Enable OVPFET (0) Note: This bit only takes effect when EN_HIZ bit is active
5	WATCHDOG[1]	0	R/W	by REG_RST by Watchdog	00 – Disable timer, 01 – 40 s, 10 – 80 s, 11 – 160 s	Default: 40 s (01)
4	WATCHDOG[0]	1	R/W	by REG_RST by Watchdog		
3	EN_TIMER	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Enable both fast charge and precharge timer	Default: Enable (1)
2	CHG_TIMER	1	R/W	by REG_RST by Watchdog	0 – 5 hrs 1 – 10 hrs	Default: 10 hours (1)
1	TREG	1	R/W	by REG_RST by Watchdog	Thermal Regulation Threshold: 0 - 90°C 1 - 110°C	Default: 110°C (1)
0	Reserved					

LEGEND: R/W = Read/Write; R = Read only

8.4.7 REG06

表 11. REG06 Field Descriptions

Bit	Field	POR	Type	Reset	Description	Comment
7	OVP[1]	0	R/W	by REG_RST		VAC OVP threshold: 00 - 5.5 V 01 – 6.5 V (5-V input) 10 – 10.5 V (9-V input) 11 – 14 V (12-V input)
6	OVP[0]	1	R/W	by REG_RST	Default: 6.5V (01)	
5	Reserved					
4	Reserved					
3	VINDPM[3]	0	R/W	by REG_RST	800 mV	Absolute VINDPM Threshold Offset: 3.9 V Range: 3.9 V (0000) – 5.4 V (1111) Default: 4.5V (0110)
2	VINDPM[2]	1	R/W	by REG_RST	400 mV	
1	VINDPM[1]	1	R/W	by REG_RST	200 mV	
0	VINDPM[0]	0	R/W	by REG_RST	100 mV	

LEGEND: R/W = Read/Write; R = Read only

8.4.8 REG07

表 12. REG07 Field Descriptions

Bit	Field	POR	Type	Reset	Description	Comment
7	Reserved					
6	TMR2X_EN	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Safety timer slowed by 2X during input DPM (both V and I) or thermal regulation	
5	BATFET_DIS	0	R/W	by REG_RST	0 – Allow Q4 turn on, 1 – Turn off Q4 with t_{BATFET_DLY} delay time (REG07[3])	Default: Allow Q4 turn on(0)
4	Reserved					
3	BATFET_DLY	1	R/W	by REG_RST	0 – Turn off BATFET immediately when BATFET_DIS bit is set 1 – Turn off BATFET after t_{BATFET_DLY} (typ. 10 s) when BATFET_DIS bit is set	Default: 1 Turn off BATFET after t_{BATFET_DLY} (typ. 10 s) when BATFET_DIS bit is set
2	BATFET_RST_EN	1	R/W	by REG_RST by Watchdog	0 – Disable BATFET reset function 1 – Enable BATFET reset function	Default: 1 Enable BATFET reset function
1	VDPM_BAT_TRACK[1]	0	R/W	by REG_RST	00 - Disable function (VINDPM set by register) 01 - VBAT + 200mV 10 - VBAT + 250mV 11 - VBAT + 300mV	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of register value and VBAT + VDPM_BAT_TRACK
0	VDPM_BAT_TRACK[0]	0	R/W	by REG_RST		

LEGEND: R/W = Read/Write; R = Read only

8.4.9 REG08

表 13. REG08 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	VBUS_STAT[2]	x	R	NA	VBUS Status register bq25600C
6	VBUS_STAT[1]	x	R	NA	000: No input 001: USB Host SDP (500 mA) → PSEL HIGH 010: Adapter → PSEL LOW 111: Reserved
5	VBUS_STAT[0]	x	R	NA	Software current limit is reported in IINDPM register
4	CHRG_STAT[1]	x	R	NA	Charging status: 00 – Not Charging 01 – Pre-charge (< $V_{BATLOWV}$) 10 – Fast Charging 11 – Charge Termination
2	PG_STAT	x	R	NA	Power Good status: 0 – Power Not Good 1 – Power Good
1	THERM_STAT	x	R	NA	0 – Not in thermAI regulation 1 – in thermAI regulation
0	VSYS_STAT	x	R	NA	0 – Not in VSYSMin regulation (BAT > VSYSMin) 1 – in VSYSMin regulation (BAT < VSYSMin)

LEGEND: R/W = Read/Write

8.4.10 REG09

表 14. REG09 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	WATCHDOG_FAULT	x	R	NA	0 – Normal, 1- Watchdog timer expiration
6	Reserved				
5	CHRG_FAULT[1]	x	R	NA	00 – Normal, 01 – input fault (VAC OVP or VBAT < VBUS < 3.8 V), 10 -
4	CHRG_FAULT[0]	x	R	NA	Thermal shutdown, 11 – Charge Safety Timer Expiration
3	BAT_FAULT	x	R	NA	0 – Normal, 1 – BAT OVP
2	Reserved				
1	Reserved				
0	Reserved				

LEGEND: R/W = Read/Write; R = Read only

8.4.11 REG0A

表 15. REG0A Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	VBUS_GD	x	R	NA	0 – Not VBUS attached, 1 – VBUS Attached
6	VINDPM_STAT	x	R	NA	0 – Not in VINDPM, 1 – in VINDPM
5	IINDPM_STAT	x	R	NA	0 – Not in IINDPM, 1 – in IINDPM
4	Reserved	x	R	NA	
3	Reserved				
2	ACOV_STAT	x	R	NA	0 – Device is NOT in ACOV 1 – Device is in ACOV
1	VINDPM_INT_ MASK	0	R/W	by REG_RST	0 - Allow VINDPM INT pulse 1 - Mask VINDPM INT pulse
0	IINDPM_INT_ MASK	0	R/W	by REG_RST	0 - Allow IINDPM INT pulse 1 - Mask IINDPM INT pulse

LEGEND: R/W = Read/Write; R = Read only

8.4.12 REG0B

表 16. REG0B Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	REG_RST	0	R/W	NA	Register reset 0 – Keep current register setting 1 – Reset to default register value and reset safety timer Note: Bit resets to 0 after register reset is completed
6	PN[3]	x	R	NA	bq25600C: 0110
5	PN[2]	x	R	NA	
4	PN[1]	x	R	NA	
3	PN[0]	x	R	NA	
2	Reserved				
1	DEV_REV[1]	x	R	NA	
0	DEV_REV[0]	x	R	NA	

LEGEND: R/W = Read/Write; R = Read only

9 Application and Implementation

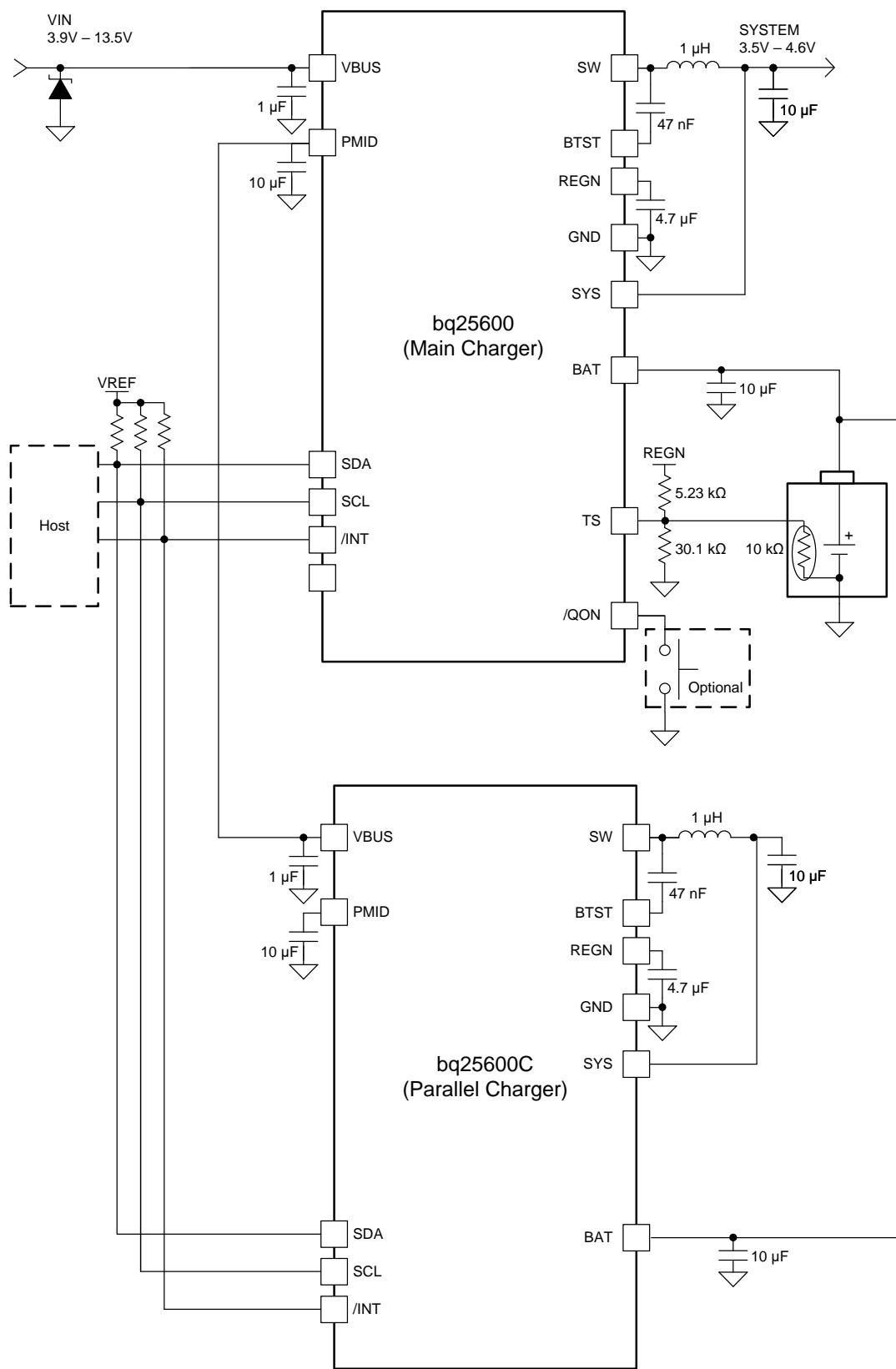
注

information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application information

A typical application consists of the device configured as an I²C controlled parallel charger with a main charger bq25600 to fast charge single cell Li-Ion and Li-polymer batteries used in a wide range of smart phones and other portable devices. bq25600 and bq25660C have different I²C address so that two devices can share the same I²C bus.

9.2 Typical Application Diagram



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图 19. Parallel Charger Application

Typical Application Diagram (接下页)

9.2.1 Design Requirements

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The 1.5-MHz switching frequency allows the use of small inductor and capacitor values to maintain an inductor saturation current higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2) I_{RIPPLE} \quad (1)$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle ($D = V_{BAT}/V_{VBUS}$), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{f_S \times L} \quad (2)$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5. Usually inductor ripple is designed in the range between 20% and 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.

9.2.2.2 Input Capacitor

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated using [公式 3](#).

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (3)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25-V or higher capacitor is preferred for 15 V input voltage. Capacitance of 22- μ F is suggested for typical of 3A charging current.

9.2.2.3 Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. [公式 4](#) shows the output capacitor RMS current I_{COUT} calculation.

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (4)$$

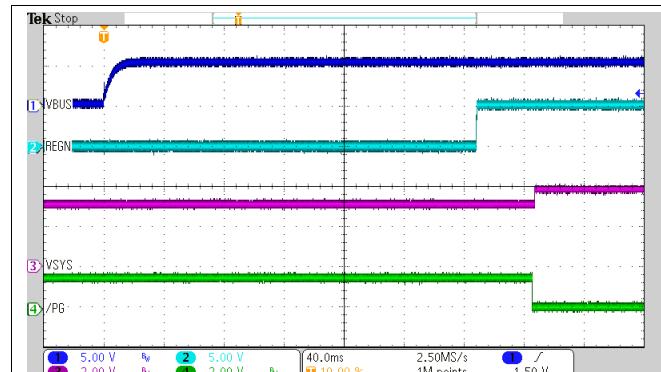
The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCf^2} \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \quad (5)$$

At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The charger device has internal loop compensation optimized for >20 μ F ceramic output capacitance. The preferred ceramic capacitor is 10V rating, X7R or X5R.

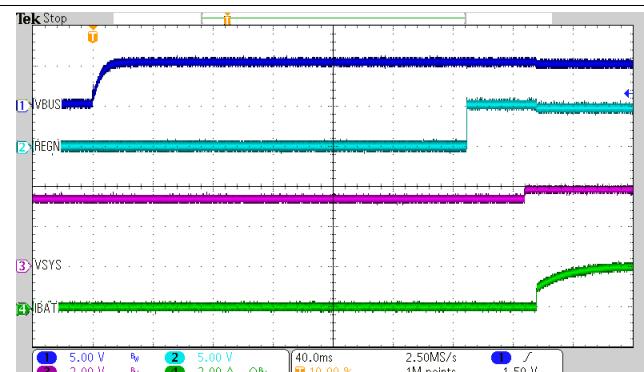
9.3 Application Curves



$V_{VBUS} = 5 \text{ V}$

$V_{VBAT} = 3.2 \text{ V}$

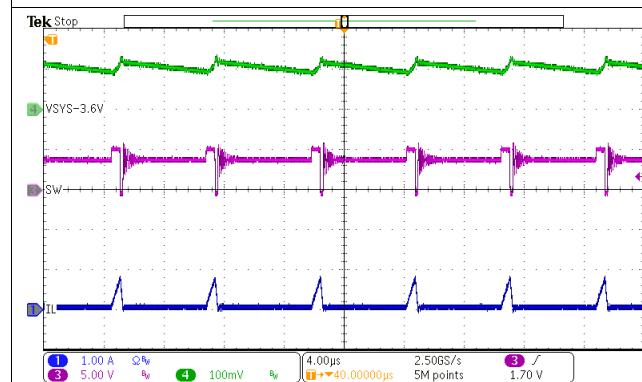
图 20. Power-Up with Charge Disabled



$V_{VBUS} = 5 \text{ V}$

$V_{VBAT} = 3.2 \text{ V}$

图 21. Power-Up with Charge Enabled

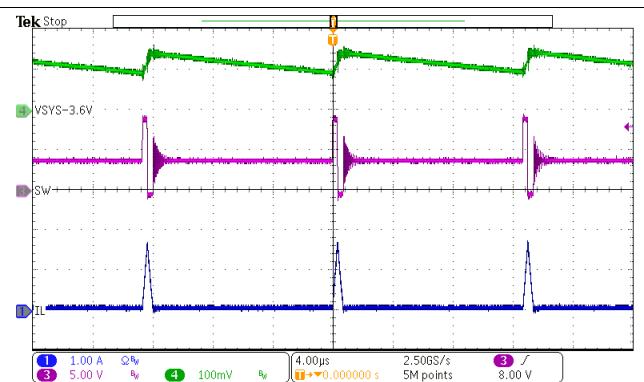


$V_{VBUS} = 5 \text{ V}$

$I_{SYS} = 50 \text{ mA}$

Charge Disabled

图 22. PFM Switching in Buck Mode

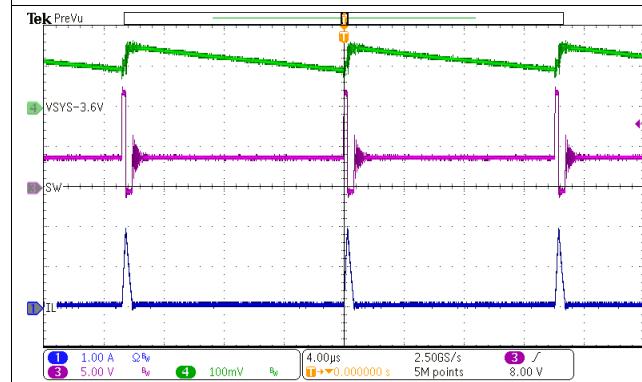


$V_{VBUS} = 9 \text{ V}$

$I_{SYS} = 50 \text{ mA}$

Charge Disabled

图 23. PFM Switching in Buck Mode

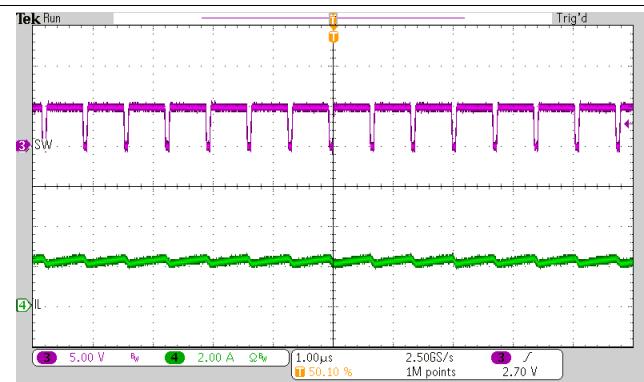


$V_{VBUS} = 12 \text{ V}$

$I_{SYS} = 50 \text{ mA}$

Charge Disabled

图 24. PFM Switching in Buck Mode



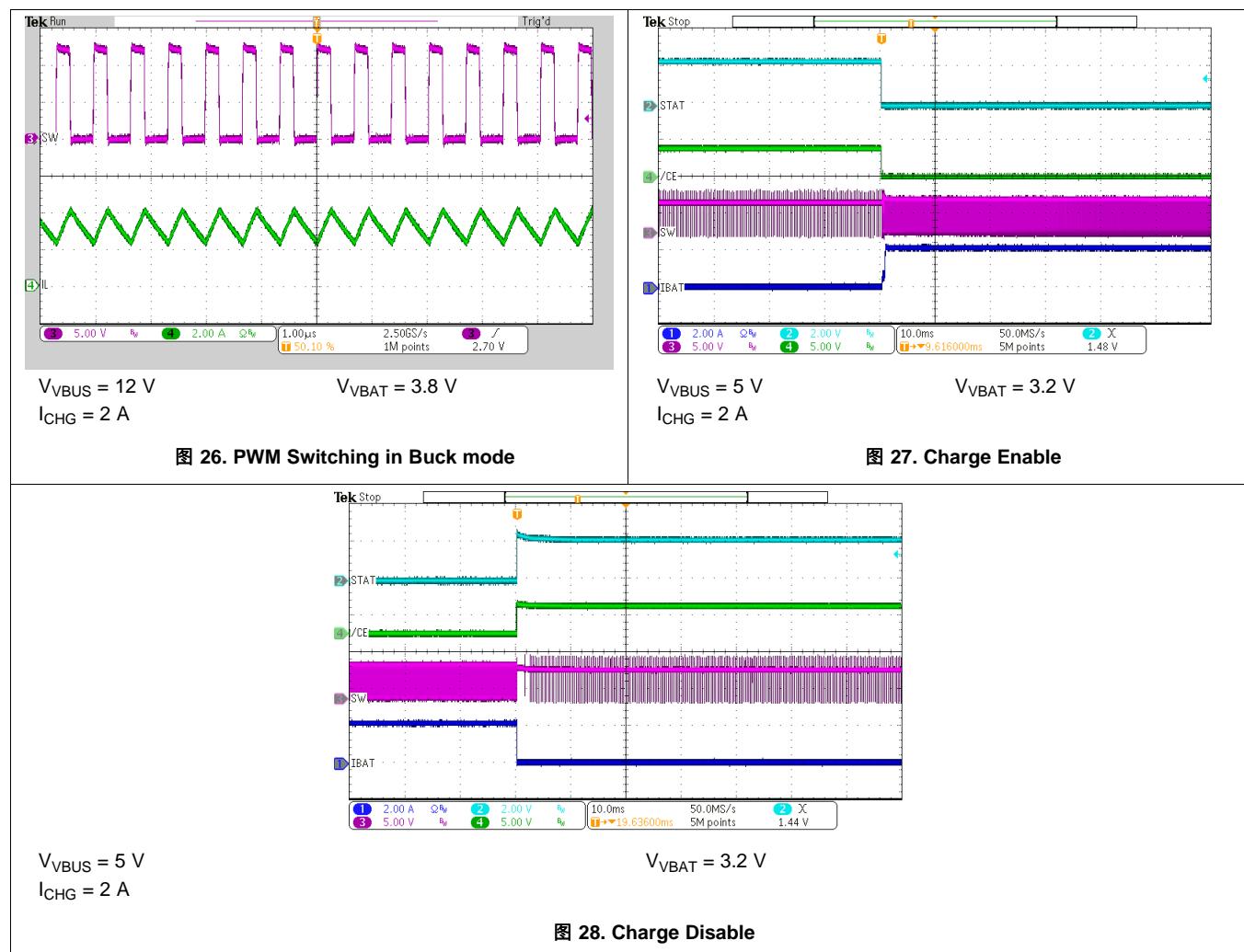
$V_{VBUS} = 5 \text{ V}$

$I_{CHG} = 2 \text{ A}$

$V_{VBAT} = 3.8 \text{ V}$

图 25. PWM Switching in Buck Mode

Application Curves (接下页)



10 Power Supply Recommendations

In order to provide an output voltage on the SYS pins, the bq25600C device requires a power supply between 3.9 V and 14.2 V input with at least 100-mA current rating connected to VBUS and a single-cell Li-Ion battery with voltage $> V_{BATUVLO}$ connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter of the charger to provide maximum output power to SYS.

11 Layout

11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see [图 29](#)) is important to prevent electrical and magnetic field radiation and high frequency resonant problems.

IMPORTANT

It is essential to follow this specific layout PCB order.

- Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
- Put output capacitor near to the inductor and the device.
- Decoupling capacitors should be placed next to the device pins and make trace connection as short as possible.
- Place inductor input terminal to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
- It is OK to connect all grounds together to reduce PCB size and improve thermal dissipation.
- Try to avoid ground planes in parallel with high frequency traces in other layers.

See the EVM design for the recommended component placement with trace and via locations.

11.2 Layout Example

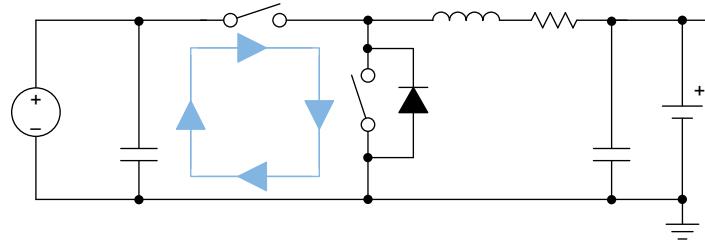


图 29. High Frequency Current Path

12 器件和文档支持

12.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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设计支持 [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.2 商标

E2E is a trademark of Texas Instruments.

12.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25600CYFFR	Active	Production	DSBGA (YFF) 30	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25600C
BQ25600CYFFR.A	Active	Production	DSBGA (YFF) 30	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25600C
BQ25600CYFFR.B	Active	Production	DSBGA (YFF) 30	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25600C
BQ25600CYFFT	Active	Production	DSBGA (YFF) 30	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25600C
BQ25600CYFFT.A	Active	Production	DSBGA (YFF) 30	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25600C
BQ25600CYFFT.B	Active	Production	DSBGA (YFF) 30	250 SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25600C

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

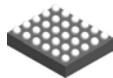
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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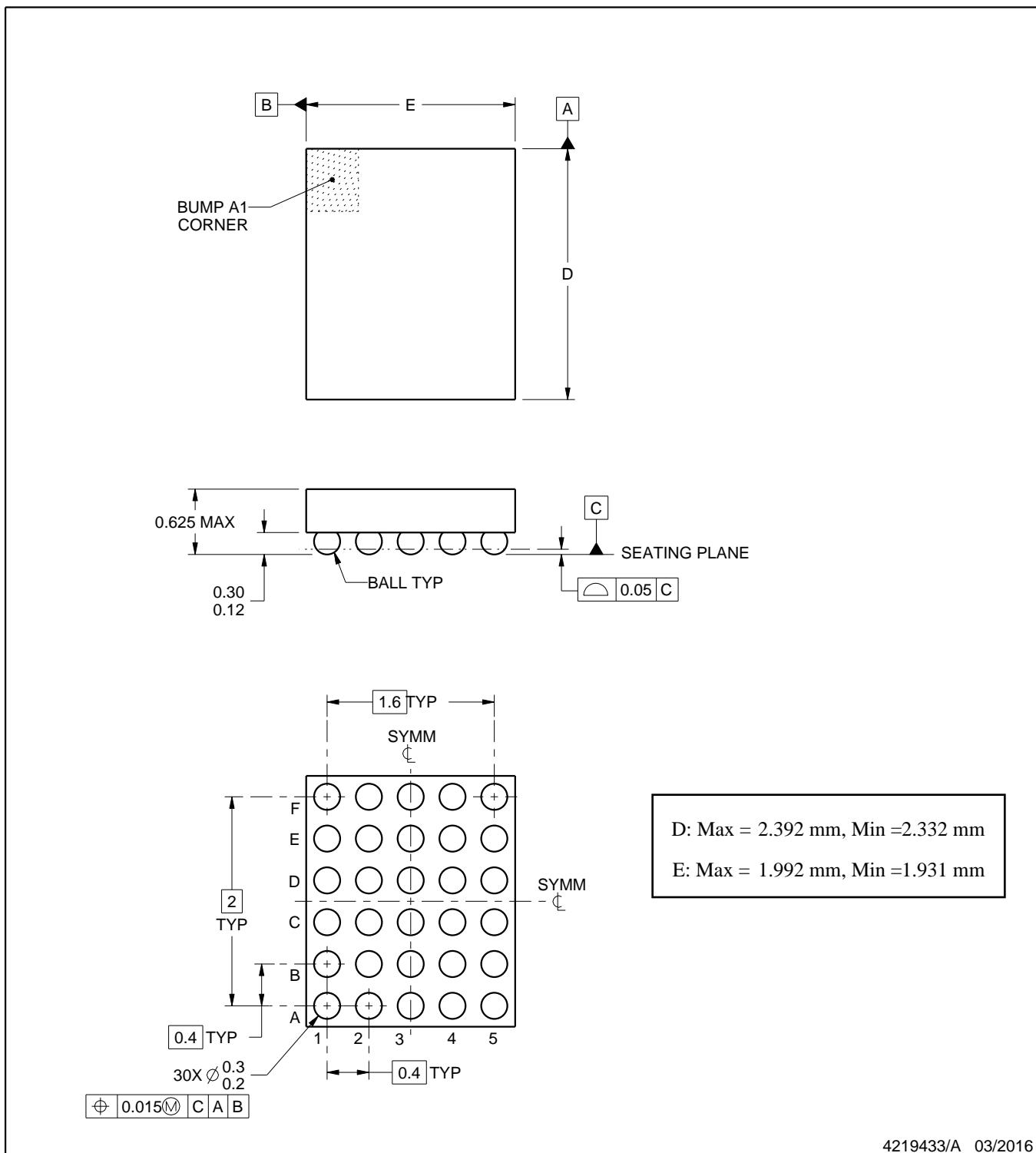
PACKAGE OUTLINE

YFF0030



DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



4219433/A 03/2016

NOTES:

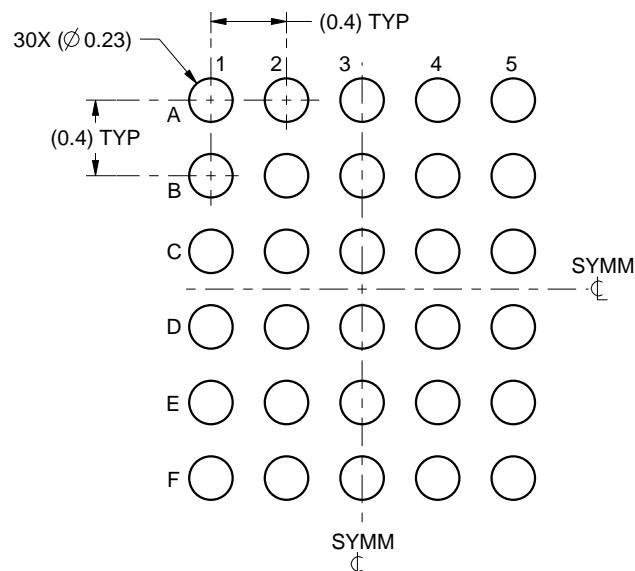
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

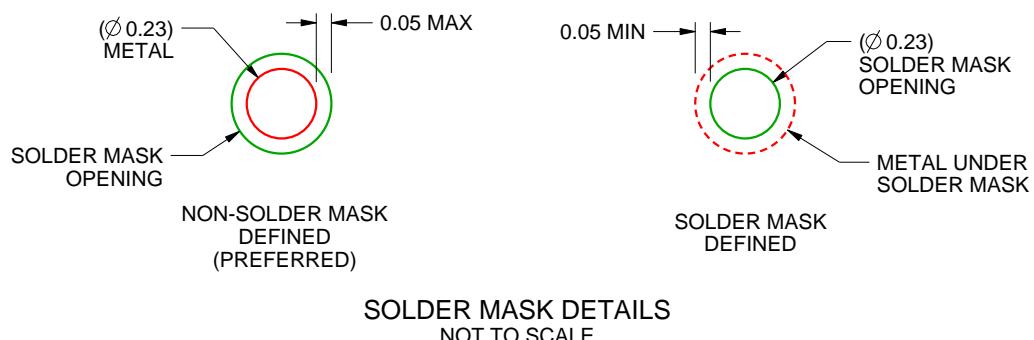
YFF0030

DSBGA - 0.625 mm max height

PIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE



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NOTES: (continued)

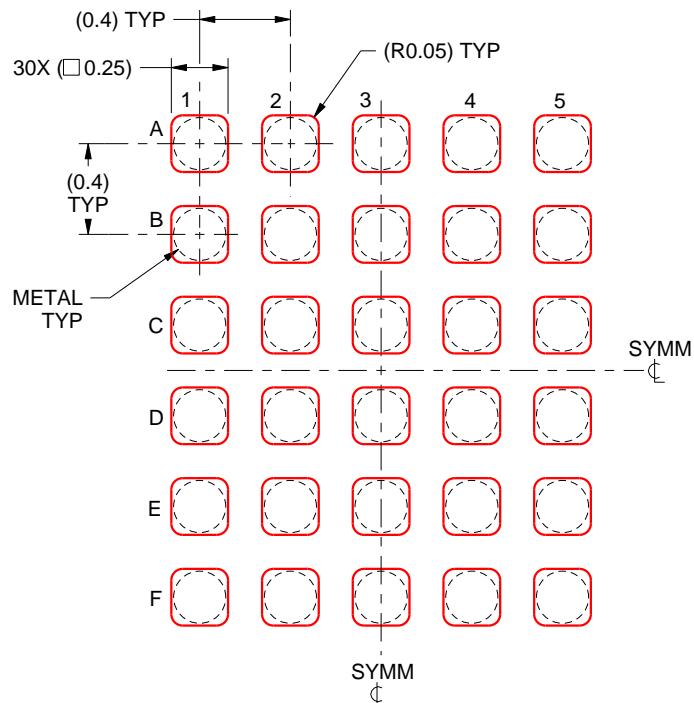
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0030

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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