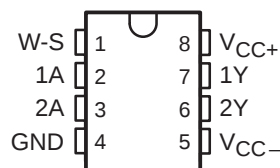


uA9636AC DUAL LINE DRIVER WITH ADJUSTABLE SLEW RATE

SLLS110B – OCTOBER 1980 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-423-B and -232-E and ITU Recommendations V.10 and V.28
- Output Slew Rate Control
- Output Short-Circuit-Current Limiting
- Wide Supply Voltage Range
- 8-Pin Package
- Designed to Be Interchangeable With National DS9636A

D OR P PACKAGE
(TOP VIEW)

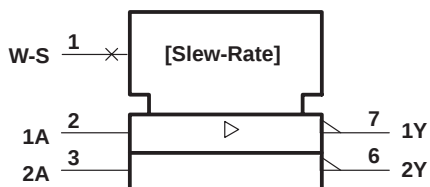


description

The uA9636AC is a dual, single-ended line driver designed to meet ANSI Standards EIA/TIA-423-B and EIA/TIA-232-E and ITU Recommendations V.10 and V.28. The slew rates of both amplifiers are controlled by a single external resistor, R_{WS} , connected between the wave-shape-control (W-S) terminal and GND. Output current limiting is provided. Inputs are compatible with TTL and CMOS and are diode protected against negative transients. This device operates from ± 12 V and is supplied in an 8-pin package.

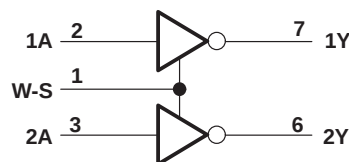
The uA9636AC is characterized for operation from 0°C to 70°C .

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



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**TEXAS
INSTRUMENTS**

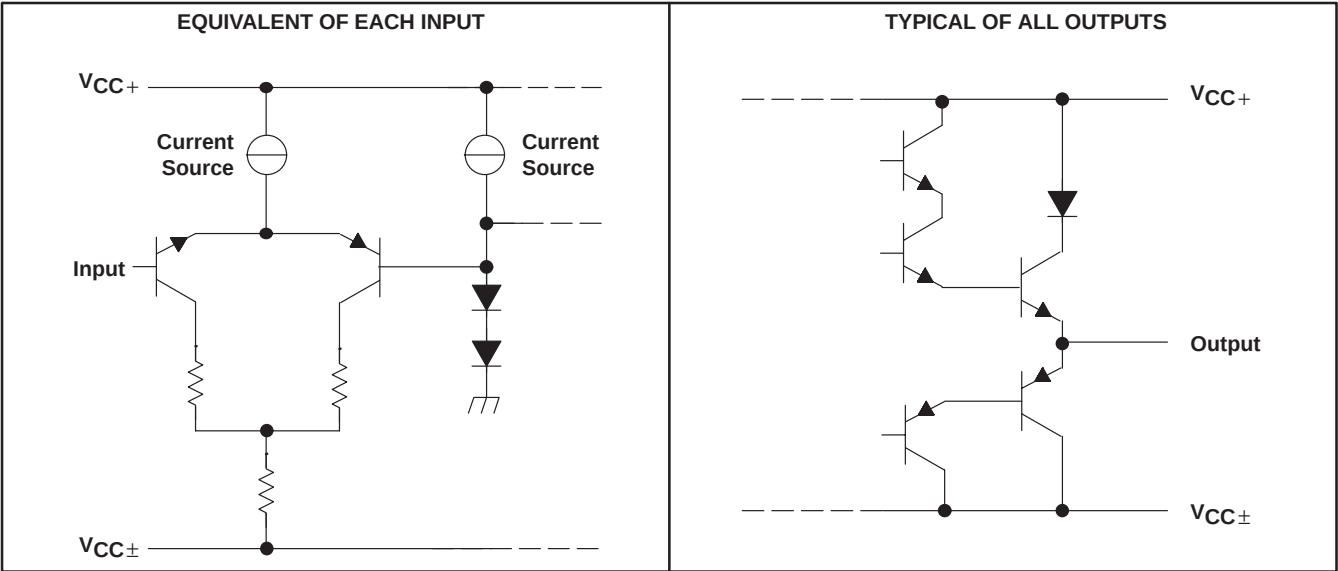
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uA9636AC
DUAL LINE DRIVER WITH ADJUSTABLE SLEW RATE

SLLS110B – OCTOBER 1980 – REVISED MAY 1995

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Positive supply voltage range, V_{CC+} (see Note 1)	V_{CC-} to 15 V
Negative supply voltage range, V_{CC-}	0.5 V to -15 V
Output voltage, V_O	± 15 V
Output current, I_O	± 150 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC+}	10.8	12	13.2	V
Negative supply voltage, V_{CC-}	-10.8	-12	-13.2	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Wave-shaping resistor, $R_{(WS)}$	10		1000	kΩ
Operating free-air temperature, T_A	0		70	°C

uA9636AC

DUAL LINE DRIVER WITH ADJUSTABLE SLEW RATE

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electrical characteristics over recommended ranges of free-air temperature, supply voltage, and wave-shaping resistance (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V _{IK} Input clamp voltage	I _I = –15 mA		–1.1	–1.5		V
V _{OH} High-level output voltage	V _I = 0.8 V	R _L = ∞	5	5.6	6	V
		R _L = 3 kΩ to GND	5	5.6	6	
		R _L = 450 Ω to GND	4	5.4	6	
V _{OL} Low-level output voltage	V _I = 2 V	R _L = ∞	–6 [‡]	–5.7	–5	V
		R _L = 3 kΩ to GND	–6 [‡]	–5.6	–5	
		R _L = 450 Ω to GND	–6 [‡]	–5.4	–4	
I _{IH} High-level input current	V _I = 2.4 V				10	μA
	V _I = 5.5 V				100	
I _{IL} Low-level input current	V _I = 0.4 V		–20	–80		μA
I _O Output current (power off)	V _{CC±} = 0, V _O = ±6 V				±100	μA
I _{OS} Short-circuit output current [§]	V _I = 2 V		15	25	150	mA
	V _I = 0		–15	–40	–150	
r _O Output resistance	R _L = 450 Ω			25	50	Ω
I _{CC+} Positive supply current	V _{CC} = ±12 V, R _(WS) = 100 kΩ, V _I = 0, Output open			13	18	mA
I _{CC–} Negative supply current	V _{CC} = ±12 V, R _(WS) = 100 kΩ, V _I = 0, Output open		–13	–18		mA

[†] All typical values are at V_{CC} = ±12 V, T_A = 25°C.

[‡] The algebraic convention, in which the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for logic voltage levels, e.g., when –5 V is the maximum, the minimum is a more-negative voltage.

[§] Not more than one output should be shorted to ground at a time.

switching characteristics, V_{CC±} = ±12 V, T_A = 25°C (see Figure 1)

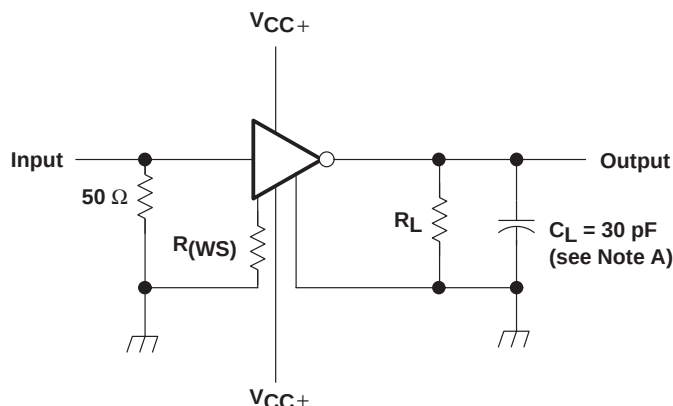
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{TLH} Transition time, low- to high-level output	R _L = 450 kΩ, C _L = 30 pF	R _(WS) = 10 kΩ	0.8	1.1	1.4	μs
		R _(WS) = 100 kΩ	8	11	14	
		R _(WS) = 500 kΩ	40	55	70	
		R _(WS) = 1 MΩ	80	110	140	
t _{THL} Transition time, high- to low-level output	R _L = 450 kΩ, C _L = 30 pF	R _(WS) = 10 kΩ	0.8	1.1	1.4	μs
		R _(WS) = 100 kΩ	8	11	14	
		R _(WS) = 500 kΩ	40	55	70	
		R _(WS) = 1 MΩ	80	110	140	



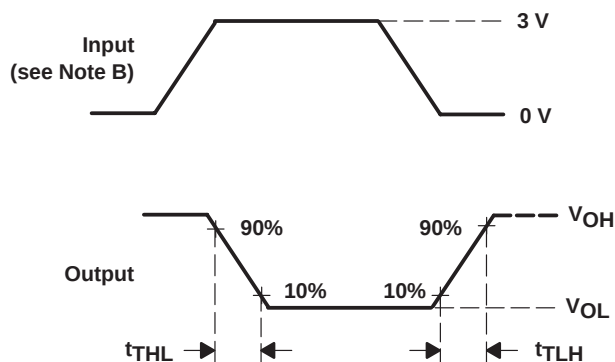
uA9636AC DUAL LINE DRIVER WITH ADJUSTABLE SLEW RATE

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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$, $PRR \leq 1$ kHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

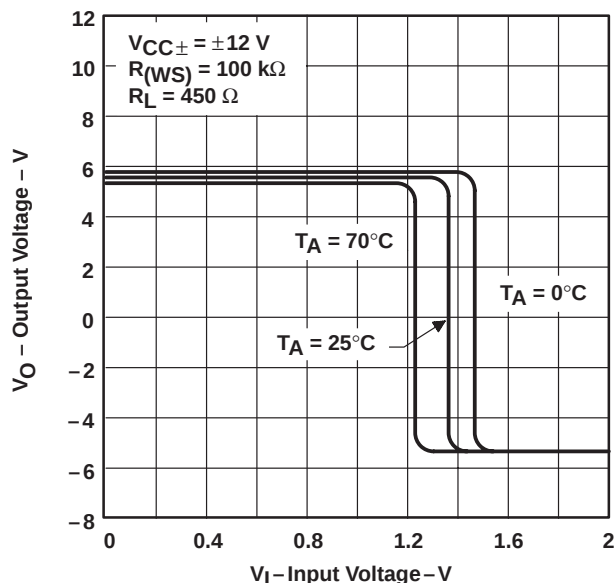


Figure 2

INPUT CURRENT
vs
INPUT VOLTAGE

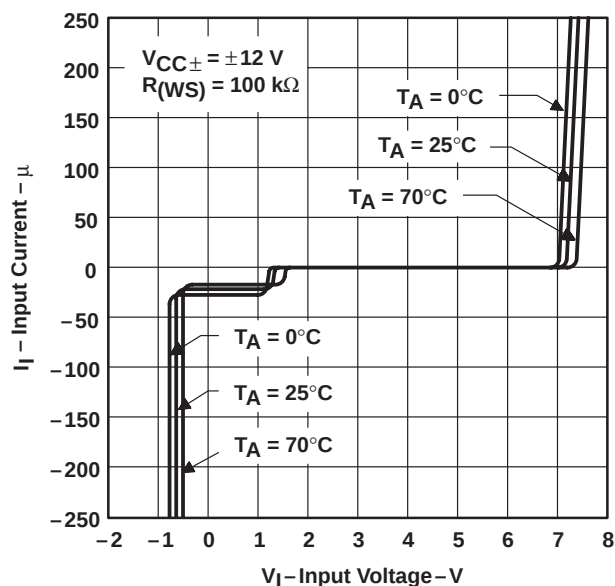
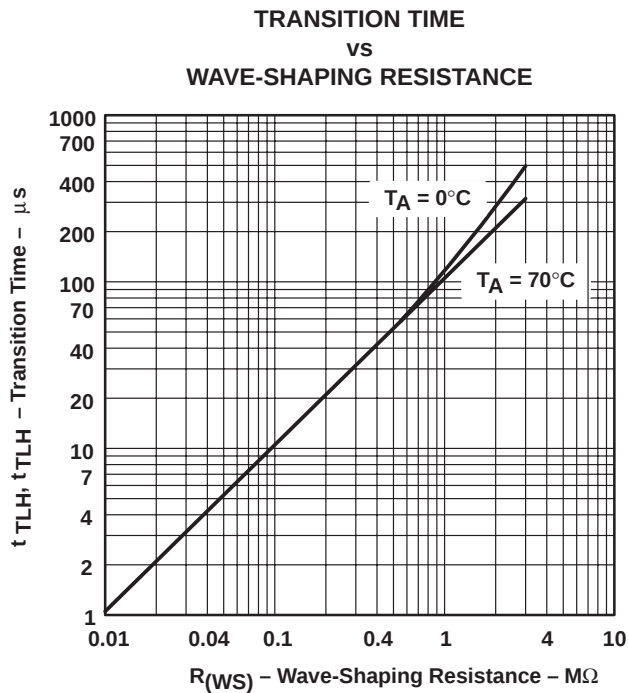
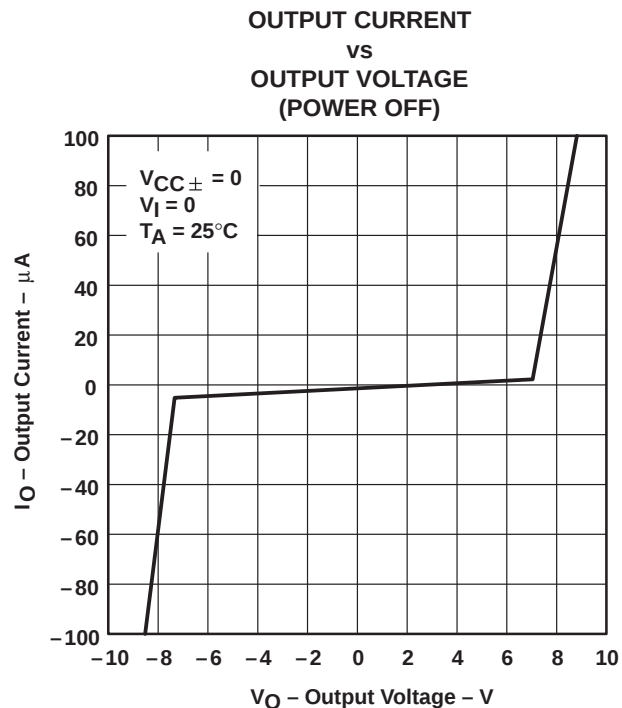
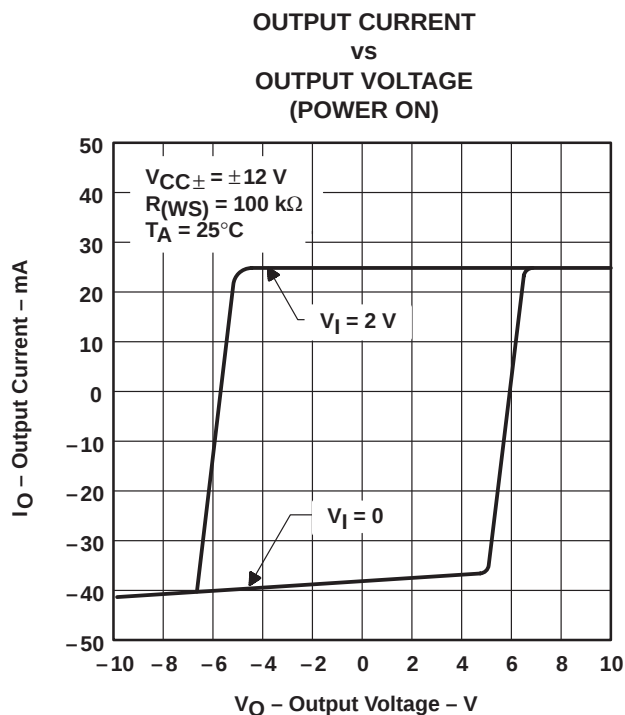


Figure 3

TYPICAL CHARACTERISTICS



uA9636AC

DUAL LINE DRIVER WITH ADJUSTABLE SLEW RATE

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APPLICATION INFORMATION

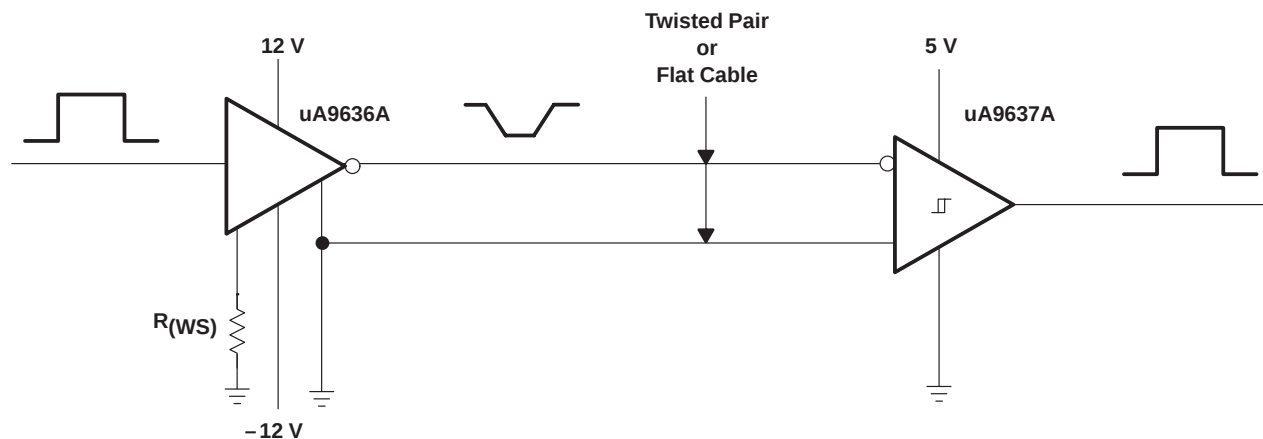


Figure 7. EIA/TIA-423-B System Application

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UA9636ACD	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	9636AC
UA9636ACD.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	9636AC
UA9636ACDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	9636AC
UA9636ACDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	9636AC
UA9636ACP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UA9636ACP
UA9636ACP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UA9636ACP
UA9636ACPE4	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UA9636ACP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA9636ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA9636ACDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UA9636ACD	D	SOIC	8	75	507	8	3940	4.32
UA9636ACD.A	D	SOIC	8	75	507	8	3940	4.32
UA9636ACP	P	PDIP	8	50	506	13.97	11230	4.32
UA9636ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
UA9636ACPE4	P	PDIP	8	50	506	13.97	11230	4.32



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



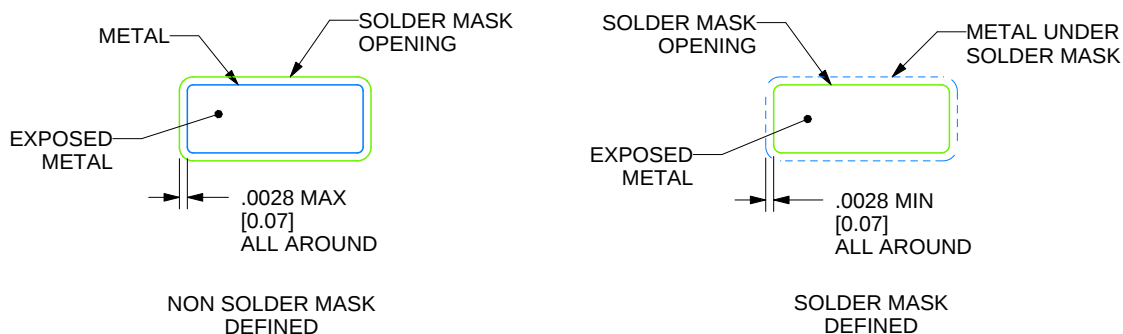
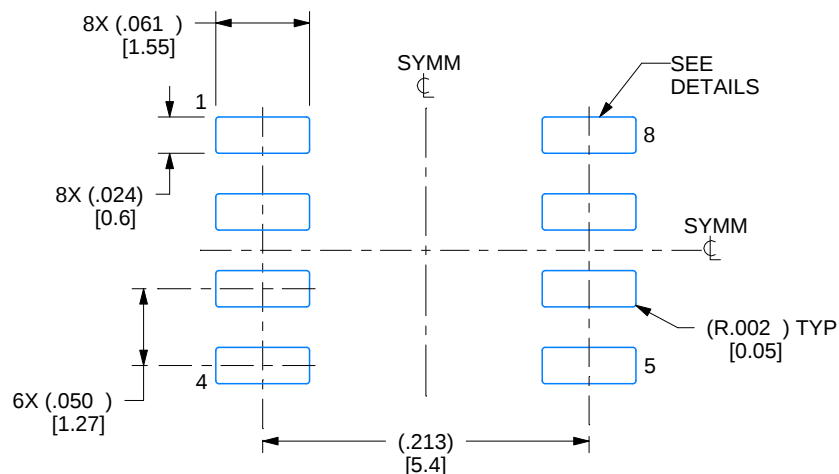
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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