

# TPA6132A2 具有杂音抑制功能的 25mW DirectPath™ 立体声耳机放大器

## 1 特性

- 有了获得专利的 DirectPath™ 技术，便不再需要隔直电容器
  - 0V 时的输出偏置
  - 卓越的低频保真度
- 主动抑制喀嗒/噼啪噪声
- 2.1mA 电源电流（典型值）
- 全差动或单端输入
  - 内置电阻减少了组件数
  - 改善了系统噪声性能
- 2.3V 至 5.5V 电源提供恒定最大输出功率
  - 简化了设计以防声震
- 改善了 RF 噪声抗扰度
- 符合 Microsoft™ Windows Vista™ 标准
- 高电源噪声抑制
  - 在 217Hz 时为 100dB PSRR
  - 在 10kHz 时为 90dB PSRR
- 宽电源范围：2.3V 至 5.5V
- 增益设置：-6dB、0dB、3dB 和 6dB
- 短路和过热保护
- 对输出提供了  $\pm 8kV$  HBM ESD 保护
- 提供小封装
  - 16 引脚、3mm x 3mm 超薄 QFN

## 2 应用范围

- 智能电话/手机
- 笔记本电脑
- CD/MP3 播放器
- 便携式游戏机

## 3 说明

TPA6132A2（有时称作 TPA6132）是 DirectPath™ 立体声耳机放大器，无需使用外部直流阻隔输出电容。差动立体声输入和内置电阻设置器件增益，进一步减少了外部组件数。增益可以选择 -6dB、0dB、3dB 或 6dB。该放大器使用单个 2.3V 电源为 16Ω 扬声器提供 25mW 功率。TPA6132A2 (TPA6132) 提供独立于电源电压的恒定最大输出功率，从而为防声震设计提供了方便。

TPA6132A2 采用全差动输入，以减少音频源与耳机放大器之间的系统噪声拾取。高电源噪声抑制性能和差动架构增加了射频噪声抗扰度。对于单端输入信号，请将 INL+ 和 INR+ 接地。

该器件具有内置杂音抑制电路，可以完全消除开启和关闭期间的噼啪噪声干扰。放大器输出具有短路和过热保护以及  $\pm 8kV$  HBM ESD 保护，简化了终端设备符合 IEC 61000-4-2 ESD 标准的工作。

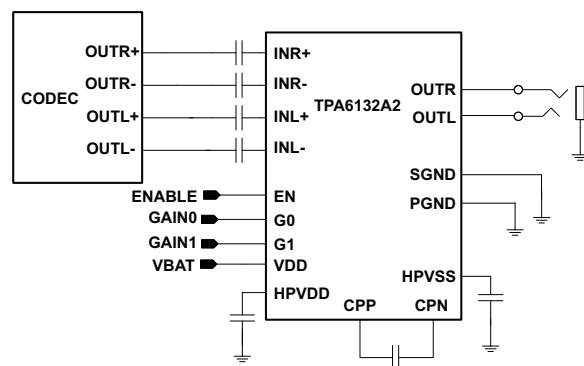
TPA6132A2 由一个 2.3V 至 5.5V 的单电源供电，电源电流典型值为 2.1mA。关断模式可将电源电流减少至  $1\mu A$  以下。

### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸（标称值）
TPA6132A2	WQFN (16)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## 目录

<b>1</b>	<b>特性</b> .....	<b>1</b>	7.4	Device Functional Modes.....	13
<b>2</b>	<b>应用范围</b> .....	<b>1</b>	<b>8</b>	<b>Application and Implementation</b> .....	<b>14</b>
<b>3</b>	<b>说明</b> .....	<b>1</b>	8.1	Application Information.....	14
<b>4</b>	<b>修订历史记录</b> .....	<b>2</b>	8.2	Typical Applications .....	14
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	<b>9</b>	<b>Power Supply Recommendations</b> .....	<b>17</b>
<b>6</b>	<b>Specifications</b> .....	<b>4</b>	9.1	Power Supply and HPVDD Decoupling Capacitors	17
6.1	Absolute Maximum Ratings .....	4	<b>10</b>	<b>Layout</b> .....	<b>18</b>
6.2	ESD Ratings .....	4	10.1	Layout Guidelines .....	18
6.3	Recommended Operating Conditions.....	4	10.2	Layout Example .....	18
6.4	Thermal Information .....	4	10.3	GND Connections .....	18
6.5	Electrical Characteristics.....	5	<b>11</b>	<b>器件和文档支持</b> .....	<b>19</b>
6.6	Operating Characteristics.....	5	11.1	接收文档更新通知 .....	19
6.7	Typical Characteristics.....	6	11.2	社区资源 .....	19
<b>7</b>	<b>Detailed Description</b> .....	<b>10</b>	11.3	商标 .....	19
7.1	Overview .....	10	11.4	静电放电警告 .....	19
7.2	Functional Block Diagram .....	10	11.5	Glossary .....	19
7.3	Feature Description.....	11	<b>12</b>	<b>机械、封装和可订购信息</b> .....	<b>19</b>

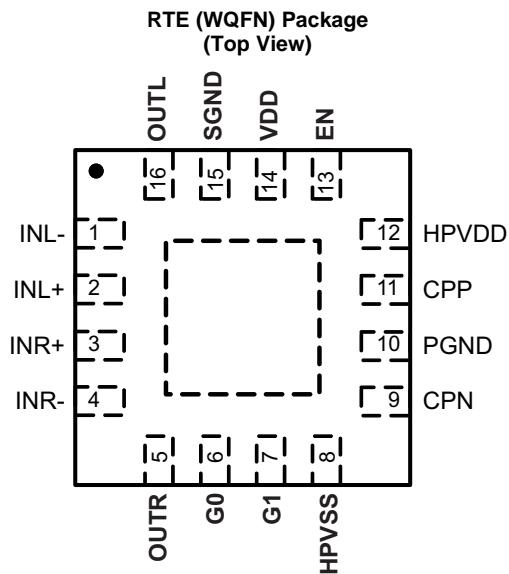
**4 修订历史记录**

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (December 2008) to Revision B	Page
• Corrected the I/O/P column of the <i>Pin Functions</i> table .....	3
• Changed the Input voltage for EN, G0, G1 MAX value From: HVDD + 0.3 To: VDD + 0.3 in the <i>Absolute Maximum Ratings</i> .....	4
• Changed Handling Ratings to <i>ESD Ratings</i> and moved the Storage temperature range to the <i>Absolute Maximum Ratings</i> .....	4

Changes from Original (December 2008) to Revision A	Page
• 添加了处理额定值表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械和封装部分。 .....	1
• Added Input voltage: EN, G0, G1 to the <i>Absolute Maximum Ratings</i> table.....	4
• Added Input voltage: INR+, INR-, INL+, INL- to the <i>Recommended Operating Conditions</i> table.....	4
• Changed Output impedance in shutdown From: TYP = 50 $\Omega$ To: TYP = 20 $\Omega$ in the <i>Operating Characteristics</i> table .....	5

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O/P	DESCRIPTION
NAME	NO.		
INL-	1	I	Inverting left input for differential signals; left input for single-ended signals
INL+	2	I	Non-inverting left input for differential signals. Connect to ground for single-ended input applications
INR+	3	I	Non-inverting right input for differential signals. Connect to ground for single-ended input applications
INR-	4	I	Inverting right input for differential signals; right input for single-ended signals
OUTR	5	O	Right headphone amplifier output. Connect to right terminal of headphone jack
G0	6	I	Gain select
GAIN0		I	
G1	7	I	Gain select
GAIN1		I	
HPVSS	8	P	Charge pump output and negative power supply for output amplifiers; connect 1µF capacitor to GND
CPN	9	P	Charge pump negative flying cap. Connect to negative side of 1µF capacitor between CPP and CPN
PGND	10	P	Ground
CPP	11	P	Charge pump positive flying cap. Connect to positive side of 1µF capacitor between CPP and CPN
HPVDD	12	P	Positive power supply for headphone amplifiers. Connect to a 2.2µF capacitor. Do not connect to VDD
EN	13	I	Amplifier enable. Connect to logic low to shutdown; connect to logic high to activate
VDD	14	P	Positive power supply for TPA6132A2
SGND	15	P	Amplifier reference voltage. Connect to ground terminal of headphone jack
OUTL	16	O	Left headphone amplifier output. Connect to left terminal of headphone jack
Thermal Pad	–		Solder the exposed metal pad on the TPA6132A2RTE QFN package to the landing pad on the PCB. Connect the landing pad to ground or leave it electrically unconnected (floating).

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	VDD	-0.3	6	V
Headphone amplifier supply voltage	HPVDD (do not connect to external supply)	-0.3	1.9	V
Input voltage, $V_I$	INR+, INR-, INL+, INL-	HPVSS -0.3	HPVDD + 0.3	V
	EN, G0, G1	-0.3	VDD + 0.3	V
Output continuous total power dissipation		See <i>Thermal Information</i>		
Operating free-air temperature range, $T_A$		-40	85	°C
Operating junction temperature range, $T_J$		-40	150	°C
Storage temperature range, $T_{\text{stg}}$		-65	85	°C

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(\text{ESD})}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	OUTL, OUTR	$\pm 8000$
			All Other Pins	$\pm 2000$
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	$\pm 1500$	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
	Supply voltage, VDD	2.3	5.5	V
$V_{IH}$	High-level input voltage; EN, G0, G1	1.3		V
$V_{IL}$	Low-level input voltage; EN, G0, G1		0.6	V
$V_I$	Input voltage; INR+, INR-, INL+, INL-	0	HPVDD + 0.3	V
	Voltage applied to Output; OUTR, OUTL (when EN = 0 V)	-0.3	3.6	V
$T_A$	Operating free-air temperature	-40	85	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	RTE	UNIT
	16 PINS	
$R_{\theta JA}$	51.1	°C/W
$R_{\theta JC(\text{top})}$	53.9	
$R_{\theta JB}$	24.3	
$\Psi_{JT}$	0.9	
$\Psi_{JB}$	24.3	
$R_{\theta JC(\text{bot})}$	9.0	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output offset voltage		-0.5	0.5	0.5	mV
Power supply rejection ratio	$V_{DD} = 2.3 \text{ V to } 5.5 \text{ V}$	100			dB
High-level output current (EN, G0, G1)			1	1	$\mu\text{A}$
Low-level output current (EN, G0, G1)			1	1	$\mu\text{A}$
Supply Current	$V_{DD} = 2.3 \text{ V, No load, EN} = V_{DD}$	2.1	3.1	3.1	mA
	$V_{DD} = 3.6 \text{ V, No load, EN} = V_{DD}$	2.1	3.1	3.1	
	$V_{DD} = 5.5 \text{ V, No load, EN} = V_{DD}$	2.2	3.2	3.2	
	$EN = 0 \text{ V, } V_{DD} = 2.3 \text{ V to } 5.5 \text{ V}$	0.7	1.2	1.2	

## 6.6 Operating Characteristics

$V_{DD} = 3.6 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 16 \Omega$  (unless otherwise noted)

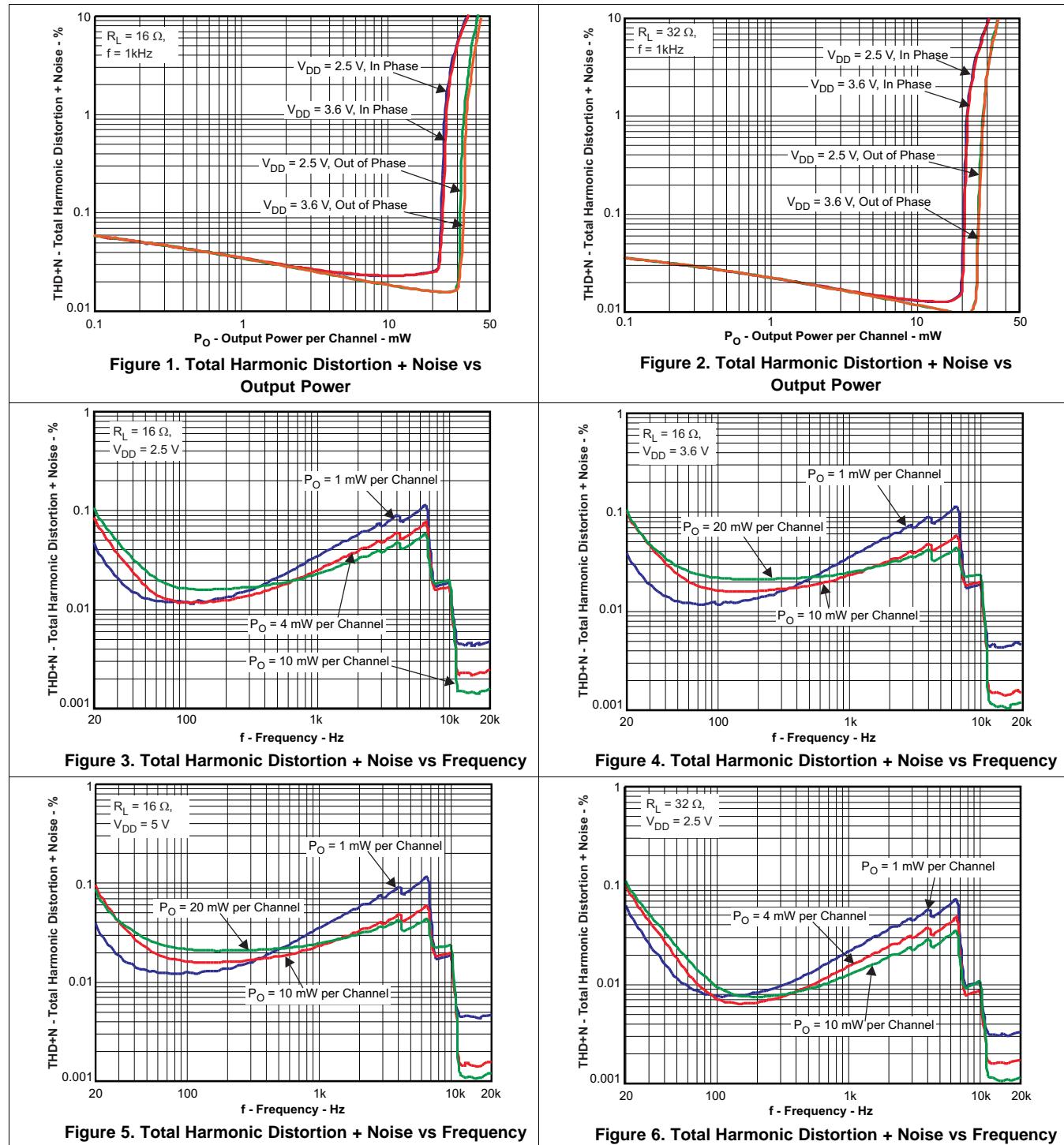
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_O$	THD = 1%, $f = 1 \text{ kHz}$	25			mW
	THD = 1%, $f = 1 \text{ kHz, } R_L = 32 \Omega$	22			
$V_O$	Output voltage <sup>(1)</sup> (Outputs in phase)	1.1			$\text{V}_{\text{RMS}}$
$A_V$	$G_0 = 0 \text{ V, } G_1 = 0 \text{ V, } (-6 \text{ dB})$	-0.45	-0.5	-0.55	V/V
	$G_0 \geq 1.3 \text{ V, } G_1 = 0 \text{ V, } (0 \text{ dB})$	-0.95	-1.0	-1.05	
	$G_0 = 0 \text{ V, } G_1 \geq 1.3 \text{ V, } (3 \text{ dB})$	-1.36	-1.41	-1.46	
	$G_0 \geq 1.3 \text{ V, } G_1 \geq 1.3 \text{ V, } (6 \text{ dB})$	-1.95	-2.0	-2.05	
$\Delta A_V$	Gain matching	Between Left and Right channels	1%		
$R_{IN}$	$G_0 = 0 \text{ V, } G_1 = 0 \text{ V, } (-6 \text{ dB})$	26.4			k $\Omega$
	$G_0 \geq 1.3 \text{ V, } G_1 = 0 \text{ V, } (0 \text{ dB})$	19.8			
	$G_0 = 0 \text{ V, } G_1 \geq 1.3 \text{ V, } (3 \text{ dB})$	16.5			
	$G_0 \geq 1.3 \text{ V, } G_1 \geq 1.3 \text{ V, } (6 \text{ dB})$	13.2			
$V_{CM}$	Input common-mode voltage range		-0.5	1.5	V
	Output impedance in shutdown		20		$\Omega$
	Input-to-output attenuation in shutdown	EN = 0 V	80		dB
$k_{SVR}$	AC-power supply rejection ratio	200 mV <sub>pp</sub> ripple, $f = 217 \text{ Hz}$		-100	dB
		200 mV <sub>pp</sub> ripple, $f = 10 \text{ kHz}$		-90	
THD+N	Total harmonic distortion plus noise <sup>(2)</sup>	$P_O = 20 \text{ mW, } f = 1 \text{ kHz}$	0.02%		
		$P_O = 25 \text{ mW into } 32 \Omega, V_{DD} = 5.5 \text{ V, } f = 1 \text{ kHz}$	0.01%		
SNR	Signal-to-noise ratio	$P_O = 20 \text{ mW; } G_0 \geq 1.3 \text{ V, } G_1 = 0 \text{ V, } (A_V = 0 \text{ dB})$	100		dB
$E_n$	Noise output voltage	A-weighted	5.5		$\mu\text{V}_{\text{RMS}}$
$f_{osc}$	Charge pump switching frequency		1200	1275	1350
$t_{ON}$	Start-up time from shutdown		5		ms
	Crosstalk	$P_O = 20 \text{ mW, } f = 1 \text{ kHz}$	-80		dB
	Thermal shutdown	Threshold	150		°C
		Hysteresis	20		°C

(1) Per output channel

(2) A-weighted

## 6.7 Typical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.6\text{ V}$ , Gain = 0 dB, EN = 3.6 V,  $C_{HPVDD} = C_{HPVSS} = 2.2\text{ }\mu\text{F}$ ,  $C_{INPUT} = C_{FLYING} = 1\text{ }\mu\text{F}$ , Outputs in Phase



## Typical Characteristics (continued)

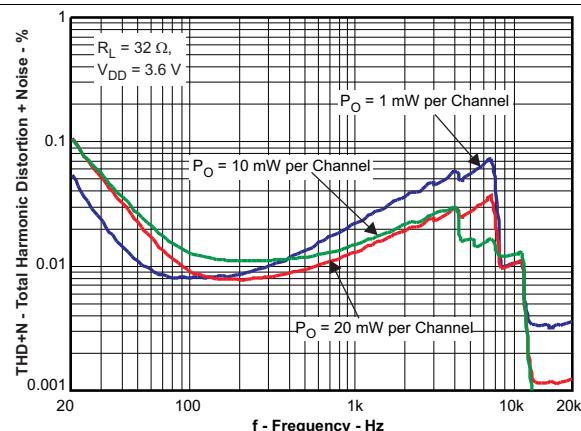


Figure 7. Total Harmonic Distortion + Noise vs Frequency

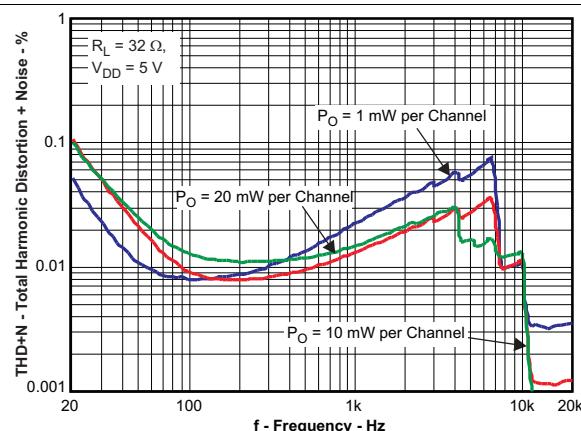


Figure 8. Total Harmonic Distortion + Noise vs Frequency

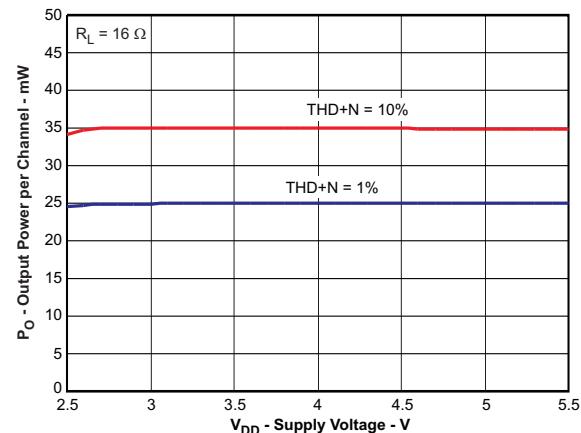


Figure 9. Output Power vs Supply Voltage

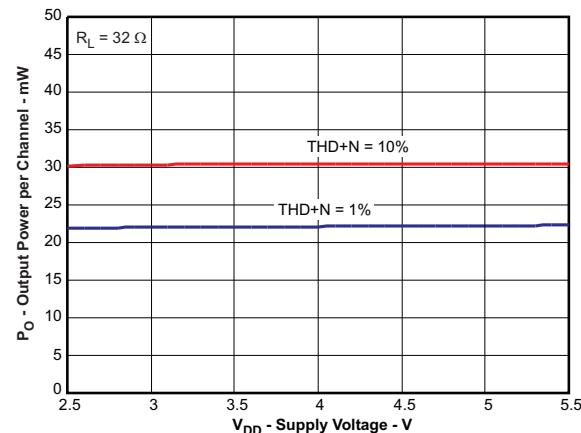


Figure 10. Output Power vs Supply Voltage

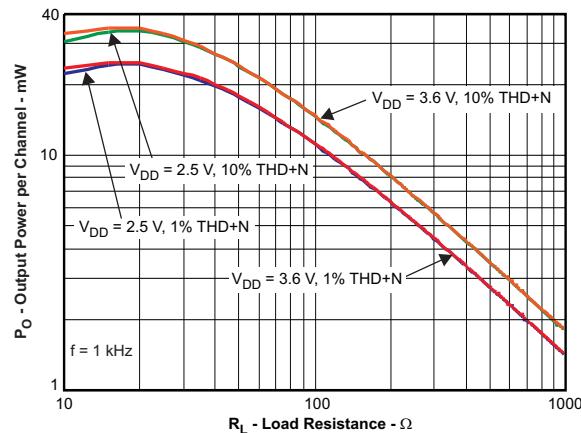


Figure 11. Output Power vs Load Resistance

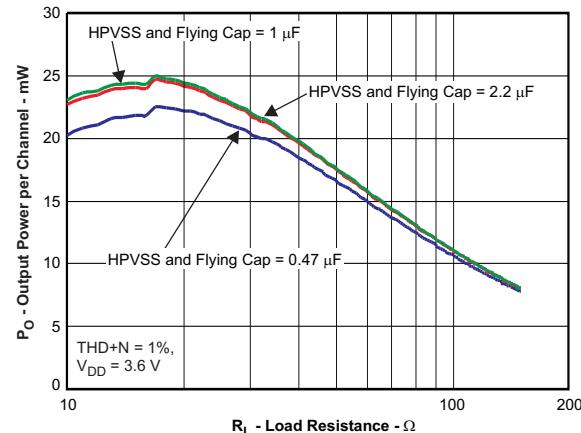
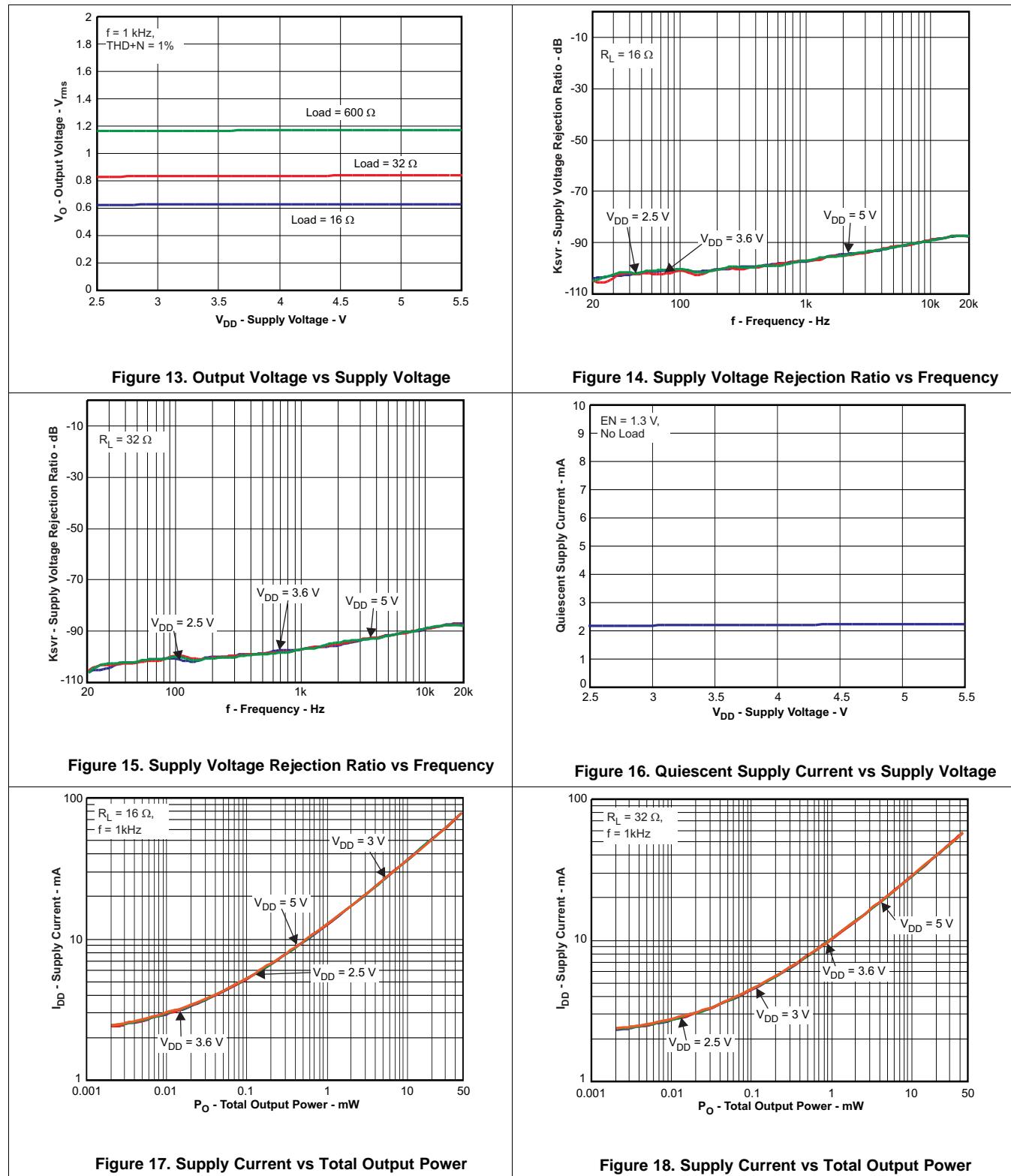
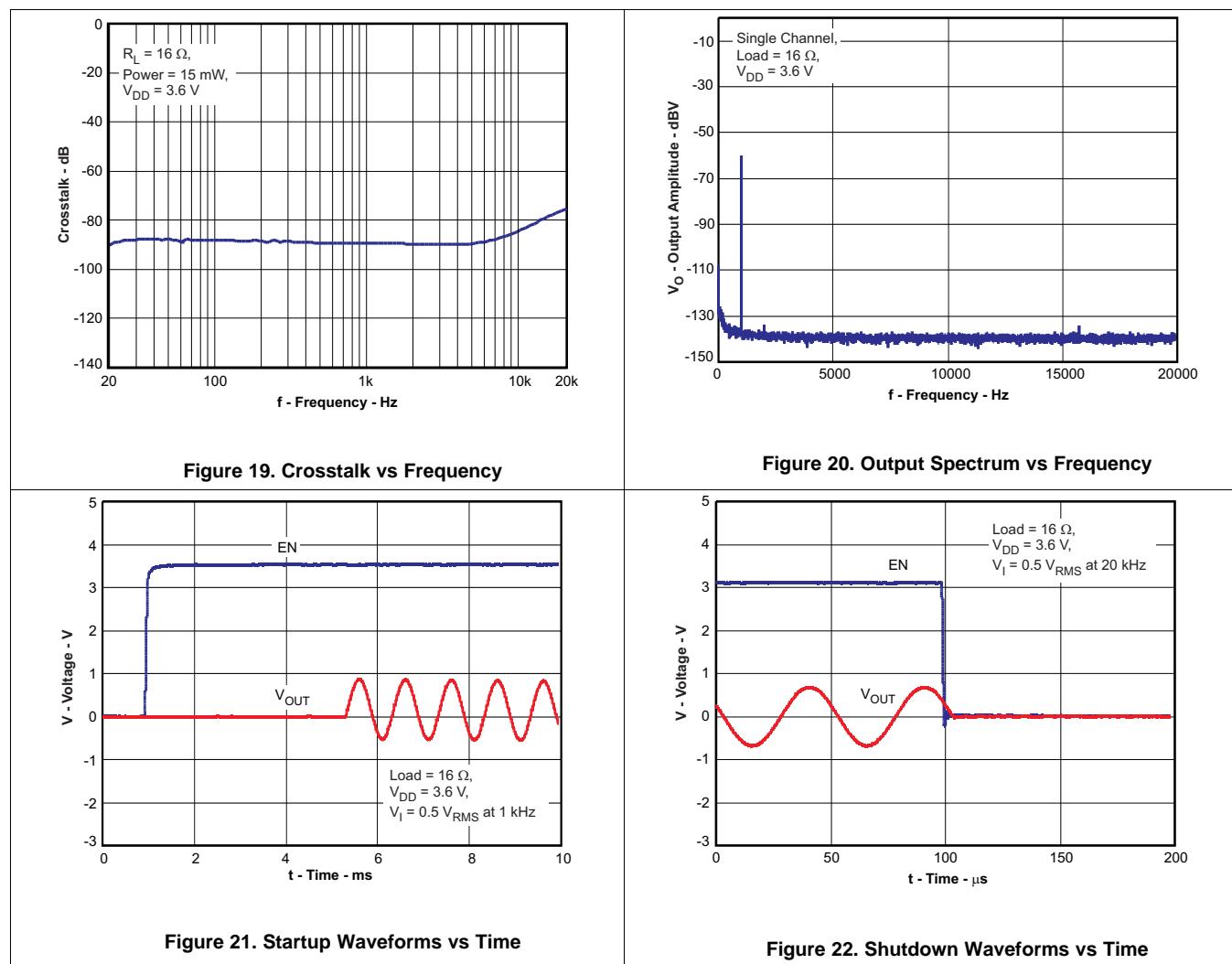


Figure 12. Output Power vs Load Resistance

**Typical Characteristics (continued)**

**Figure 13. Output Voltage vs Supply Voltage**
**Figure 14. Supply Voltage Rejection Ratio vs Frequency**
**Figure 15. Supply Voltage Rejection Ratio vs Frequency**
**Figure 16. Quiescent Supply Current vs Supply Voltage**
**Figure 17. Supply Current vs Total Output Power**
**Figure 18. Supply Current vs Total Output Power**

## Typical Characteristics (continued)



## 7 Detailed Description

### 7.1 Overview

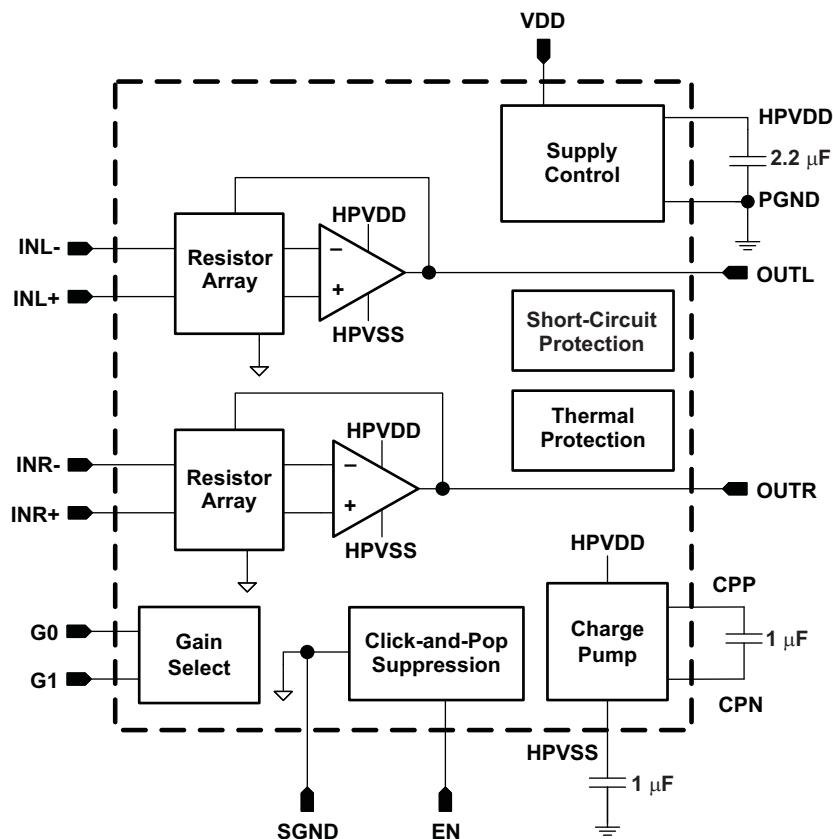
The TPA6132A2 is a DirectPath™ stereo headphone amplifier that requires no output DC blocking capacitors and is capable of delivering 25m-W/Ch into 16- $\Omega$  speakers. The device has built-in pop suppression circuitry to completely eliminate pop noise during turn-on and turn-off. The amplifier outputs have short-circuit and thermal-overload protection.

The TPA6132A2 features fully differential inputs to reduce system noise pickup between the audio source and the headphone amplifier. The high power supply noise rejection performance and differential architecture provides increased RF noise immunity.

Differential stereo inputs and built-in resistors set the device gain, reducing external component count. The TPA6132A2 has four gain settings which are controlled with pins G0 and G1. The combination of these pins set the device to -6-dB, 0-dB, 3-dB or 6-dB gain.

The TPA6132A2 operates from a single 2.3-V to 5.5-V supply with 2.1 mA of typical supply current, as it uses a built-in charge pump to generate a negative voltage supply for the headphone amplifiers. Shutdown mode reduces supply current to less than 1  $\mu$ A

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Headphone Amplifiers

Single-supply headphone amplifiers typically require dc-blocking capacitors to remove dc bias from their output voltage. The top drawing in [Figure 23](#) illustrates this connection. If dc bias is not removed, large dc current will flow through the headphones which wastes power, clip the output signal, and potentially damage the headphones.

These dc-blocking capacitors are often large in value and size. Headphone speakers have a typical resistance between  $16\ \Omega$  and  $32\ \Omega$ . This combination creates a high-pass filter with a cutoff frequency as shown in [Equation 1](#), where  $R_L$  is the load impedance,  $C_O$  is the dc-block capacitor, and  $f_C$  is the cutoff frequency.

$$f_C = \frac{1}{2\pi R_L C_O} \quad (1)$$

For a given high-pass cutoff frequency and load impedance, the required dc-blocking capacitor is found as:

$$C_O = \frac{1}{2\pi f_C R_L} \quad (2)$$

Reducing  $f_C$  improves low frequency fidelity and requires a larger dc-blocking capacitor. To achieve a 20 Hz cutoff with  $16\ \Omega$  headphones,  $C_O$  must be at least  $500\ \mu\text{F}$ . Large capacitor values require large packages, consuming PCB area, increasing height, and increasing cost of assembly. During start-up or shutdown the dc-blocking capacitor has to be charged or discharged. This causes an audible pop on start-up and power-down. Large dc-blocking capacitors also reduce audio output signal fidelity.

Two different headphone amplifier architectures are available to eliminate the need for dc-blocking capacitors. The Capless amplifier architecture is similar provides a reference voltage to the headphone connector shield pin as shown in the middle drawing of [Figure 23](#). The audio output signals are centered around this reference voltage, which is typically half of the supply voltage to allow symmetrical output voltage swing.

When using a Capless amplifier do not connect the headphone jack shield to any ground reference or large currents will result. This makes Capless amplifiers ineffective for plugging non-headphone accessories into the headphone connector. Capless amplifiers are useful only with floating GND headphones.

## Feature Description (continued)

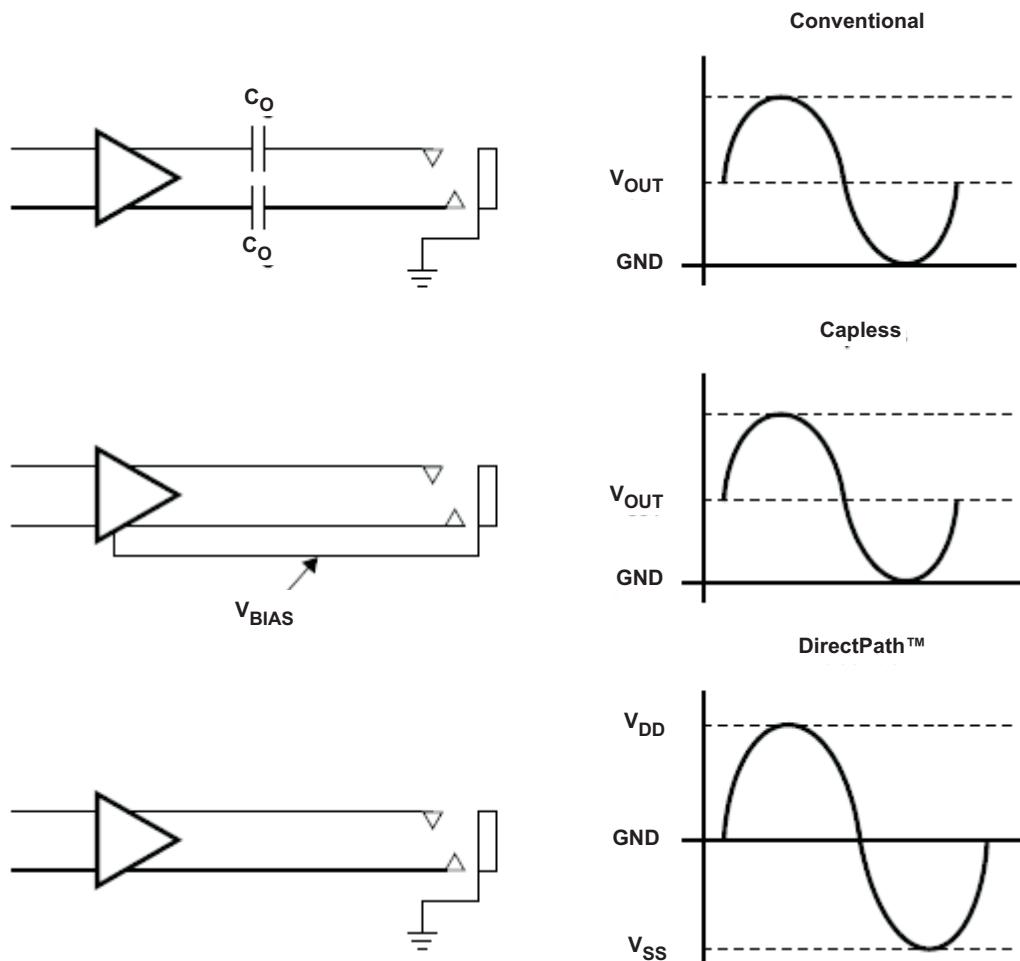


Figure 23. Amplifier Applications

The DirectPath™ amplifier architecture operates from a single supply voltage and uses an internal charge pump to generate a negative supply rail for the headphone amplifier. The output voltages are centered around 0 V and are capable of positive and negative voltage swings as shown in the bottom drawing of Figure 23. DirectPath amplifiers require no output dc-blocking capacitors. The headphone connector shield pin connects to ground and will interface with headphones and non-headphone accessories. The TPA6132A2 is a DirectPath amplifier.

### 7.3.2 Eliminating Turn-on Pop and Power Supply Sequencing

The TPA6132A2 has excellent noise and turn-on / turn-off pop performance. It uses an integrated click-and-pop suppression circuit to allow fast start-up and shutdown without generating any voltage transients at the output pins. Typical start-up time from shutdown is 5 ms.

DirectPath technology keeps the output dc voltage at 0 V even when the amplifier is powered up. The DirectPath technology together with the active pop-and-click suppression circuit eliminates audible transients during start up and shutdown.

Use input coupling capacitors to ensure inaudible turn-on pop. Activate the TPA6132A2 after all audio sources have been activated and their output voltages have settled. On power-down, deactivate the TPA6132A2 before deactivating the audio input source. The EN pin controls device shutdown: Set to 0.6 V or lower to deactivate the TPA6132A2; set to 1.3 V or higher to activate.

## Feature Description (continued)

### 7.3.3 RF and Power Supply Noise Immunity

The TPA6132A2 employs a new differential amplifier architecture to achieve high power supply noise rejection and RF noise rejection. RF and power supply noise are common in modern electronics. Although RF frequencies are much higher than the 20 kHz audio band, signal modulation often falls in-band. This, in turn, modulates the supply voltage, allowing a coupling path into the audio amplifier. A common example is the 217 Hz GSM frame-rate buzz often heard from an active speaker when a cell phone is placed nearby during a phone call.

The TPA6132A2 has excellent rejection of power supply and RF noise, preventing audio signal degradation.

### 7.3.4 Constant Maximum Output Power and Acoustic Shock Prevention

Typically the output power increases with increasing supply voltage on an unregulated headphone amplifier. The TPA6132A2 maintains a constant output power independent of the supply voltage. Thus the design for prevention of acoustic shock (hearing damage due to exposure to a loud sound) is simplified since the output power will remain constant, independent of the supply voltage. This feature allows maximizing the audio signal at the lowest supply voltage.

## 7.4 Device Functional Modes

### 7.4.1 Gain Control

The TPA6132A2 has four gain settings which are controlled with pins G0 and G1. [Table 1](#) gives an overview of the gain function.

G0 VOLTAGE	G1 VOLTAGE	AMPLIFIER GAIN
≤ 0.5 V	≤ 0.5 V	-6 dB
≥ 1.3 V	≤ 0.5 V	0 dB
≤ 0.5 V	≥ 1.3 V	3 dB
≥ 1.3 V	≥ 1.3 V	6 dB

**Table 1. Windows Vista™ Premium Mobile Mode Specifications**

Device Type	Requirement	Windows Premium Mobile Vista Specifications	TPA6132A2 Typical Performance
Analog Speaker Line Jack ( $R_L = 10 \text{ k}\Omega$ , FS = 0.707 Vrms)	THD+N	≤ -65 dB FS [20 Hz, 20 kHz]	-75 dB FS [20 Hz, 20 kHz]
	Dynamic Range with Signal Present	≤ -80 dB FS A-Weight	-100 dB FS A-Weight
	Line Output Crosstalk	≤ -60 dB [20 Hz, 20 kHz]	-90 dB [20 Hz, 20 kHz]
Analog Headphone Out Jack ( $R_L = 32\Omega$ , FS = 0.300 Vrms)	THD+N	≤ -45 dB FS [20 Hz, 20 kHz]	-65 dB FS [20 Hz, 20 kHz]
	Dynamic Range with Signal Present	≤ -80 dB FS A-Weight	-94 dB FS A-Weight
	Headphone Output Crosstalk	≤ -60 dB [20 Hz, 20 kHz]	-90 dB [20 Hz, 20 kHz]

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPA6132A2 starts its operation by asserting the EN pin to logic 1. The device enters in shutdown mode when pulling low EN pin. The charge pump generates a negative supply voltage. The charge pump flying capacitor connected between CPP and CPN transfers charge to generate the negative supply voltage. The output voltages are capable of positive and negative voltage swings and are centered close to 0 V, eliminating the need for output capacitors. Input coupling capacitors block any dc bias from the audio source and ensure maximum dynamic range. The device has built-in pop suppression circuitry to completely eliminate pop noise during turn-on, turn-off and enter or exit shutdown mode.

### 8.2 Typical Applications

#### 8.2.1 Configuration with Differential Input Signals

Figure 24 shows a typical application circuit for the TPA6132A2 with a stereo headphone jack output and differential input signals. Also supports charge pump flying capacitor and power supply decoupling capacitors.

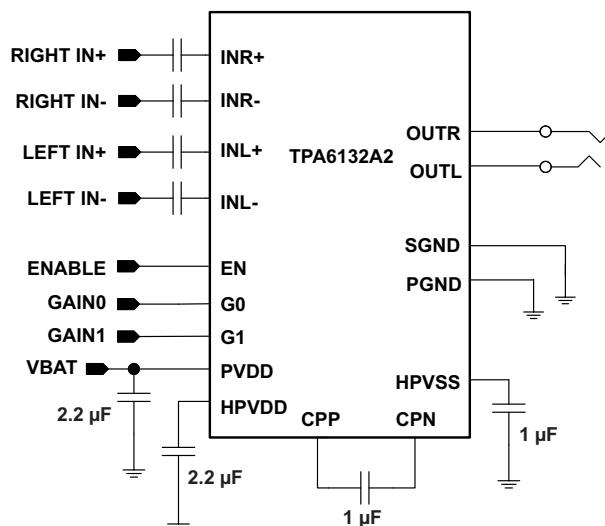


Figure 24. Typical Application Configuration with Differential Input Signals

##### 8.2.1.1 Design Requirements

For this design example, use the parameters shown in Table 2.

Table 2. Design Parameters

PARAMETERS	VALUES
Input voltage range	2.2 V to 5.3 V
Output voltage	$1.1 \cdot V_{RMS}$
Current	2 mA to 3.2 mA

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 Input Coupling Capacitors

Input coupling capacitors block any dc bias from the audio source and ensure maximum dynamic range. Input coupling capacitors also minimize TPA6132A2 turn-on pop to an inaudible level.

The input capacitors are in series with TPA6132A2 internal input resistors, creating a high-pass filter. [Equation 3](#) calculates the high-pass filter corner frequency. The input impedance,  $R_{IN}$ , is dependent on device gain. Larger input capacitors decrease the corner frequency. See the Operating Characteristics table for input impedance values.

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}} \quad (3)$$

For a given high-pass cutoff frequency, the minimum input coupling capacitor is found as:

$$C_{IN} = \frac{1}{2\pi f_C R_{IN}} \quad (4)$$

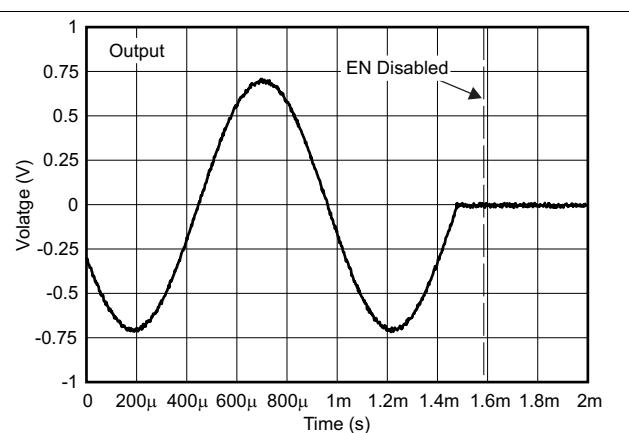
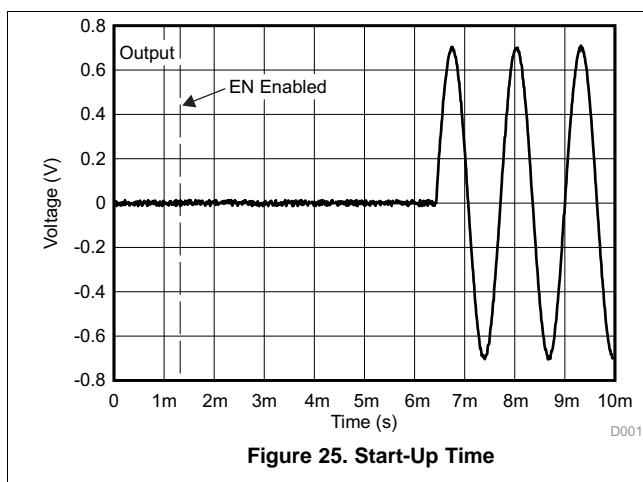
Example: Design for a 20 Hz corner frequency with a TPA6132A2 gain of +6 dB. The Operating Characteristics table gives  $R_{IN}$  as 13.2 kΩ. [Equation 4](#) shows the input coupling capacitors must be at least 0.6 μF to achieve a 20 Hz high-pass corner frequency. Choose a 0.68 μF standard value capacitor for each TPA6132A2 input (X5R material or better is required for best performance).

Input capacitors can be removed provided the TPA6132A2 inputs are driven differentially with less than ±1 V and the common-mode voltage is within the input common-mode range of the amplifier. Without input capacitors turn-on pop performance may be degraded and should be evaluated in the system.

#### 8.2.1.2.2 Charge Pump Flying Capacitor and HPVSS Capacitor

The TPA6132A2 uses a built-in charge pump to generate a negative voltage supply for the headphone amplifiers. The charge pump flying capacitor connects between CPP and CPN. It transfers charge to generate the negative supply voltage. The HPVSS capacitor must be at least equal in value to the flying capacitor to allow maximum charge transfer. Use low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance) to maximize charge pump efficiency. Typical values are 1 μF to 2.2 μF for the HPVSS and flying capacitors. Although values down to 0.47 μF can be used, total harmonic distortion (THD) will increase.

#### 8.2.1.3 Application Curves



## 8.2.2 Configuration with Single-Ended Input Signals

Figure 27 shows a typical application circuit for the TPA6132A2 with a stereo headphone jack output and single-ended input signals. Also supports charge pump flying capacitor and power supply decoupling capacitors.

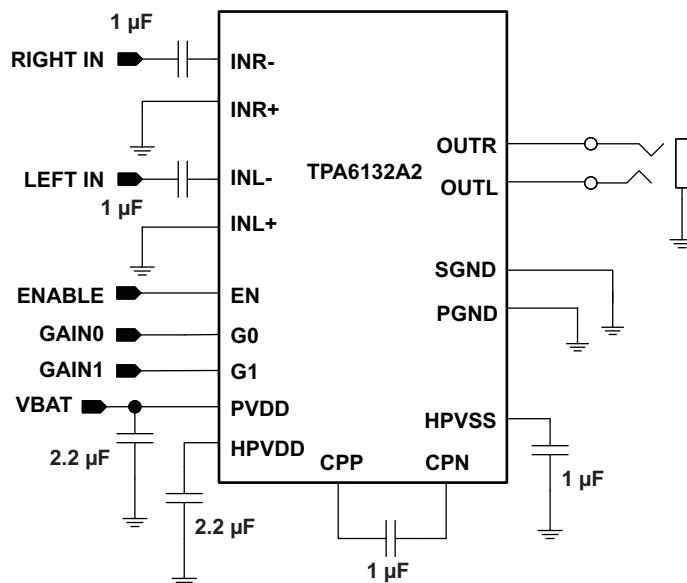


Figure 27. Typical Application Configuration with Single-Ended Input Signals

### 8.2.2.1 Design Requirements

Refer to the [Configuration with Differential Input Signals](#) design requirements

### 8.2.2.2 Detailed Design Procedure

Refer to the [Configuration with Differential Input Signals](#) detailed design procedures.

### 8.2.2.3 Application Curves

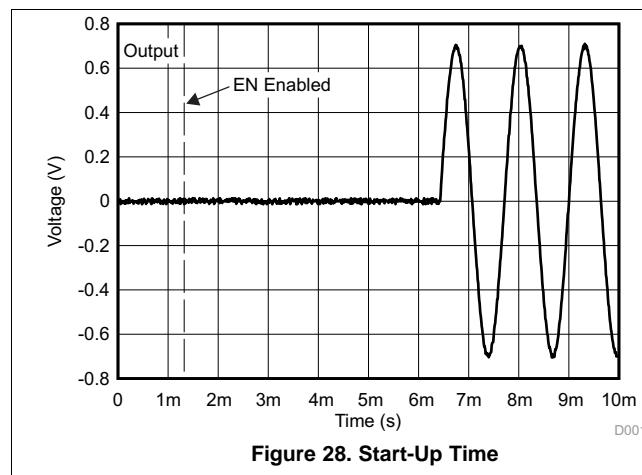


Figure 28. Start-Up Time

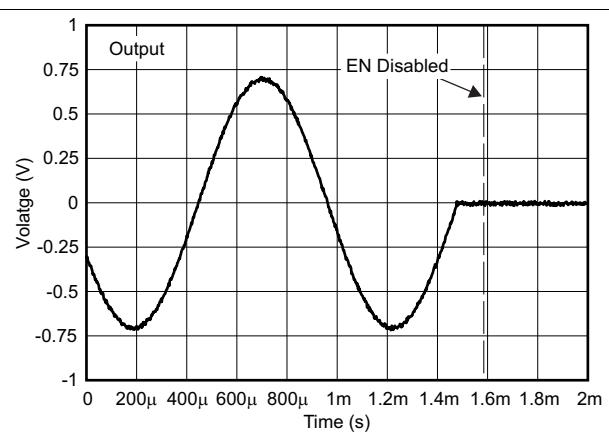


Figure 29. Shutdown

## 9 Power Supply Recommendations

Connect the supply voltage to the VDD pin and decouple it with an X5R or better capacitor. Connect the HPVDD pin only to a 2.2  $\mu$ F, X5R or better, capacitor. Do not connect HPVDD to an external voltage supply. Place both capacitors within 5 mm of their associated pins on the TPA6132A2. Ensure that the ground connection of each of the capacitors has a minimum length return path to the device. Failure to properly decouple the TPA6132A2 may degrade audio or EMC performance.

### 9.1 Power Supply and HPVDD Decoupling Capacitors

The TPA6132A2 DirectPath headphone amplifier requires adequate power supply decoupling to ensure that output noise and total harmonic distortion (THD) remain low. Use good low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance). Place a 2.2  $\mu$ F capacitor within 5 mm of the VDD pin. Reducing the distance between the decoupling capacitor and VDD minimizes parasitic inductance and resistance, improving TPA6132A2 supply rejection performance. Use 0402 or smaller size capacitors if possible.

For additional supply rejection, connect an additional 10  $\mu$ F or higher value capacitor between VDD and ground. This will help filter lower frequency power supply noise. The high power supply rejection ratio (PSRR) of the TPA6132A2 makes the 10  $\mu$ F capacitor unnecessary in most applications.

Connect a 2.2  $\mu$ F capacitor between HPVDD and ground. This ensures the amplifier internal bias supply remains stable and maximizes headphone amplifier performance.

**WARNING**

**DO NOT connect HPVDD directly to VDD or an external supply voltage. The voltage at HPVDD is generated internally. Connecting HPVDD to an external voltage can damage the device.**

## 10 Layout

### 10.1 Layout Guidelines

- Solder the exposed metal pad on the TPA6132A2RTE QFN package to the landing pad on the PCB.
- Connect the landing pad to ground or leave it electrically unconnected (floating). *Do not connect the landing pad to VDD or to any other power supply voltage.*
- If the pad is grounded, it must be connected to the same ground as the PGND pin (10).
- See the layout and mechanical drawings at the end of the data sheet for proper sizing.
- Soldering the thermal pad is required for mechanical reliability and enhances thermal conductivity of the package.

#### WARNING

**DO NOT connect the TPA6132A2RTE exposed metal pad to VDD or any other power supply voltage.**

### 10.2 Layout Example

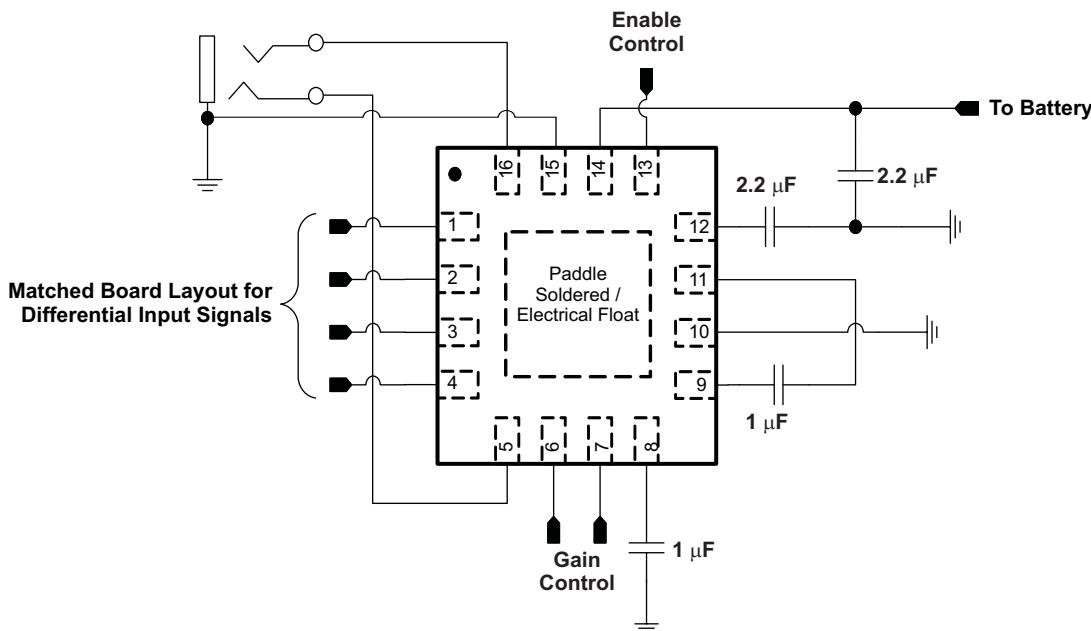


Figure 30. Board Layout Concept

### 10.3 GND Connections

The SGND pin is an input reference and must be connected to the headphone ground connector pin. This ensures no turn-on pop and minimizes output offset voltage. Do not connect more than  $\pm 0.3$  V to SGND.

PGND is a power ground. Connect supply decoupling capacitors for VDD, HPVDD, and HPVSS to PGND.

## 11 器件和文档支持

### 11.1 接收文档更新通知

要接收文档更新通知, 请导航至德州仪器 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。请单击右上角的通知我 进行注册, 即可收到任意产品信息更改每周摘要。有关更改的详细信息, 请查看任意已修订文档中包含的修订历史记录。

### 11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范, 并且不一定反映 TI 的观点; 请参阅 TI 的 [《使用条款》](#)。

**TI E2E™ 在线社区** **TI 的工程师对工程师 (E2E) 社区**。此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](http://e2e.ti.com) 中, 您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** **TI 参考设计支持** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 11.3 商标

DirectPath, E2E are trademarks of Texas Instruments.

Windows Vista is a trademark of Microsoft Corporation.

All other trademarks are the property of their respective owners.

### 11.4 静电放电警告

 这些装置包含有限的内置 ESD 保护。 存储或装卸时, 应将导线一起截短或将装置放置于导电泡棉中, 以防止 MOS 门极遭受静电损伤。

### 11.5 Glossary

[SLYZ022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时, 我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本, 请参阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPA6132A2RTER</a>	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AIWI
TPA6132A2RTER.A	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AIWI
TPA6132A2RTER.B	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AIWI
TPA6132A2RTERG4	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AIWI
TPA6132A2RTERG4.A	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AIWI
TPA6132A2RTERG4.B	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AIWI
<a href="#">TPA6132A2RTET</a>	Active	Production	WQFN (RTE)   16	250   SMALL T&R	Yes	NIPDAU   NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AIWI
TPA6132A2RTET.A	Active	Production	WQFN (RTE)   16	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AIWI
TPA6132A2RTET.B	Active	Production	WQFN (RTE)   16	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AIWI

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

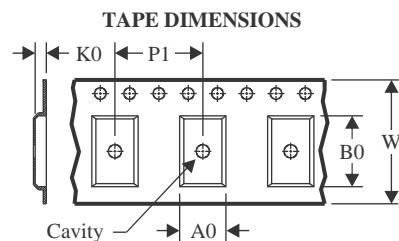
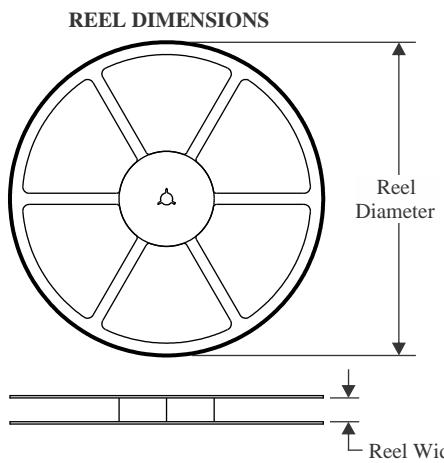
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

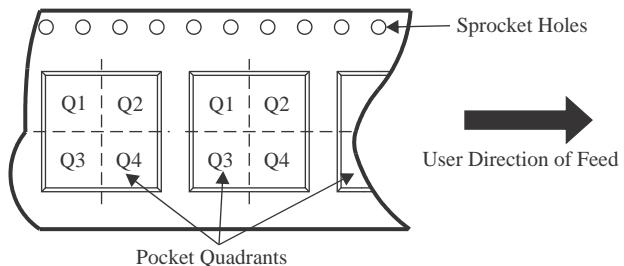
---

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

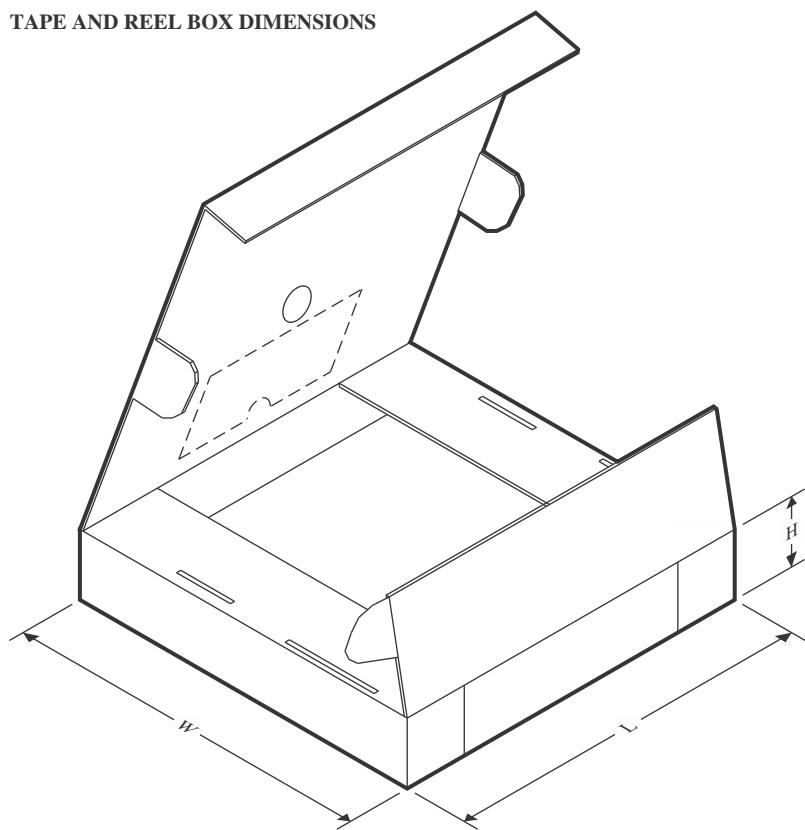
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6132A2RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA6132A2RTERG4	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA6132A2RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6132A2RTER	WQFN	RTE	16	3000	346.0	346.0	33.0
TPA6132A2RTERG4	WQFN	RTE	16	3000	346.0	346.0	33.0
TPA6132A2RTET	WQFN	RTE	16	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

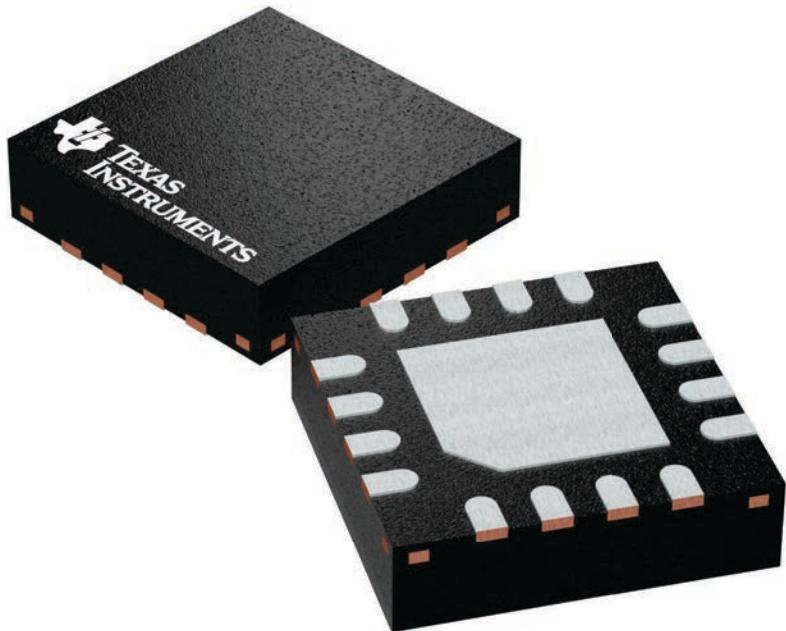
### RTE 16

### WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

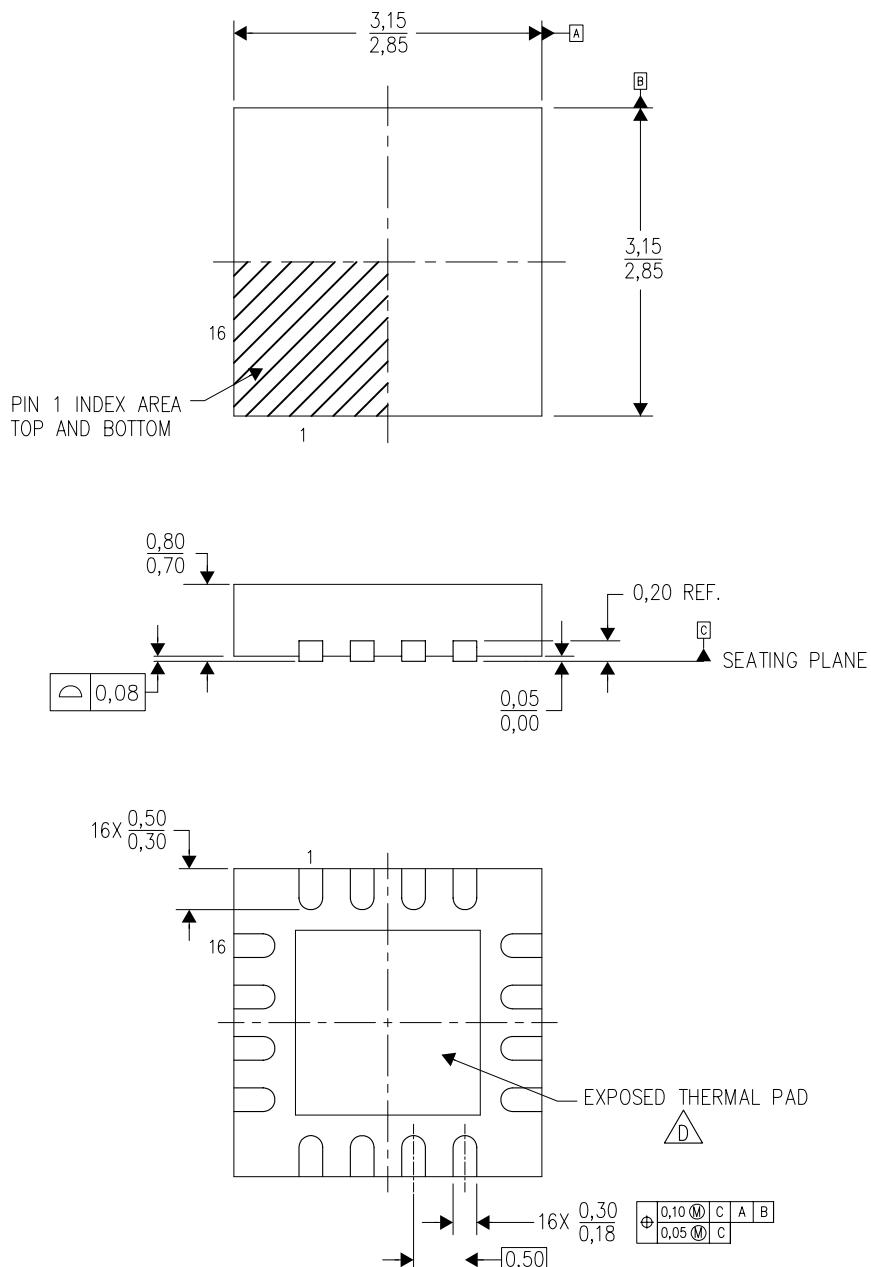
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225944/A

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4205254/D 01/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
 B. This drawing is subject to change without notice.

C. Quad Flatpack, No-leads (QFN) package configuration.

 The package thermal pad must be soldered to the board for thermal and mechanical performance.  
 See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

E. Falls within JEDEC MO-220.

## THERMAL PAD MECHANICAL DATA

RTE (S-PWQFN-N16)

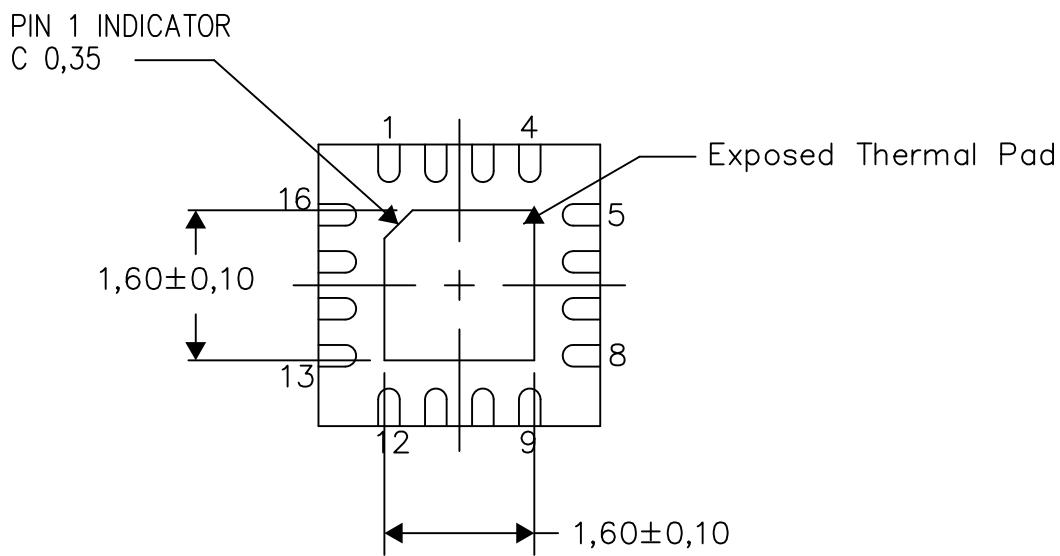
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206446-2/U 08/15

NOTE: A. All linear dimensions are in millimeters

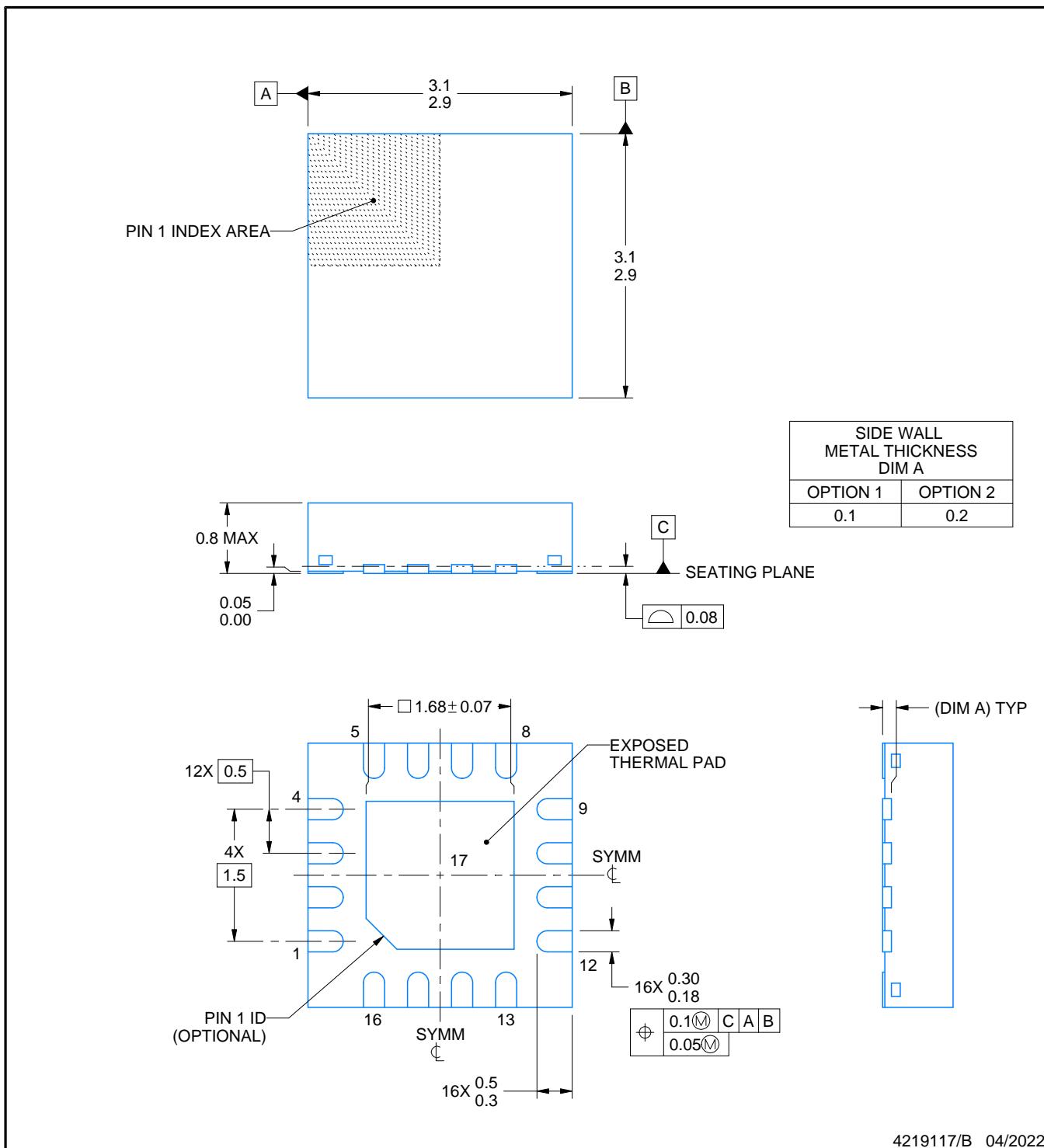
# PACKAGE OUTLINE

RTE0016C



WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## NOTES:

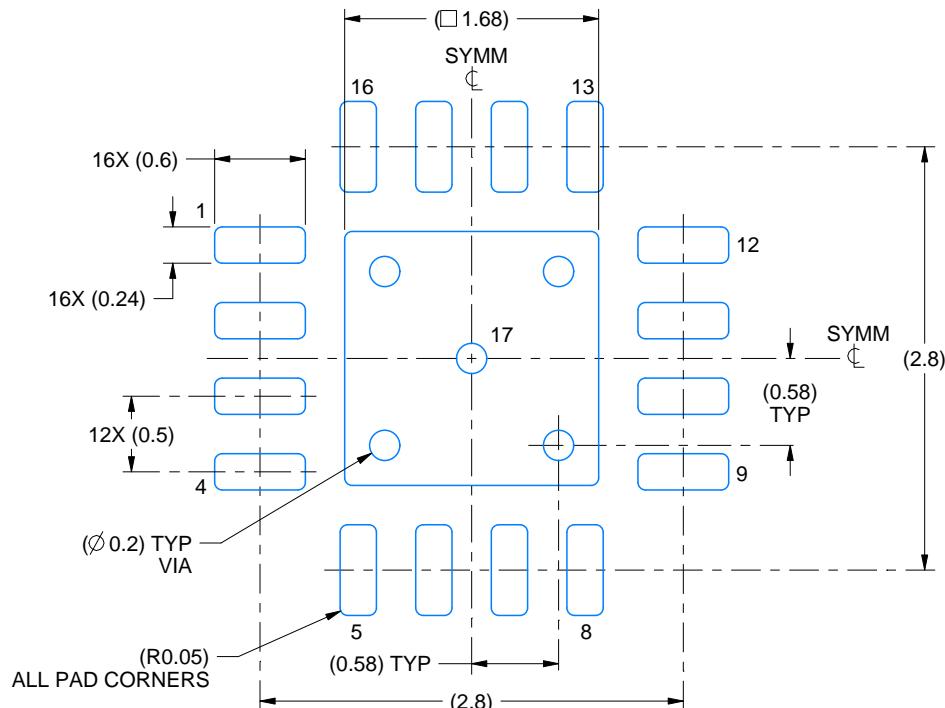
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

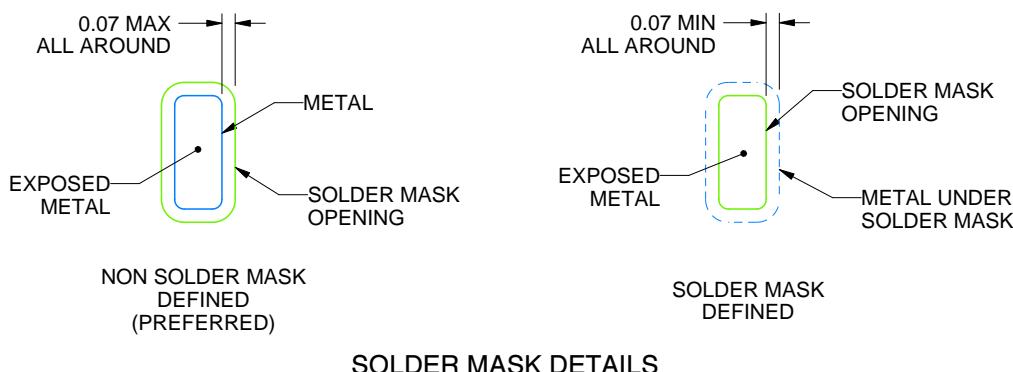
**RTE0016C**

## **WQFN - 0.8 mm max height**

## PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



4219117/B 04/2022

#### NOTES: (continued)

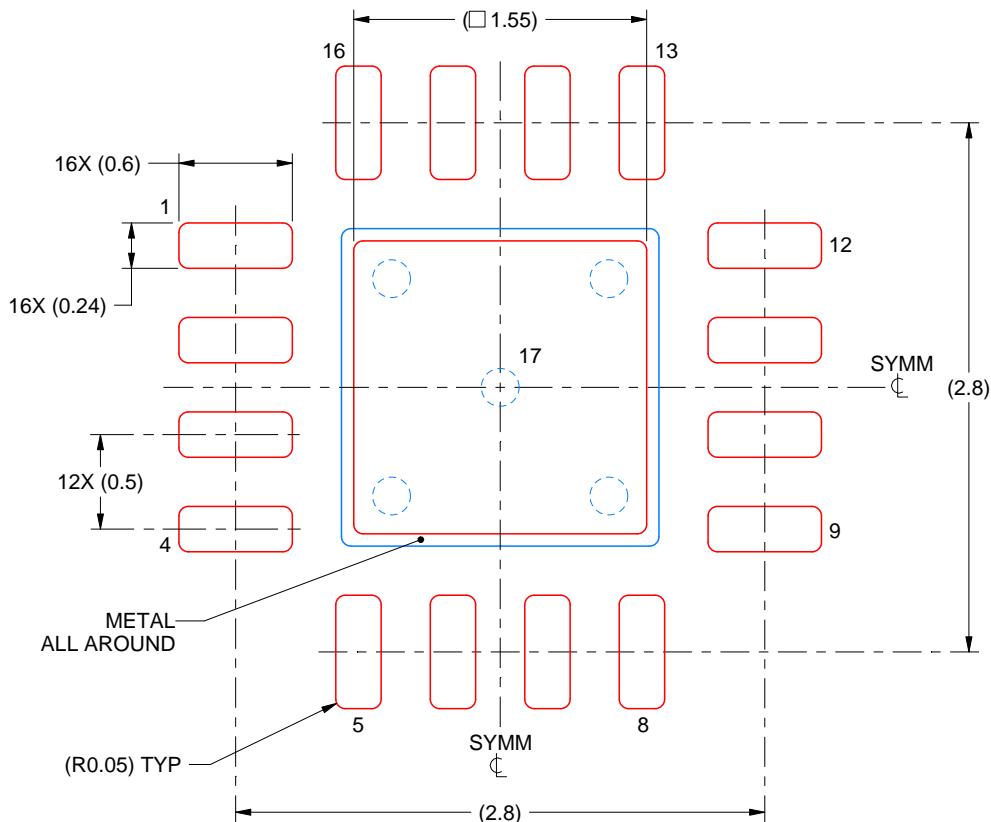
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

版权所有 © 2025, 德州仪器 (TI) 公司