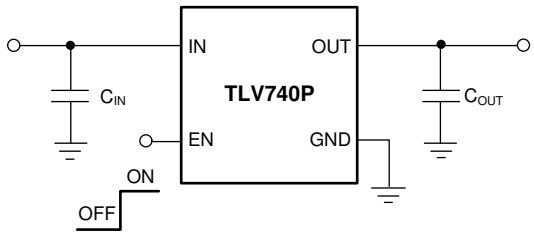
具有折返电流限制的 TLV740P 300mA 低压降稳压器

1 特性

- 折返过流保护
- 封装：
  - 1mm × 1mm 4 引脚 X2SON
  - 5 引脚 SOT-23 封装
- 超低压降：300mA 时为 460mV
- 精度：1%
- 低 I_Q：50μA
- 输入电压范围：1.4V 至 5.5V
- 可提供固定输出电压：
  1V 至 3.3V
- 高 PSRR：1kHz 时为 65dB
- 有源输出放电

2 应用

- 便携式媒体播放器
- 普通笔记本电脑
- 流媒体播放器
- 家用打印机
- STB 和 DVR



典型应用电路

3 说明

TLV740P 低压降 (LDO) 线性稳压器是一款低静态电流 LDO，具有出色的线路和负载瞬态性能，专为对功耗敏感的应用设计。此器件可提供 1% 的典型精度。

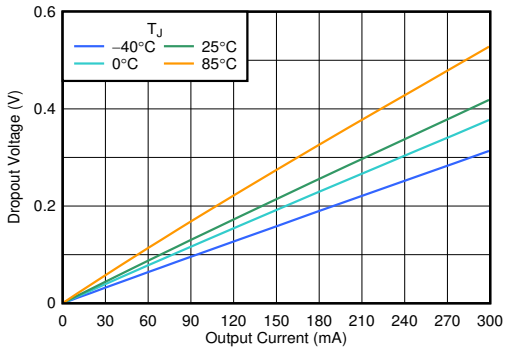
TLV740P 还可在器件上电和使能期间提供浪涌电流控制。TLV740P 将输入电流限制为定义的电流限值，从而防止从输入电源流出的电流过大。此功能对于电池供电类器件尤为重要。

TLV740P 采用标准的 DQN 和 DBV 封装。TLV740P 还提供了有源下拉电路，用于对输出负载进行快速放电。

器件信息(1)

器件名称	封装	封装尺寸
TLV740P	SOT-23 (5)	2.90mm × 1.60mm
	X2SON (4)	1.00mm × 1.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



压降电压与输出电流间的关系 (3.3V V_{OUT})

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (June 2020) to Revision A (December 2020)	Page
• 将 DQN 封装状态从预发布更改为量产数据	1

5 Pin Configuration and Functions

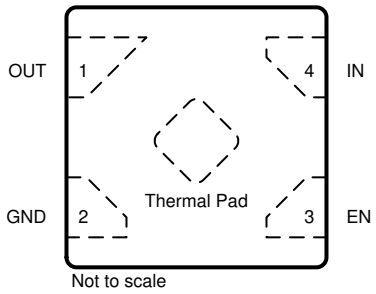


图 5-1. DQN Package, 4-Pin X2SON, Top View

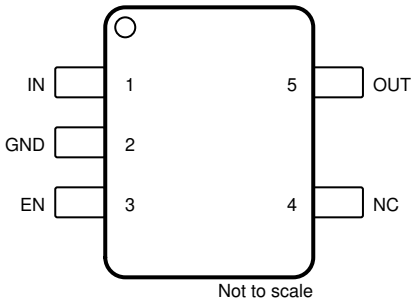


图 5-2. DBV Package, 5-Pin SOT-23, Top View

表 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	X2SON	SOT-23		
EN	3	3	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. Do not float this pin. If not used, connect EN to IN.
GND	2	2	—	Ground pin. This pin must be connected to ground on the board.
IN	4	1	I	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground; see the *Recommended Operating Conditions* table. Place the input capacitor as close to the input of the device as possible.
NC	—	4	—	No connect pin. This pin is not internally connected. Connect to ground for best thermal performance or leave floating.
OUT	1	5	O	Regulated output pin. A 1-µF or greater effective capacitance is required from OUT to ground for stability. see the *Recommended Operating Conditions* table. For best transient response, use a 1-µF or larger ceramic capacitor from OUT to ground. Place the output capacitor as close to output of the device as possible.
Thermal pad		—	—	The thermal pad is electrically connected to the GND pin. Connect the thermal pad to a large-area GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6.0	V
	V_{EN}	–0.3	VIN(2)	
	V_{OUT}	–0.3	V_{IN} + 0.3 or 3.6(3)	
Temperature	Operating junction, T_J	–55	125	°C
	Storage, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum is V_{IN} or smaller.
(3) Maximum is V_{IN} + 0.3 V or 3.6 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.4		5.5	V
V_{OUT}	Output voltage	0		V_{IN} + 0.3	V
V_{EN}	Enable voltage	0		V_{IN} (1)	V
I_{OUT}	Output current	0		300	mA
C_{IN}	Input capacitor	1			µF
C_{OUT}	Output capacitor(2)	1		100	µF
f_{EN}	Enable toggle frequency			10	kHz
T_J	Junction temperature	–40		85	°C

(1) V_{EN} is V_{IN} or smaller.
(2) Effective output capacitance of 0.5 µF minimum required for stability.

6.4 Thermal Information

THERMAL METRIC(1)		TLV740P		UNIT
		DQN (X2SON)	DBV (SOT-23-5)	
		4 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	224.3	216	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	161.5	123.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	164.6	88.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.9	62.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	164.0	87.8	°C/W

THERMAL METRIC[1]		TLV740P		UNIT
		DQN (X2SON)	DBV (SOT-23-5)	
		4 PINS	5 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	154.8	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at operating temperature range (T_J = +25°C), V_{IN} = $V_{OUT(NOM)}$ + 2.1 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 μF, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Output accuracy	1 V ≤ V_{OUT} ≤ 3.3 V		–1		1	%
	Maximum output current[1]					300	mA
	Output voltage temperature coefficient	I_{OUT} = 0.1 mA, –40°C ≤ T_J ≤ +85°C			0.0017		%/℃
	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V			1	5	mV
	Load regulation	1 mA ≤ I_{OUT} ≤ 300 mA			10	30	mV
V_{DO}	Dropout voltage	V_{OUT} = 0.95 x $V_{OUT(nom)}$	1 V ≤ V_{OUT} < 1.8 V, I_{OUT} = 300 mA		1200	1300	mV
		V_{OUT} = 0.95 x $V_{OUT(nom)}$	1.8 V ≤ V_{OUT} < 2.1 V, I_{OUT} = 300 mA		700	800	
		V_{OUT} = 0.95 x $V_{OUT(nom)}$	2.1 V ≤ V_{OUT} ≤ 3.3 V, I_{OUT} = 300 mA		460	500	
I_{GND}	Ground current	I_{OUT} = 0 mA			50	80	μA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4 V, 3.1 V ≤ V_{IN} ≤ 5.5 V, –40°C ≤ T_J ≤ +85°C			0.1	1	μA
PSRR	Power-supply rejection ratio	V_{IN} = 5.4 V, V_{OUT} = 3.3 V, I_{OUT} = 150 mA	f = 100 Hz		67		dB
			f = 10 kHz		45		
			f = 1 MHz		32		
Vn	Output noise voltage	BW = 100 Hz to 100 kHz, V_{OUT} = 1.0 V, I_{OUT} = 1 mA			65		$μV_{RMS}$
t_{STR}	Startup time[2]	C_{OUT} = 1 μF, I_{OUT} = 300 mA			100		μs
V_{HI}	EN pin high voltage (enabled)	–40°C ≤ T_J ≤ +85°C		1.0		V_{IN}	V
V_{LO}	EN pin low voltage (disabled)			0		0.4	V
I_{EN}	Enable pin current	EN = 5.5 V, –40°C ≤ T_J ≤ +85°C			10		nA
$R_{PULLDOWN}$	Pulldown resistance	V_{IN} = 5.5 V, V_{EN} = 0 V			120		Ω
I_{CL}	Output current limit			360			mA
I_{SC}	Short circuit current limit	V_{OUT} = 0 V			40		mA
$T_{SD(shutdown)}$	Thermal shutdown temperature	Shutdown, temperature increasing			158		°C
$T_{SD(reset)}$	Thermal shutdown reset temperature	Reset, temperature decreasing			140		

(1) Maximum output current is affected by the PCB layout, metal trace width, number of layers, ambient temperatrue and other environmental factors. Thermal limitations of the system must be carefully considered.

(2) Startup time = time from EN assertion to 0.95 × $V_{OUT(NOM)}$.

6.6 Typical Characteristics

over operating temperature range (T_J = –40°C to 85°C), V_{IN} = $V_{OUT(nom)}$ + 2.1 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C

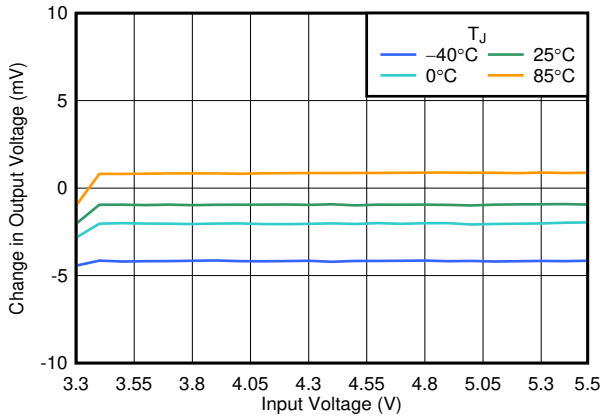


图 6-1. Line Regulation vs V_{IN}

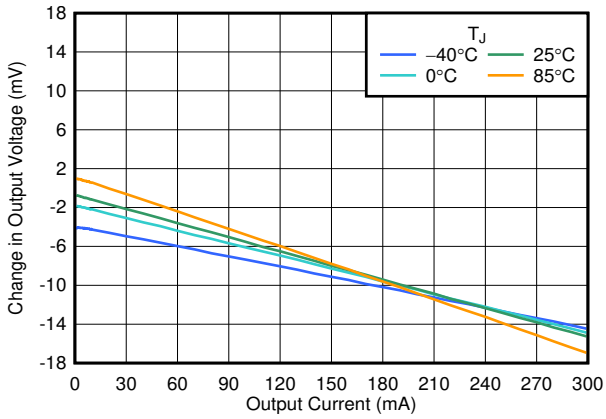
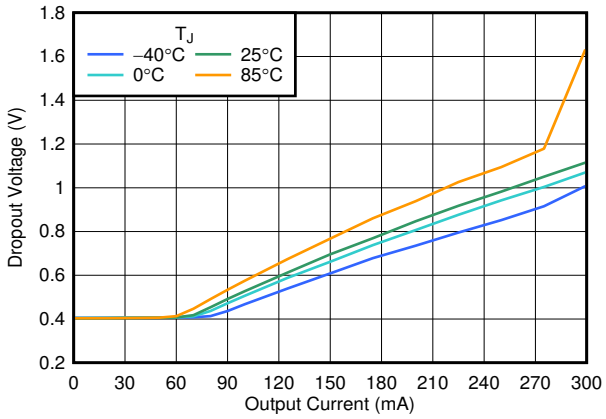
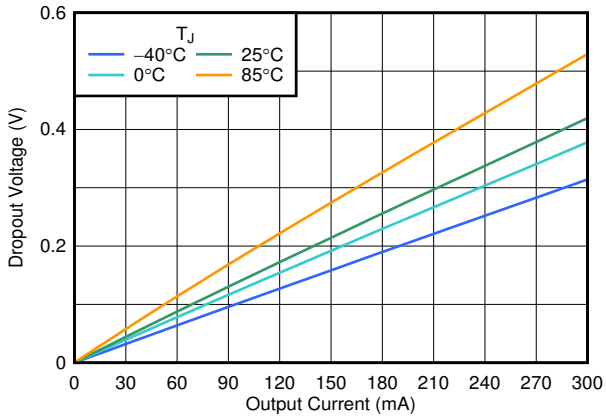


图 6-2. Load Regulation vs I_{OUT}



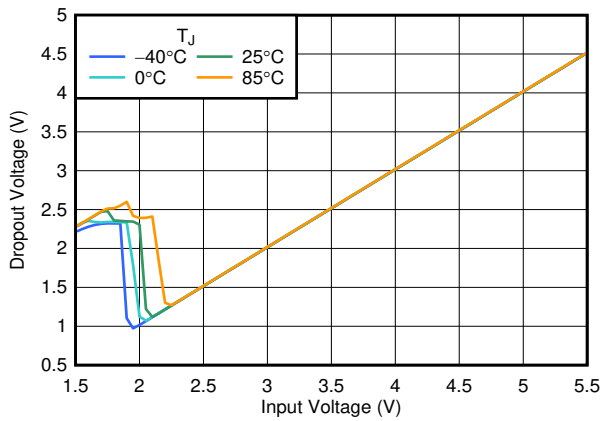
V_{OUT} = 1.0 V

图 6-3. Dropout Voltage vs I_{OUT}



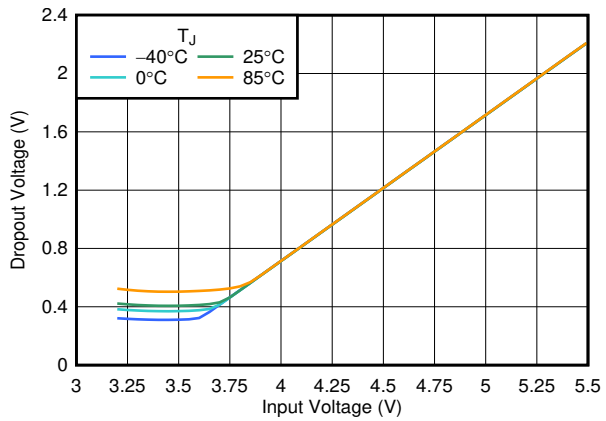
V_{OUT} = 3.3 V

图 6-4. Dropout Voltage vs I_{OUT}



V_{OUT} = 1.0 V

图 6-5. Dropout Voltage vs V_{IN}

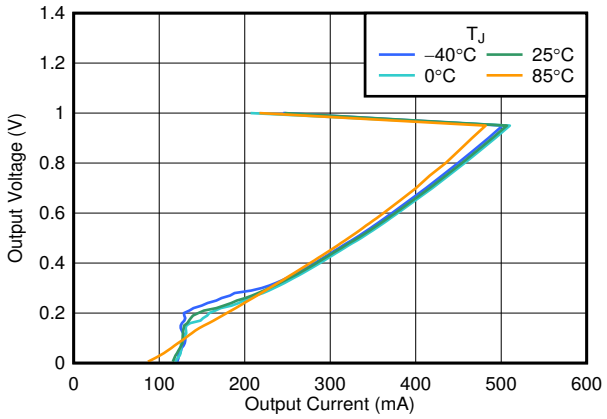


V_{OUT} = 3.3 V

图 6-6. Dropout Voltage vs V_{IN}

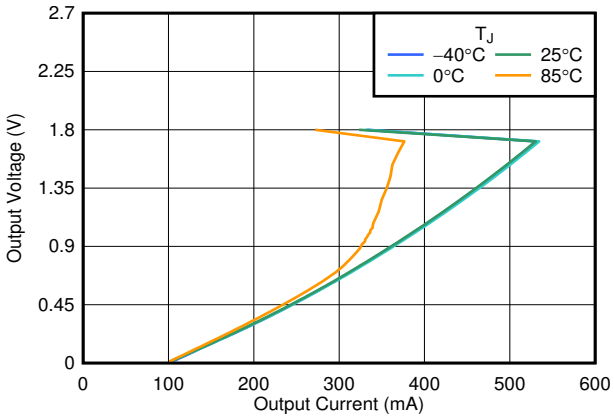
6.6 Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to 85°C), V_{IN} = $V_{OUT(nom)}$ + 2.1 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



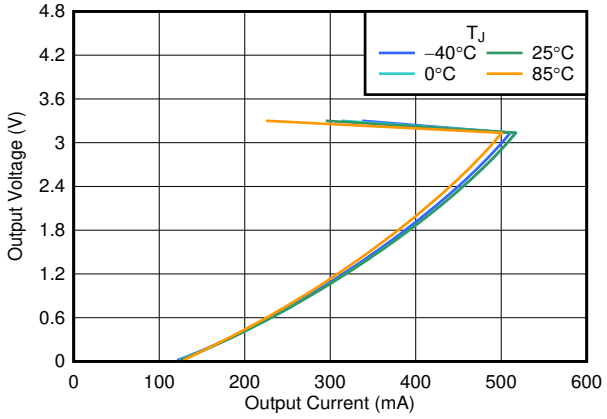
V_{OUT} = 1.0 V

图 6-7. Foldback Current Limit vs I_{OUT}



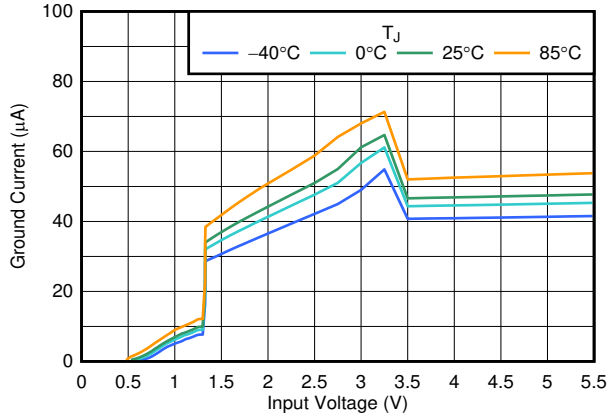
V_{OUT} = 1.8 V

图 6-8. Foldback Current Limit vs I_{OUT}



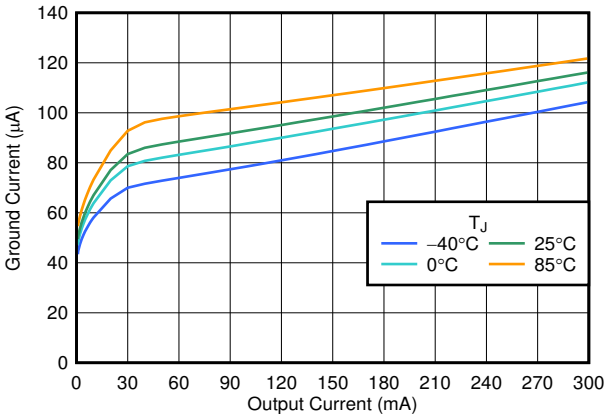
V_{OUT} = 3.3 V

图 6-9. Foldback Current Limit vs I_{OUT}



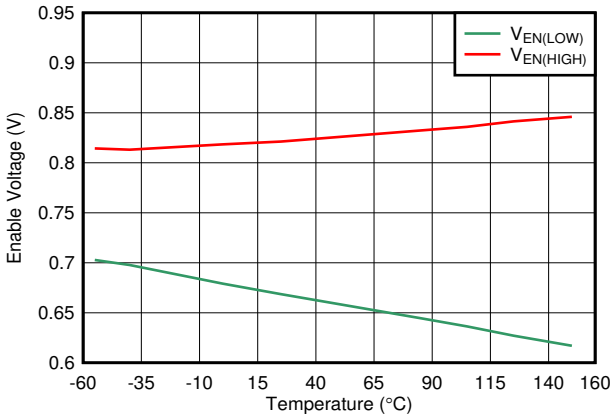
V_{OUT} = 3.3 V, I_{OUT} = 0 mA

图 6-10. I_{GND} vs V_{IN}



V_{OUT} = 3.3 V

图 6-11. I_{GND} vs I_{OUT}



V_{IN} = 5.5 V

图 6-12. EN High and Low Threshold vs Temperature

6.6 Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to 85°C), V_{IN} = $V_{OUT(nom)}$ + 2.1 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C

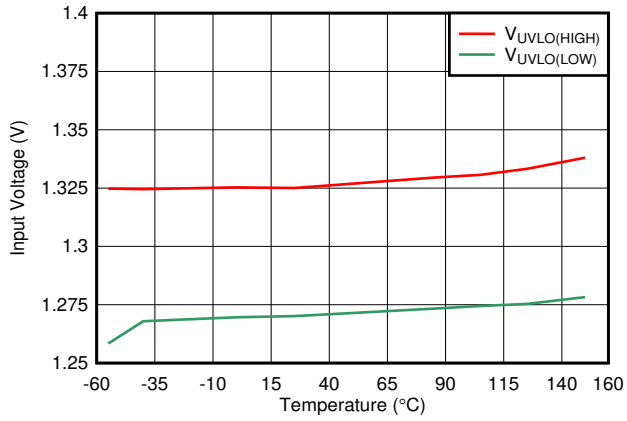
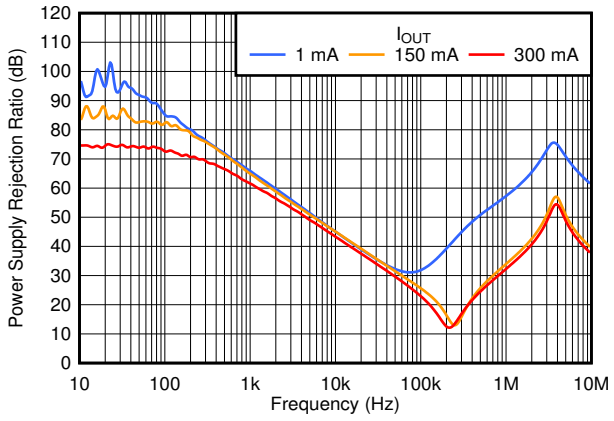
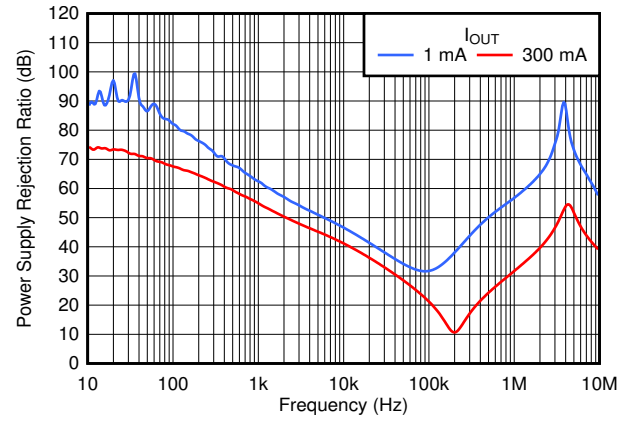


图 6-13. UVLO Rising and Falling Threshold vs Temperature



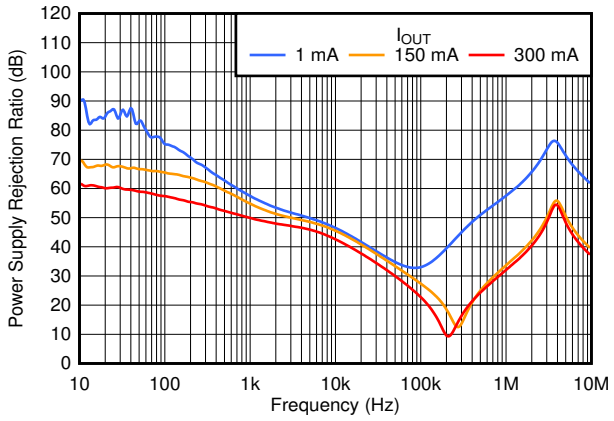
C_{IN} = open, V_{OUT} = 1.0 V

图 6-14. PSRR vs Frequency and I_{OUT}



C_{IN} = open, V_{OUT} = 1.8 V

图 6-15. PSRR vs Frequency and I_{OUT}



C_{IN} = open, V_{OUT} = 3.3 V

图 6-16. PSRR vs Frequency and I_{OUT}

6.6 Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to 85°C), V_{IN} = $V_{OUT(nom)}$ + 2.1 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C

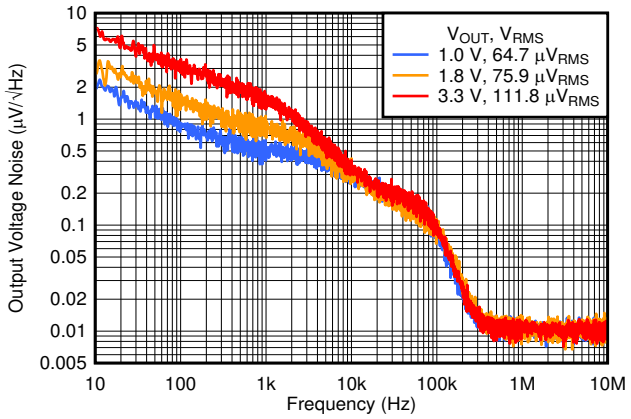
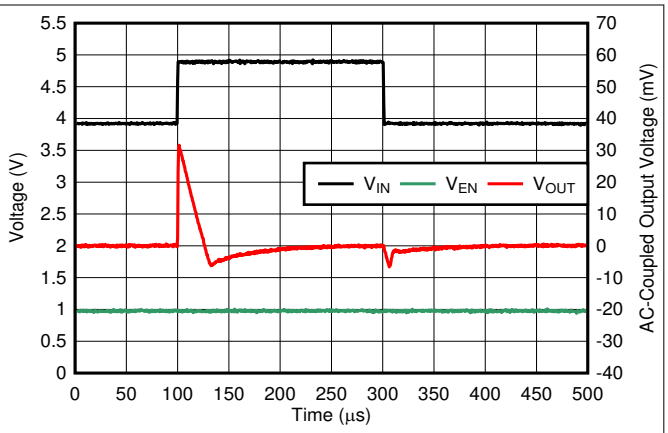
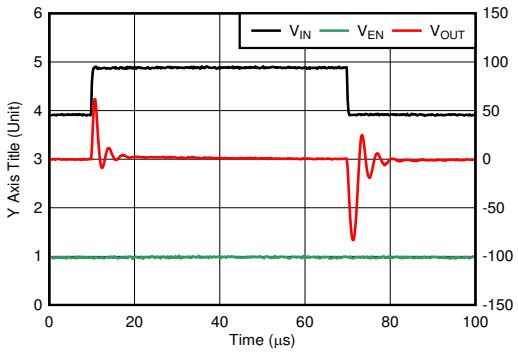


图 6-17. Output Noise vs Frequency and V_{OUT}



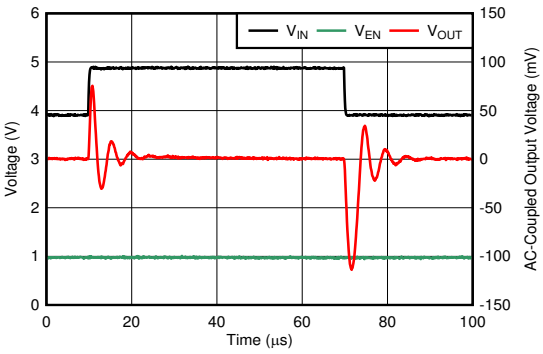
V_{IN} = 3.9 V to 4.9 V, slew rate = 1 V/µs, V_{EN} = 1 V, I_{OUT} = 1 mA

图 6-18. Line Transient



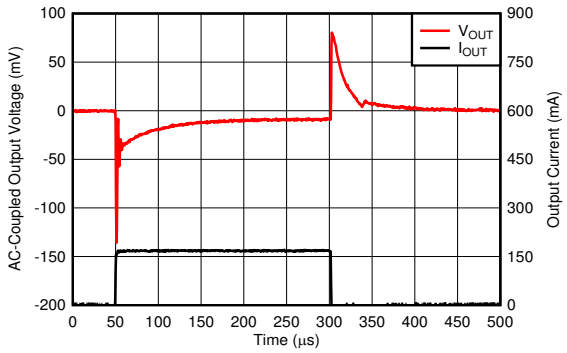
V_{IN} = 3.9 V to 4.9 V, slew rate = 1 V/µs, V_{EN} = 1 V, I_{OUT} = 150 mA

图 6-19. Line Transient



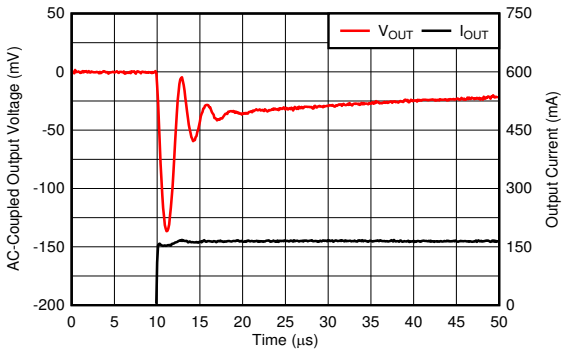
V_{IN} = 3.9 V to 4.9 V, slew rate = 1 V/µs, V_{EN} = 1 V, I_{OUT} = 300 mA

图 6-20. Line Transient



V_{IN} = 3.9 V, V_{EN} = 1 V, I_{OUT} = 1 mA to 150 mA, slew rate = 1 A/µs

图 6-21. Load Transient

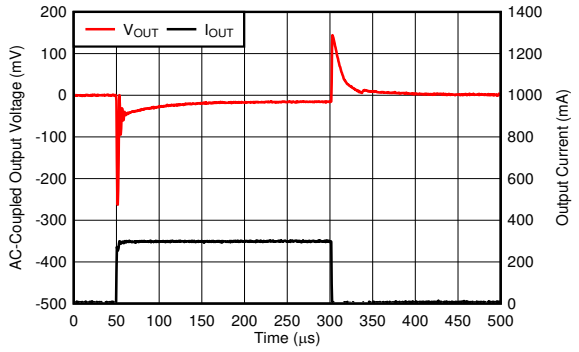


V_{IN} = 3.9 V, V_{EN} = 1 V, I_{OUT} = 1 mA to 150 mA, slew rate = 1 A/µs, rising edge

图 6-22. Load Transient

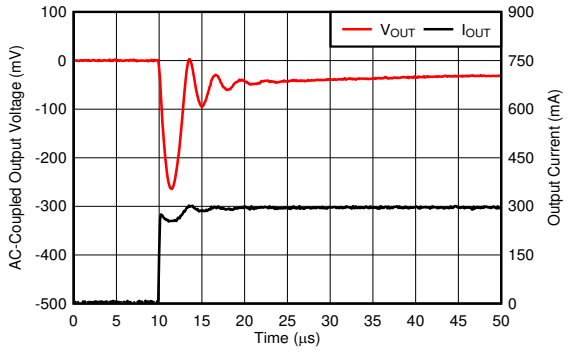
6.6 Typical Characteristics (continued)

over operating temperature range (T_J = –40°C to 85°C), V_{IN} = $V_{OUT(nom)}$ + 2.1 V, I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C



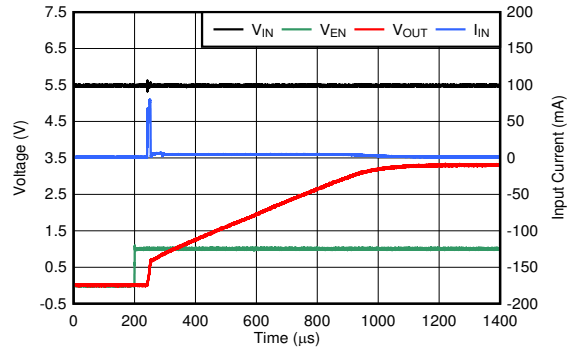
V_{IN} = 3.9 V, V_{EN} = 1 V, I_{OUT} = 1 mA to 300 mA, slew rate = 1 A/µs

图 6-23. Load Transient



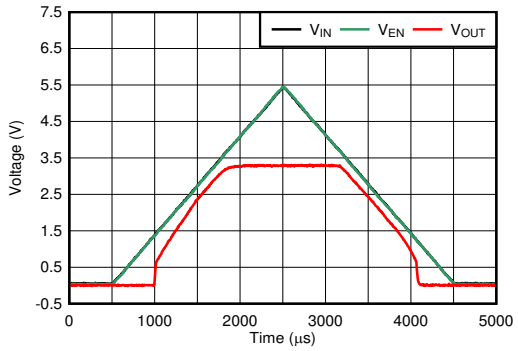
V_{IN} = 3.9 V, V_{EN} = 1 V, I_{OUT} = 1 mA to 300 mA, slew rate = 1 A/µs, rising edge

图 6-24. Load Transient



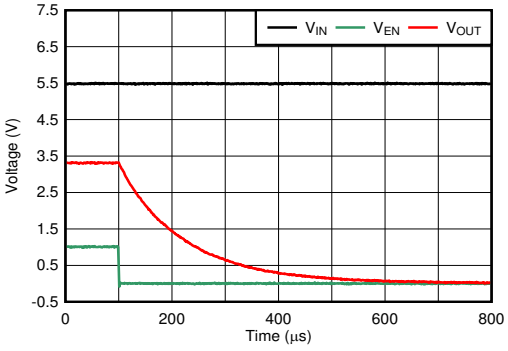
V_{IN} = 5.5 V, C_{IN} = open, I_{OUT} = open

图 6-25. Start-Up With EN, Inrush Current



V_{IN} = 0 V to 5.5 V to 0 V, I_{OUT} = 150 mA

图 6-26. Start-Up and Shutdown



V_{IN} = 5.5 V, V_{EN} = 1 V to 0 V, I_{OUT} = open

图 6-27. Shutdown Response With Enable

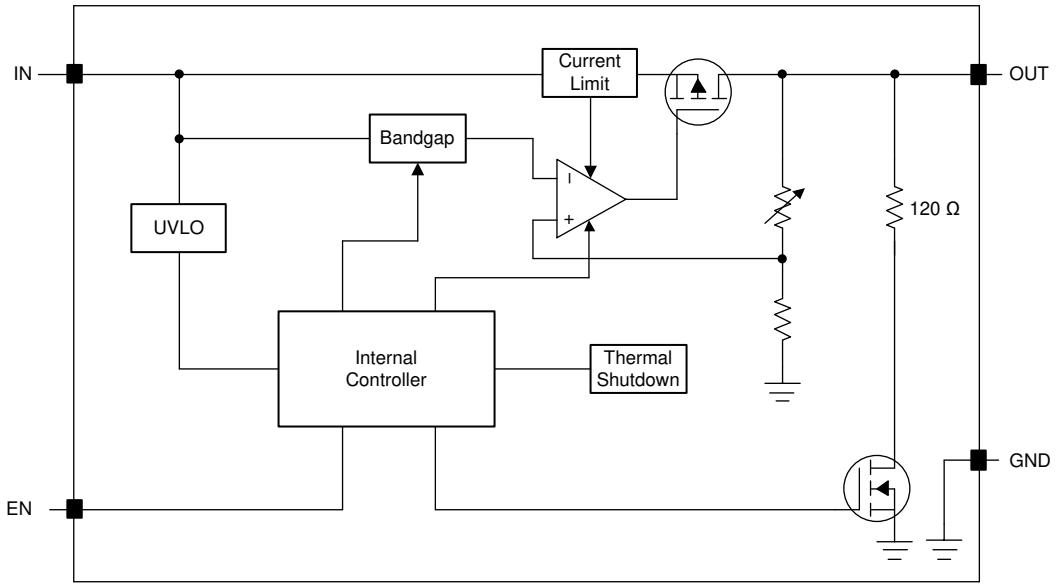
7 Detailed Description

7.1 Overview

The TLV740P is a cost-effective low-dropout (LDO) regulator that consumes low quiescent current and delivers excellent line and load transient performance. These characteristics make the device ideal for a wide range of portable applications.

This LDO offers foldback current limit, output enable, active discharge, undervoltage lockout (UVLO), and thermal protection.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 0.95\ V \times V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{CL}]$. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{SC}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

图 7-1 shows a diagram of the foldback current limit.

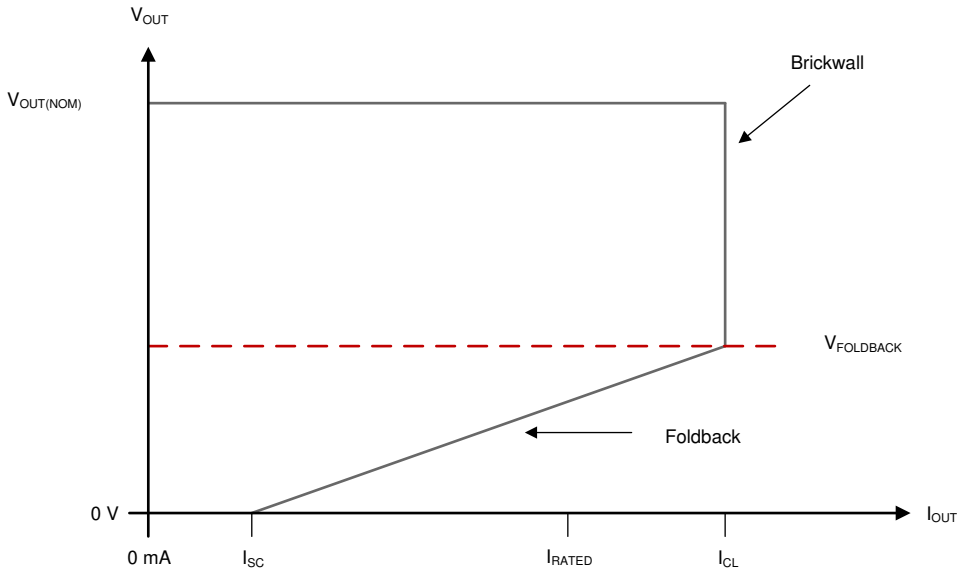


图 7-1. Foldback Current Limit

7.3.2 Output Enable

The enable pin (EN) is active high. Enable the device by forcing the voltage of the enable pin to exceed the minimum EN pin high-level input voltage (see the *Electrical Characteristics* table). Turn off the device by forcing the voltage of the enable pin to drop below the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). If shutdown capability is not required, connect EN to IN.

This device has an internal pulldown circuit that activates when the device is disabled to actively discharge the output voltage.

7.3.3 Active Discharge

The device has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

7.3.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit ensures that the device stays disabled before its input supply reaches the minimum operational voltage range, and ensures that the device shuts down when the input supply collapses. 图 7-2 illustrates the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.

- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

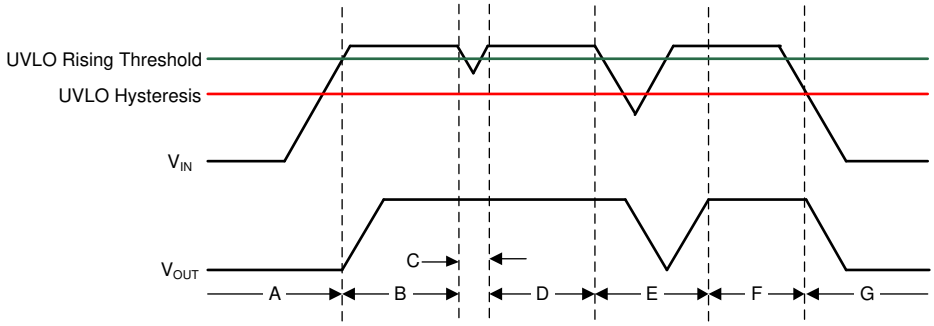


图 7-2. Typical UVLO Operation

7.3.5 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

7.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

The device requires an input capacitor of 1.0 µF or larger, as specified in the *Recommended Operating Conditions* table for stability. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

The device also requires an output capacitor of 1.0 µF or larger, as specified in the *Recommended Operating Conditions* table for stability. Dynamic performance of the device is improved by using a higher capacitor than the minimum output capacitor.

8.1.3 Dropout Voltage

The device uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout.

8.1.4 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on V_{IN} during start-up. As with other LDOs, the output can overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in 图 8-1, when the slew rate and voltage levels are in the correct range. Use an enable signal to delay the LDO startup to avoid V_{OUT} overshoot resulting from dropout exit. The enable signal can be set high after V_{IN} is greater than $V_{OUT(nom)}$.

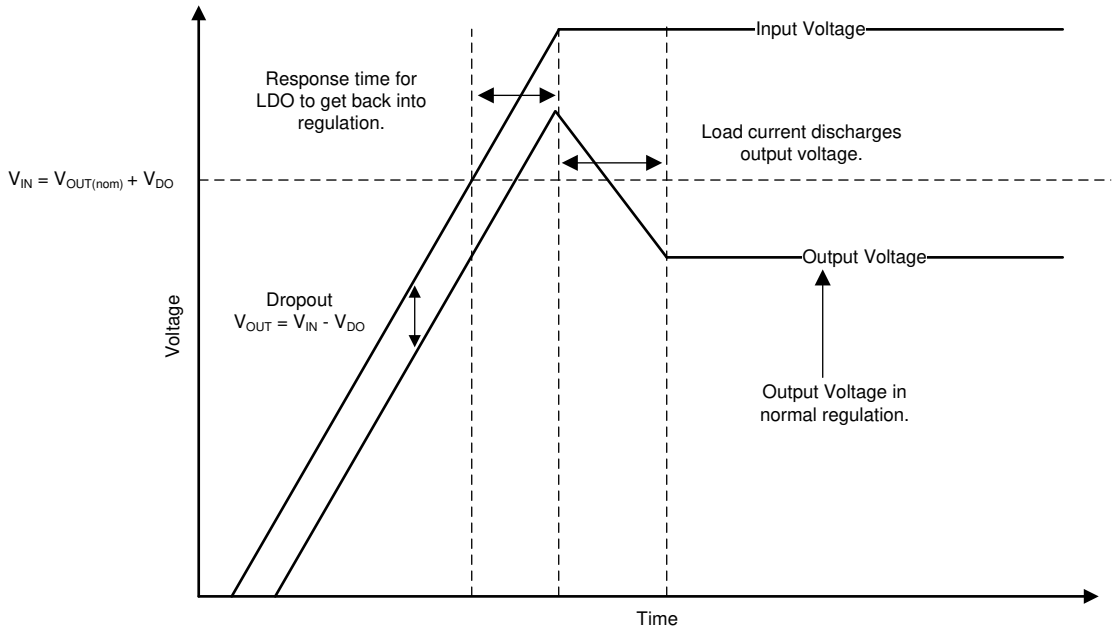


图 8-1. Start-Up Into Dropout

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. 图 8-2 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (V_{GS}) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

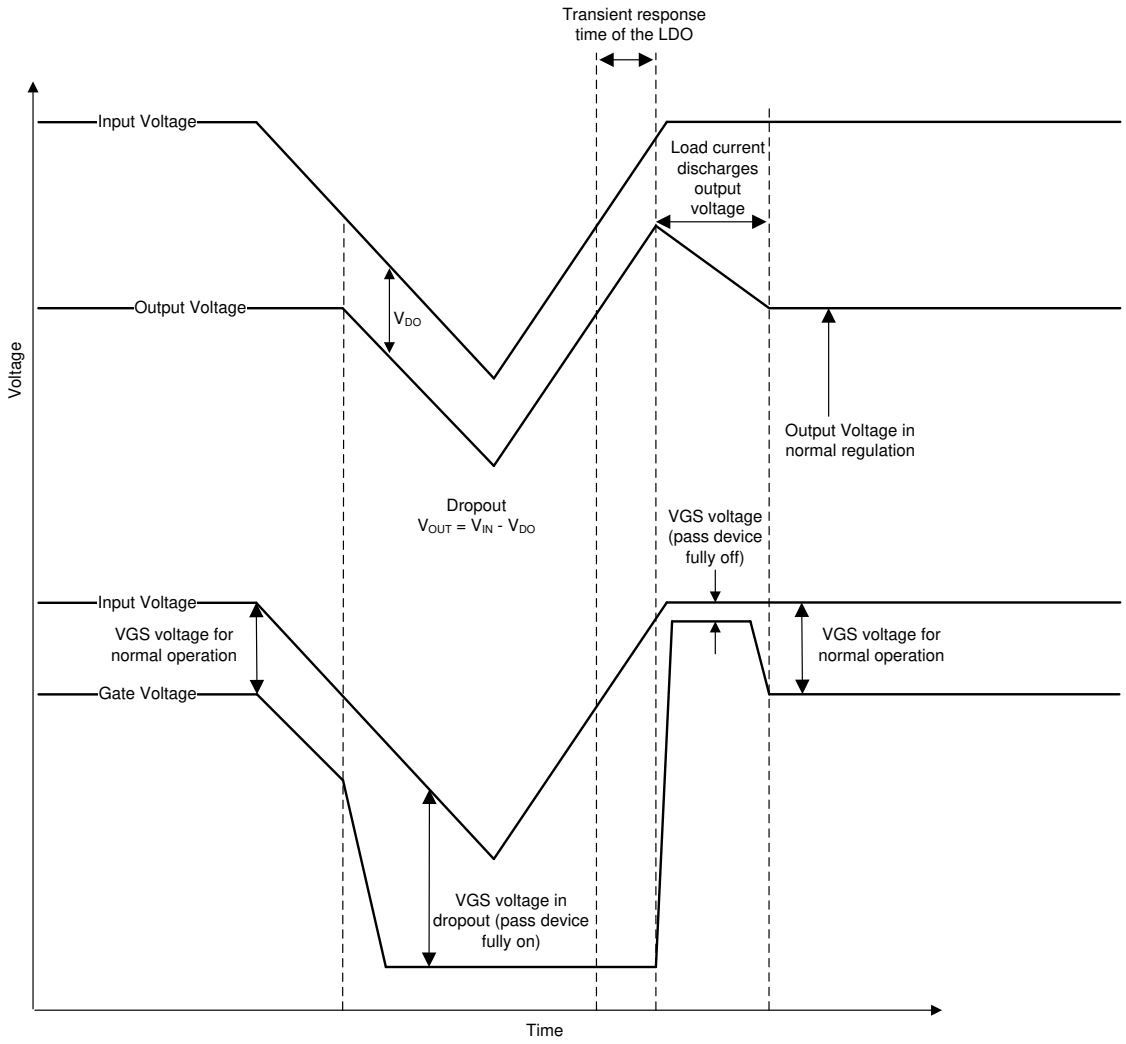


图 8-2. Line Transients From Dropout

8.1.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

8.1.6 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass element instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection must be used to protect the device. 图 8-3 shows one approach of protecting the device.

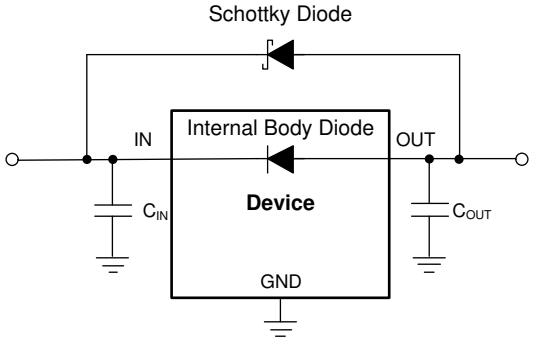


图 8-3. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.7 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use 方程式 2 to approximate P_D:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TLV740P allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the DQN package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to 方程式 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). 方程式 4 rearranges 方程式 3 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (4)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Recommended Operating Conditions* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the X2SON package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

8.1.7.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 方程式 5 and are given in the *Recommended Operating Conditions* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \quad (5)$$

where:

- P_D is the power dissipated as explained in 方程式 2
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

8.1.7.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in 图 8-4 and can be separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output (V_{IN} – V_{OUT}) at a given output current level. See the *Dropout Voltage* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - The shape of the slope is given by 方程式 4. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO; thus when V_{IN} – V_{OUT} increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of V_{IN} – V_{OUT}.

图 8-4 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{\theta JA}$ as given in the *Recommended Operating Conditions* table.

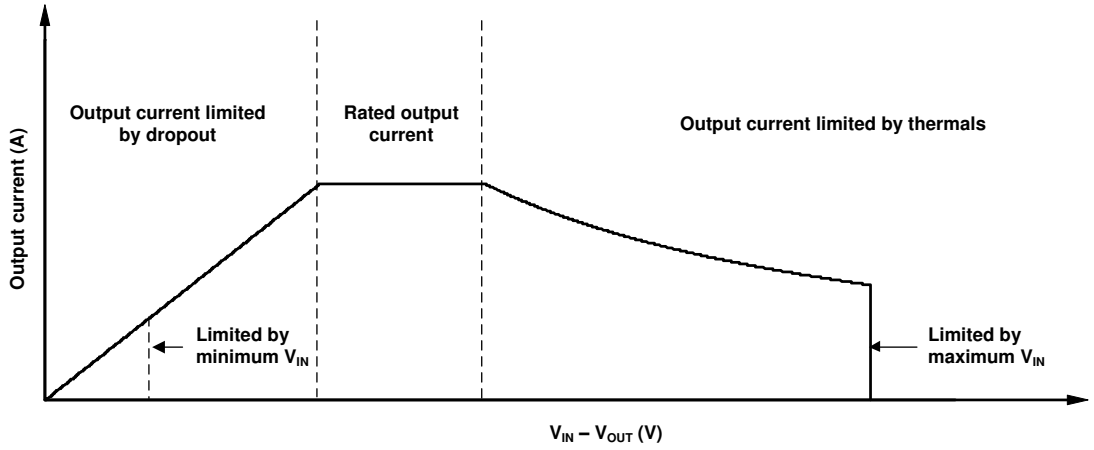


图 8-4. Region Description of Continuous Operation Regime

8.2 Typical Application

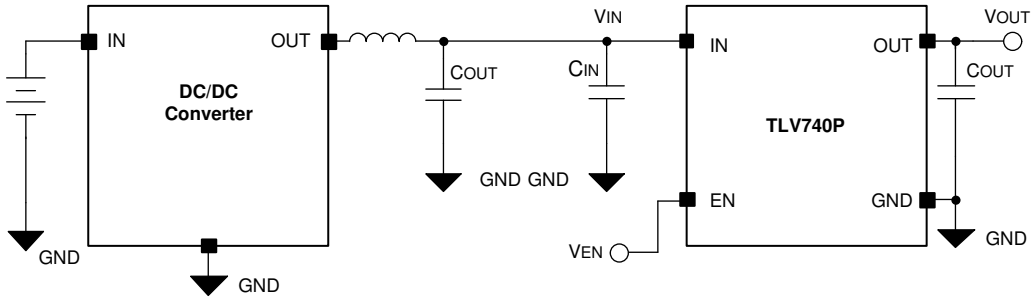


图 8-5. Operation From a DC/DC Converter

8.2.1 Design Requirements

表 8-1 summarizes the design requirement for this application.

表 8-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.9 V
Output voltage	1.8 V
Output load	30 mA
Output Capacitor	1 µF

8.2.2 Detailed Design Procedure

For this design example, the 1.8-V output voltage device is selected. The device is powered by DC/DC converter connected to a battery. A 2.1-V headroom between V_{IN} and V_{OUT} is used to keep the device within the dropout voltage specification and to ensure the device stays in regulation under all load conditions for this design.

8.2.3 Application Curves

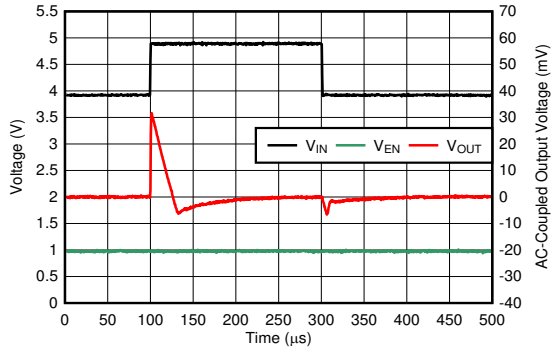


图 8-6. VIN Line Transient, I_{OUT} = 1 mA

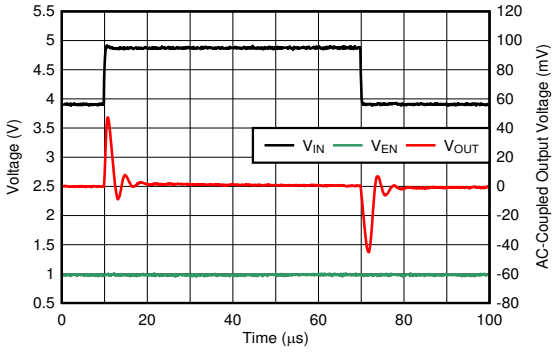


图 8-7. VIN Line Transient, I_{OUT} = 30 mA

8.3 What to Do and What Not to Do

Place at least one 1-µF ceramic capacitor as close as possible to the OUT pin of the regulator for best transient performance.

Place at least one 1-µF capacitor as close as possible to the IN pin for best transient performance.

Do not place the output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not continuously operate the device in current limit or near thermal shutdown.

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.4 V to 5.5 V. The input supply must be well regulated and free of spurious noise. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 2.1 V. TI requires using a 1 µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections, in order to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Only place tented thermal vias directly beneath the thermal pad of the DQN package. An untented via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

10.2 Layout Examples

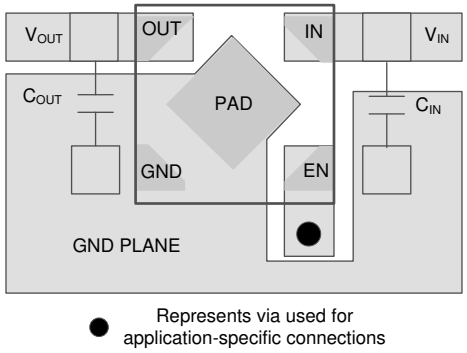


图 10-1. Layout Example for the DQN Package

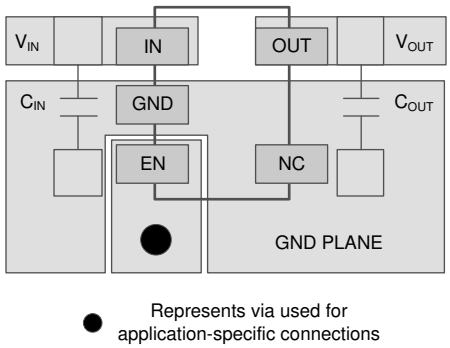


图 10-2. Layout Example for the DBV Package

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Device Nomenclature

表 11-1. Ordering Information(1) (2)

PRODUCT	V_O
TLV740**xx(x)Pyyyz**	**XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 175 = 1.75 V). **P** is optional; devices with P have an LDO regulator with an active output discharge. **YYY** is the package designator. **Z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

(2) Output voltages from 1.0 V to 3.3 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

-
- Texas Instruments, *Universal Low-Dropout (LDO) Linear Voltage Regulator MultiPkgLDOEVM-823 Evaluation Module* user's guide
- Texas Instruments, *Using New Thermal Metrics* application report

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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所有商标均为其各自所有者的财产。

11.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV74010PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	74010
TLV74010PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74010
TLV74010PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	10
TLV74010PDQNR.A	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	10
TLV74012PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	12
TLV74012PDQNR.A	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	12
TLV74018PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	74018
TLV74018PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74018
TLV74018PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	18
TLV74018PDQNR.A	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	18
TLV74028PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	28
TLV74028PDQNR.A	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	28
TLV74033PDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	74033
TLV74033PDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74033
TLV74033PDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74033
TLV74033PDBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74033
TLV74033PDQNR	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	33
TLV74033PDQNR.A	Active	Production	X2SON (DQN) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	33

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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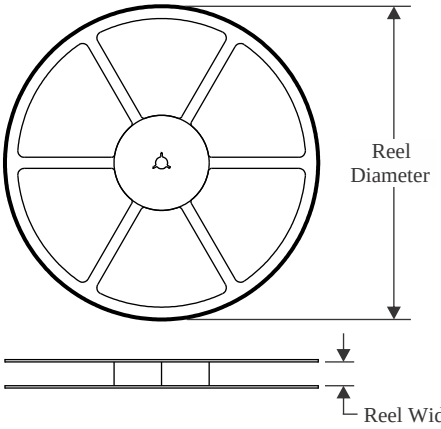
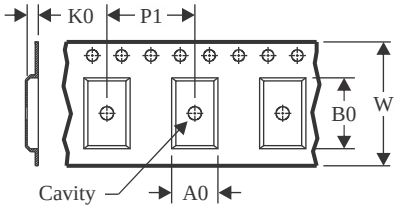
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

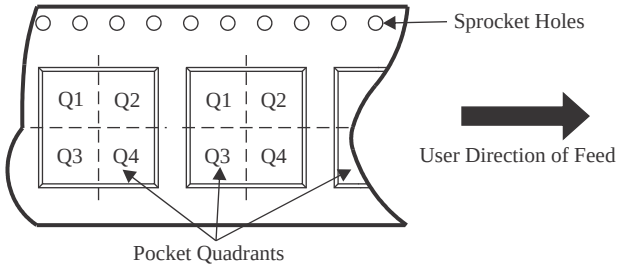


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

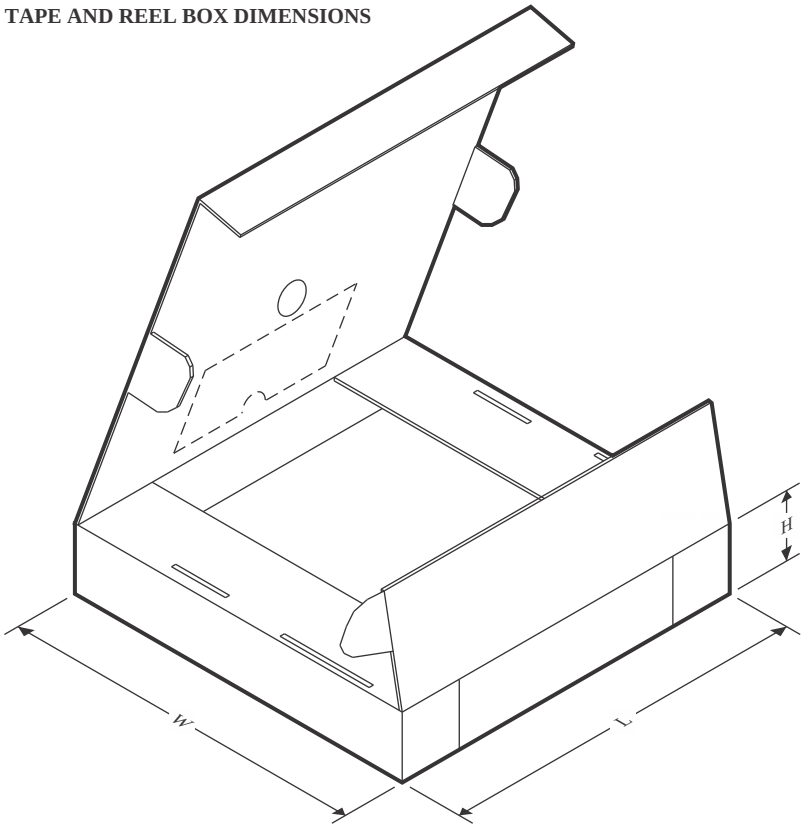
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV74010PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74010PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74012PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74018PDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74018PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74018PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74028PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74033PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74033PDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74033PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

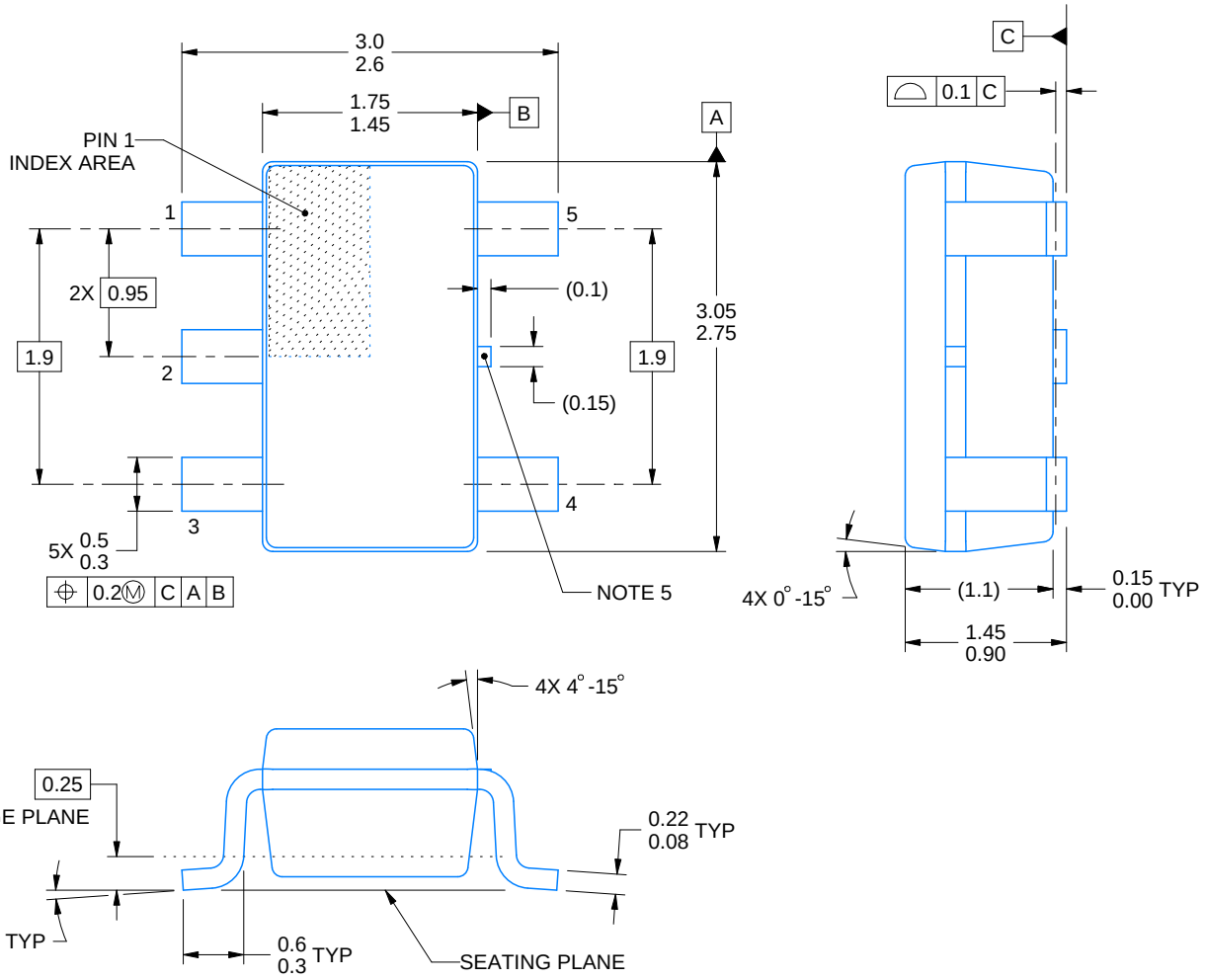
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV74010PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74010PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74012PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74018PDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV74018PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74018PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74028PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74033PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74033PDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74033PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

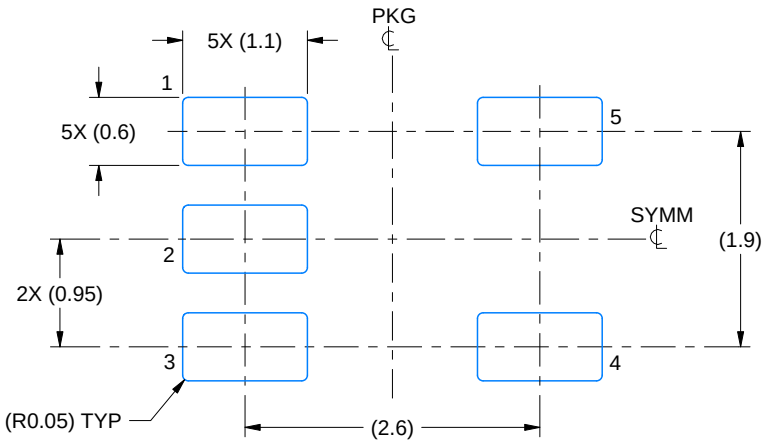
SMALL OUTLINE TRANSISTOR



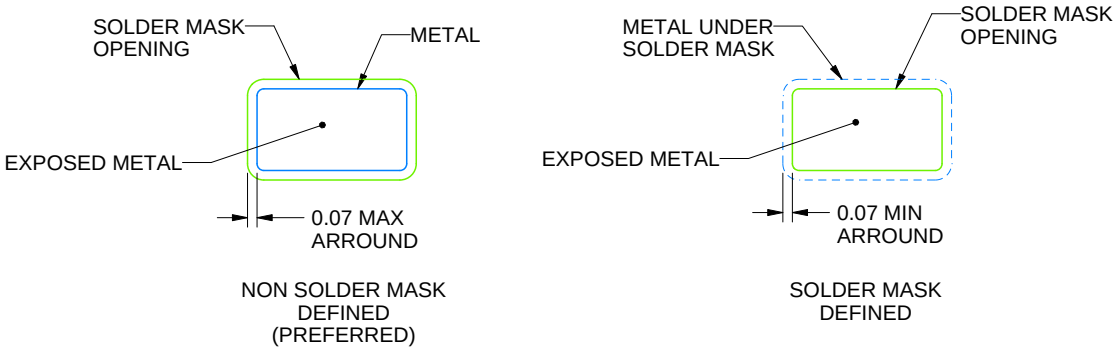
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

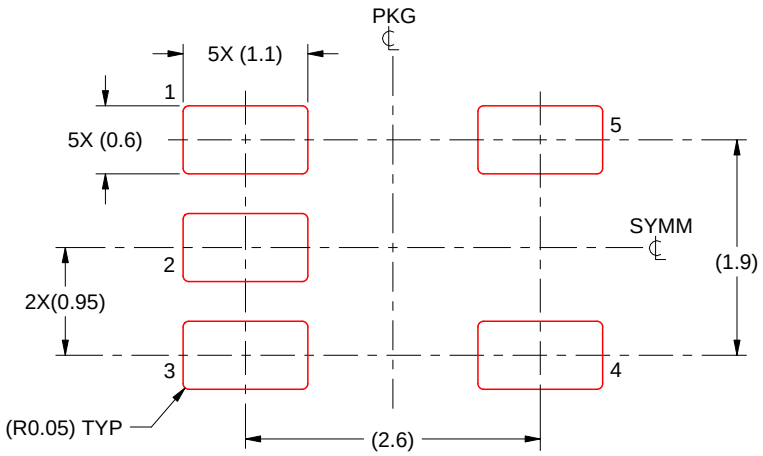


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

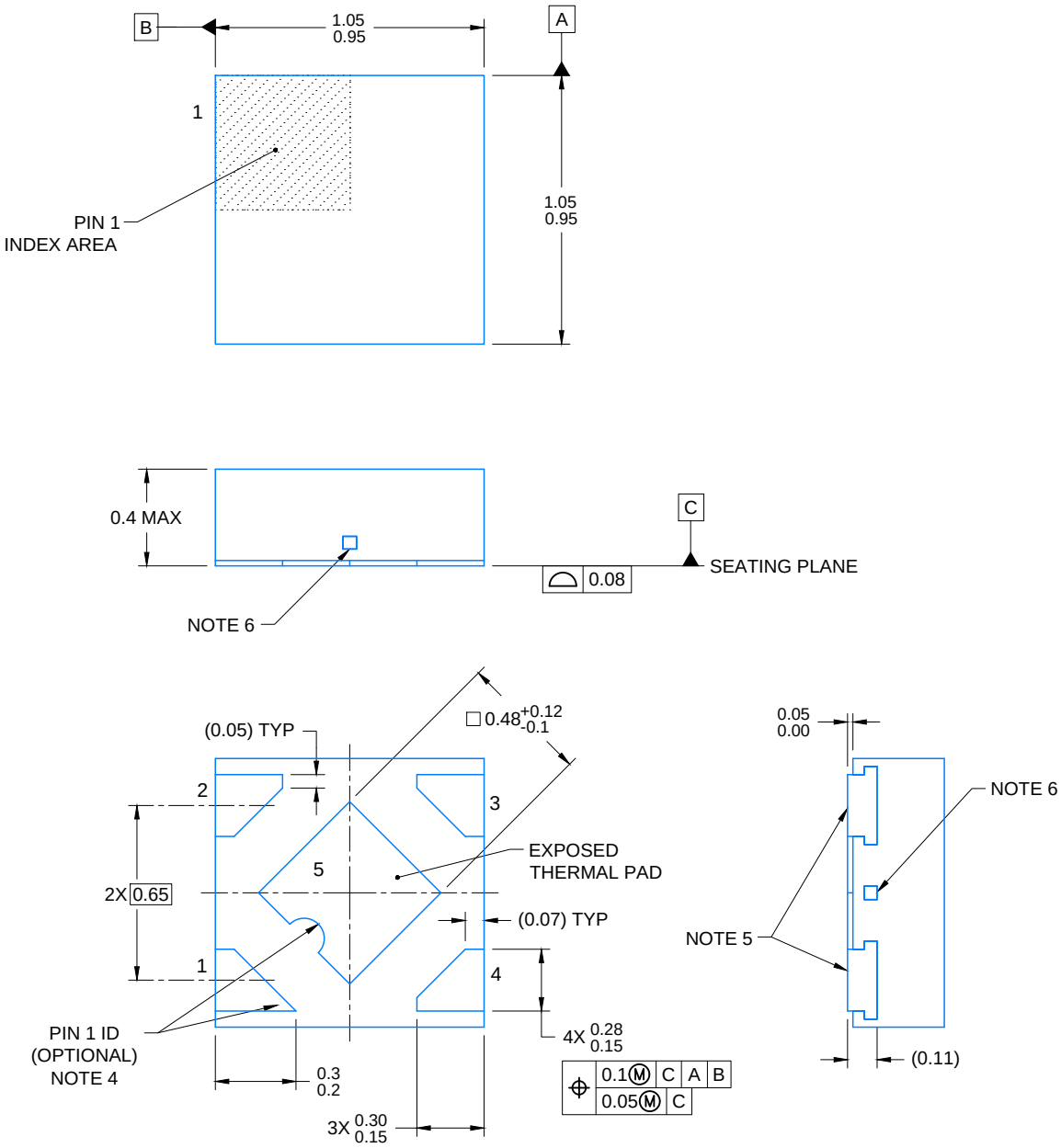
4210367/F

PACKAGE OUTLINE

DQN0004A

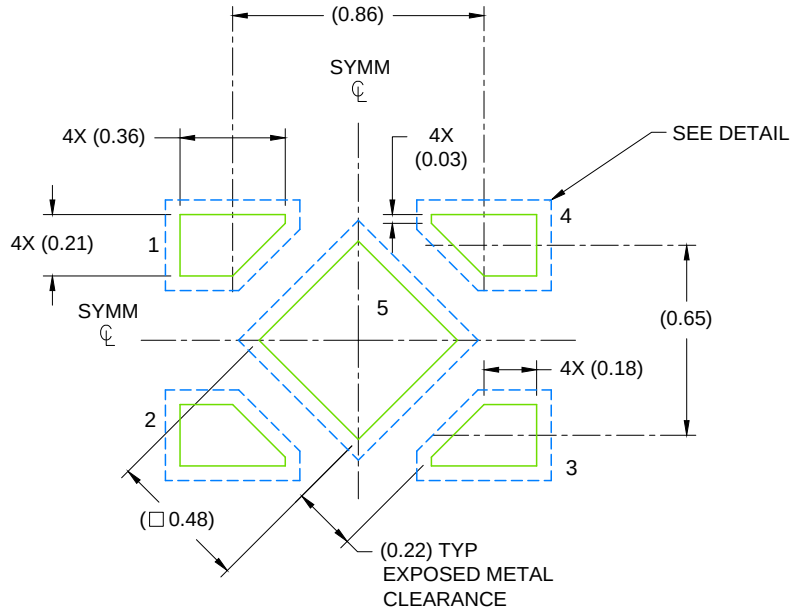
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



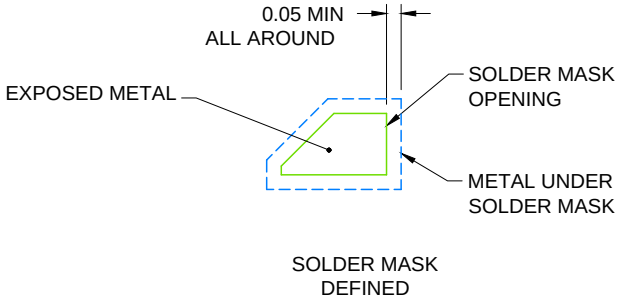
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE

SCALE: 40X

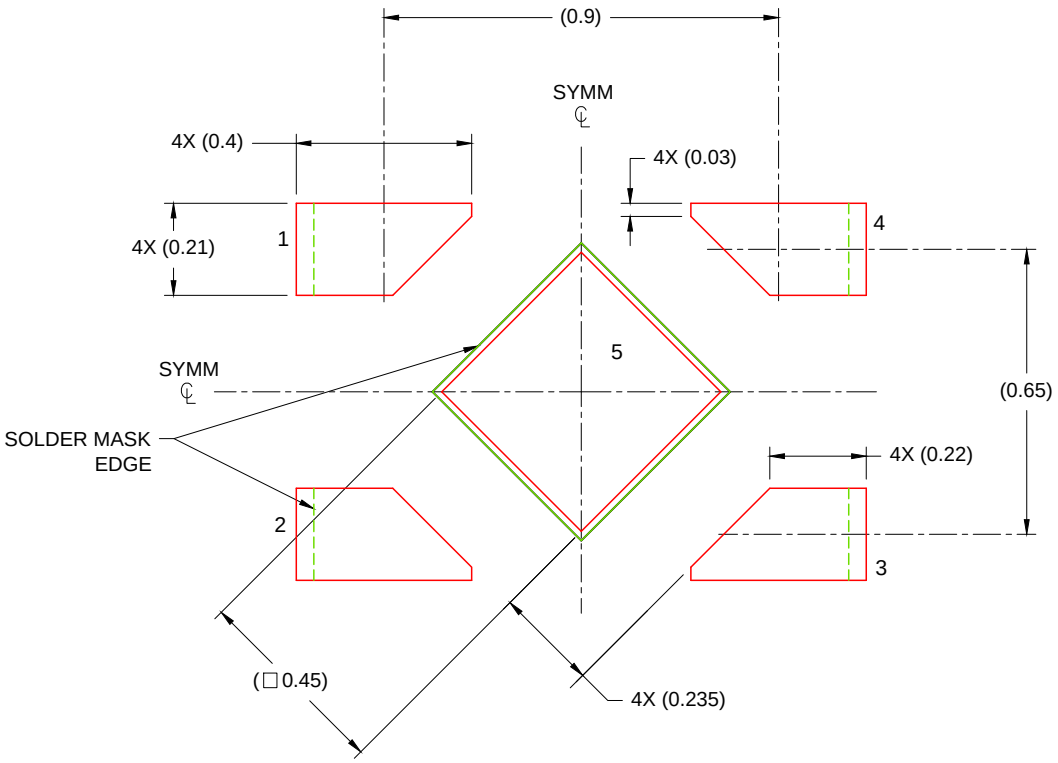


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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