

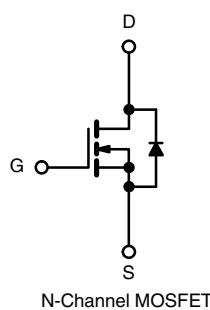
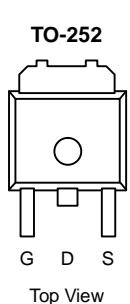
# FDD850N10L-VB Datasheet

## N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY			
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ.)
100	0.055 at $V_{GS} = 10$ V	25	21nC
	0.057 at $V_{GS} = 4.5$ V	25	

### FEATURES

- TrenchFET® power MOSFET
- 100 % UIS tested



### APPLICATIONS

- Primary side switch

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175$ °C)	$T_C = 25$ °C	$I_D$	25	A
	$T_C = 70$ °C		20	
	$T_A = 25$ °C		12 b, c	
	$T_A = 70$ °C		10 b, c	
Pulsed Drain Current		$I_{DM}$	75	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	$I_S$	50 e	
	$T_A = 25$ °C		6.9 b, c	
Avalanche Current Pulse		$I_{AS}$	33	
Single Pulse Avalanche Energy	$L = 0.1$ mH	$E_{AS}$	55	mJ
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	83	W
	$T_C = 70$ °C		58	
	$T_A = 25$ °C		8.3 b, c	
	$T_A = 70$ °C		5.8 b, c	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +175	°C

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient b, d	$t \leq 10$ s	$R_{thJA}$	15	18	°C/W
Maximum Junction-to-Case	Steady State	$R_{thJC}$	1.5	1.8	

### Notes

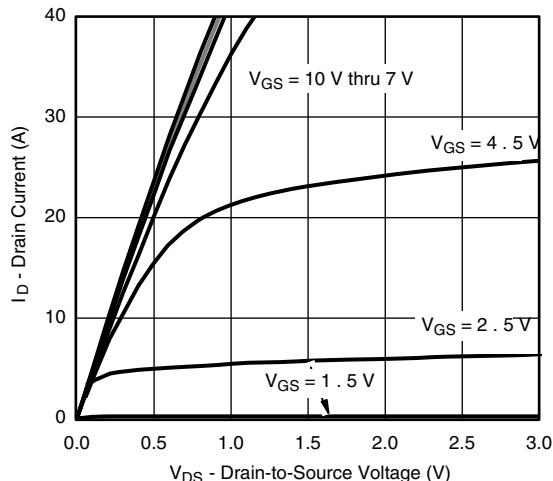
- Based on  $T_C = 25$  °C.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$  s.
- Maximum under steady state conditions is 50 °C/W.
- Calculated based on maximum junction temperature. Package limitation current is 50 A.

SPECIFICATIONS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$	100	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$	-	165	-	mV/°C
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$		-	-11	-	
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$	1.0		3.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}$ , $V_{GS} = \pm 20 \text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100 \text{ V}$ , $V_{GS} = 0 \text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 55^\circ\text{C}$	-	-	10	
On-State Drain Current <sup>a</sup>	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$ , $V_{GS} = 10 \text{ V}$	25	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$ , $I_D = 12 \text{ A}$	-	0.055		$\Omega$
		$V_{GS} = 4.5 \text{ V}$ , $I_D = 8 \text{ A}$		0.057		
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15 \text{ V}$ , $I_D = 12 \text{ A}$	-	25	-	S
<b>Dynamic <sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 12 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$	-	1800	-	pF
Output Capacitance	$C_{oss}$		-	180	-	
Reverse Transfer Capacitance	$C_{rss}$		-	60	-	
Total Gate Charge	$Q_g$	$V_{DS} = 50 \text{ V}$ , $V_{GS} = 10 \text{ V}$ , $I_D = 12 \text{ A}$	-	21	32	nC
Gate-Source Charge	$Q_{gs}$		-	10	-	
Gate-Drain Charge	$Q_{gd}$		-	9	-	
Gate Resistance	$R_g$	$f = 1 \text{ MHz}$	-	1.5	-	$\Omega$
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 50 \text{ V}$ , $R_L = 5 \Omega$ $I_D \geq 10 \text{ A}$ , $V_{GEN} = 10 \text{ V}$ , $R_g = 1 \Omega$	-	10	15	ns
Rise Time	$t_r$		-	10	15	
Turn-Off Delay Time	$t_{d(\text{off})}$		-	15	25	
Fall Time	$t_f$		-	10	15	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	-	-	50	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	40	
Body Diode Voltage	$V_{SD}$	$I_S = 10 \text{ A}$	-	0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $T_J = 25^\circ\text{C}$	-	50	75	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	100	150	
Reverse Recovery Fall Time	$t_a$		-	38	-	ns
Reverse Recovery Rise Time	$t_b$		-	12	-	

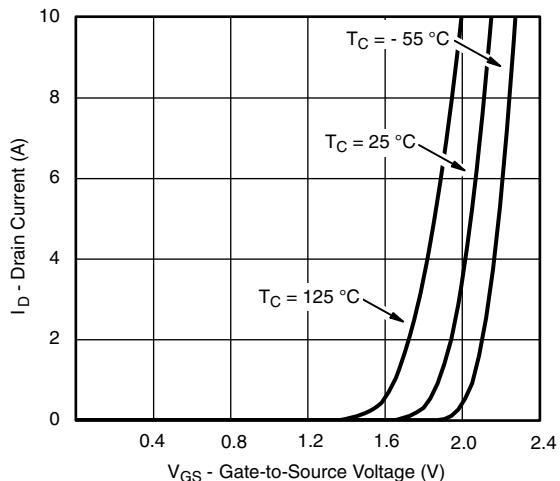
**Note**

- a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

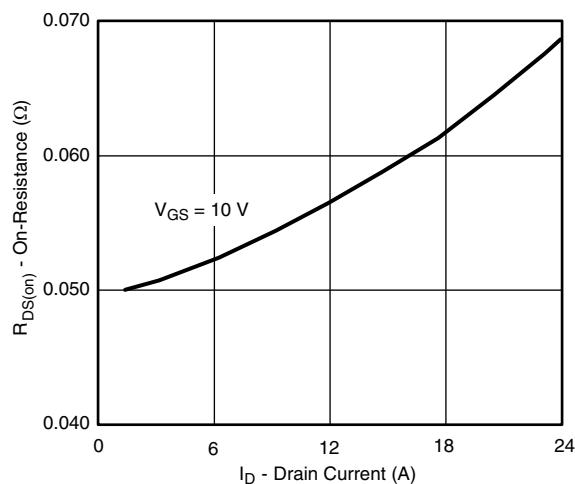
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)


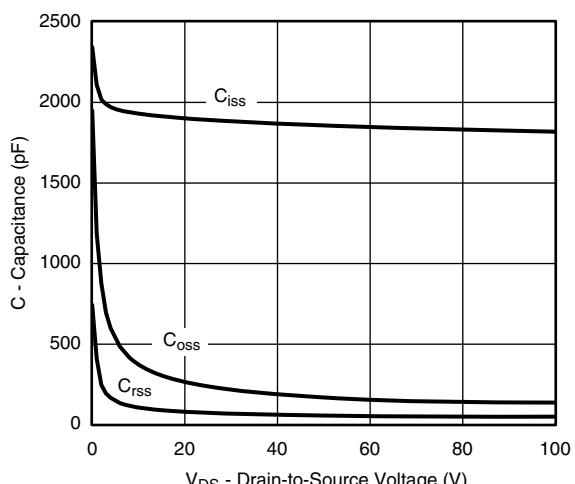
Output Characteristics



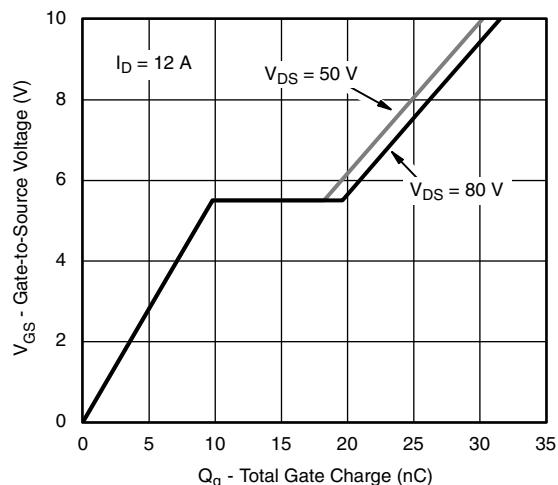
Transfer Characteristics



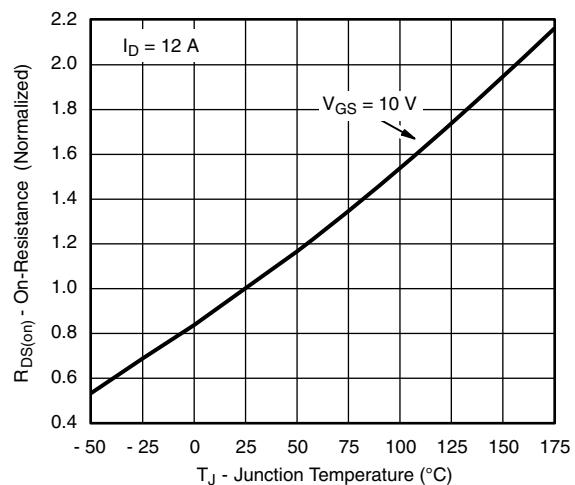
On-Resistance vs. Drain Current



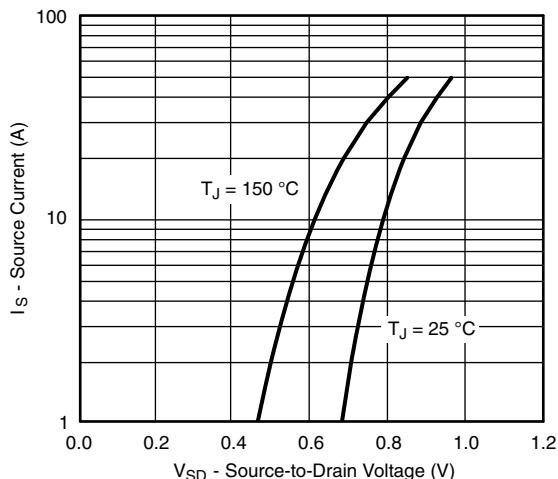
Capacitance



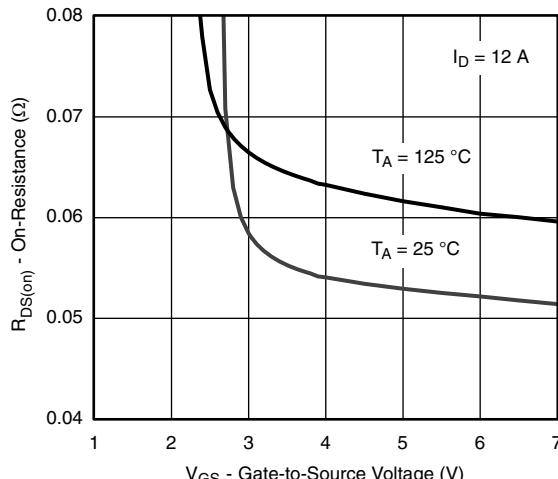
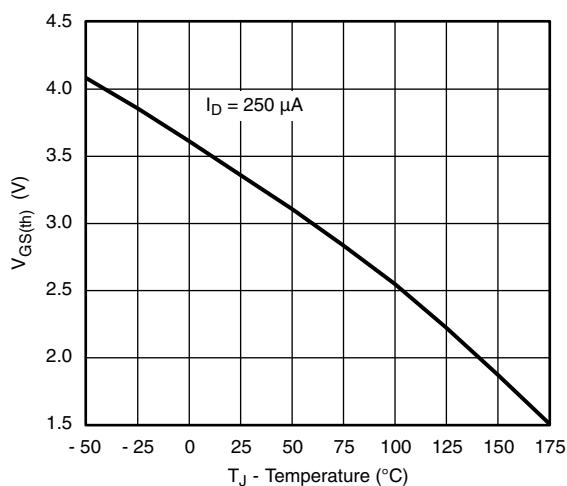
Gate Charge



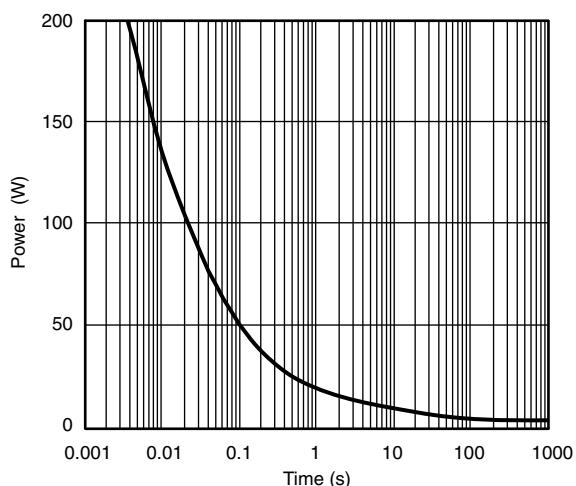
On-Resistance vs. Junction Temperature

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)


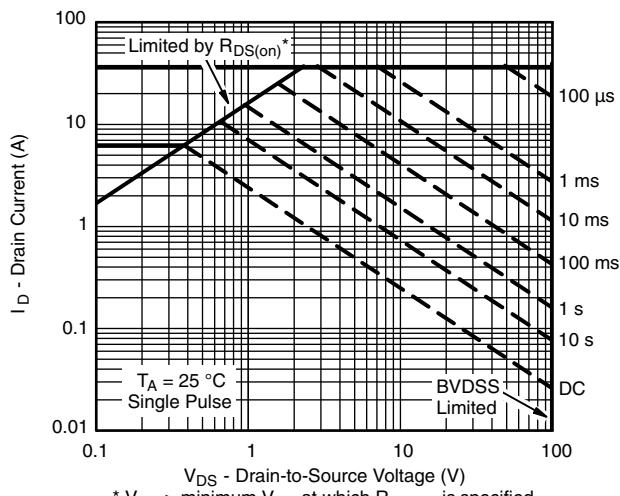
Source-Drain Diode Forward Voltage

 $R_{DS(on)}$  vs.  $V_{GS}$  vs. Temperature

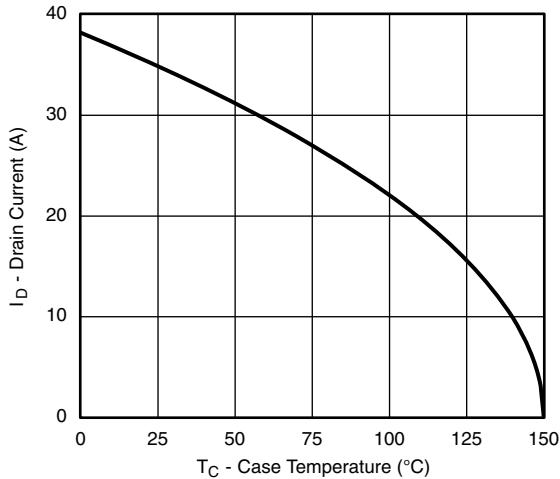
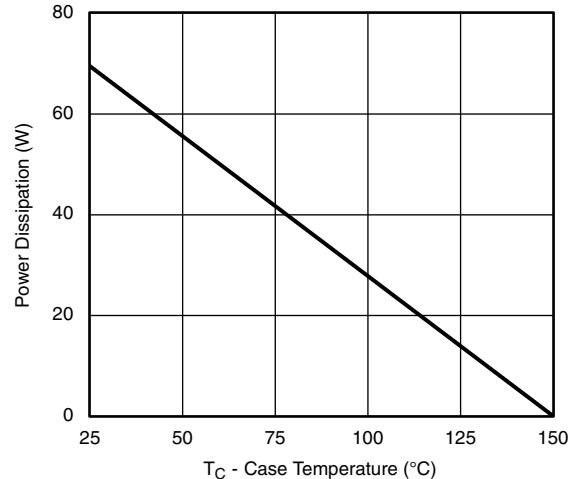
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



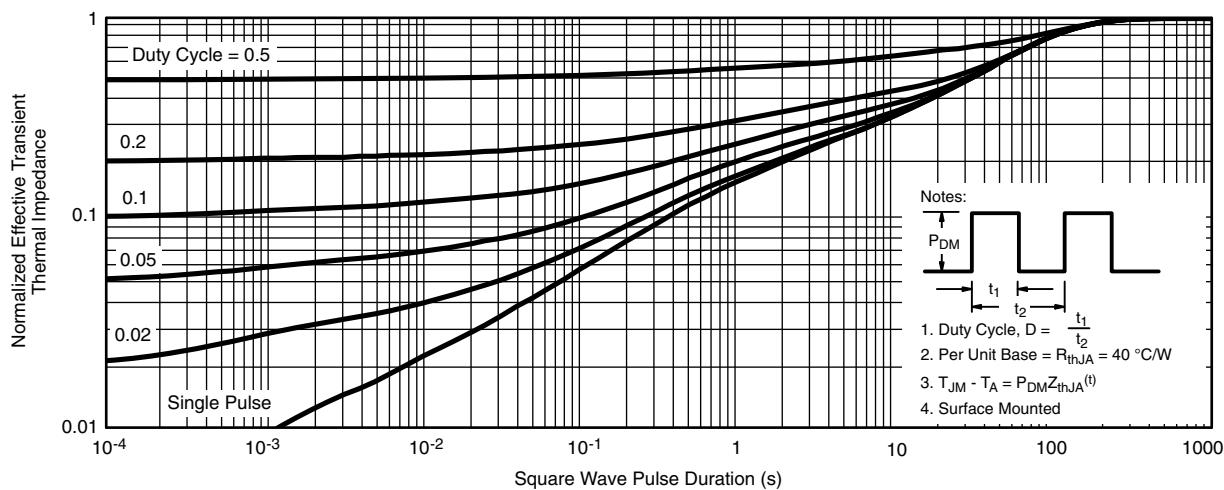
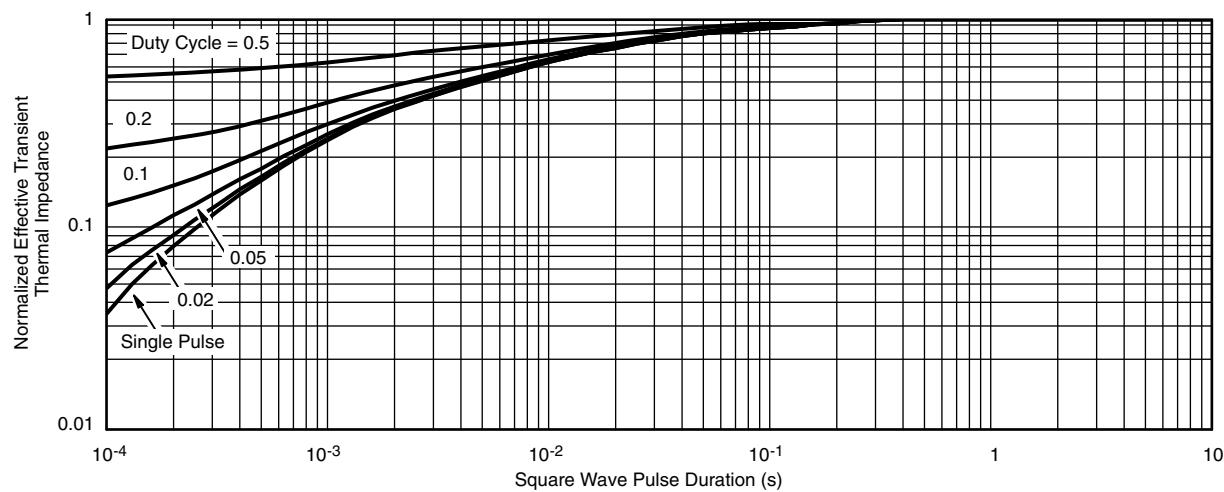
Safe Operating Area

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)
Current Derating <sup>a</sup>

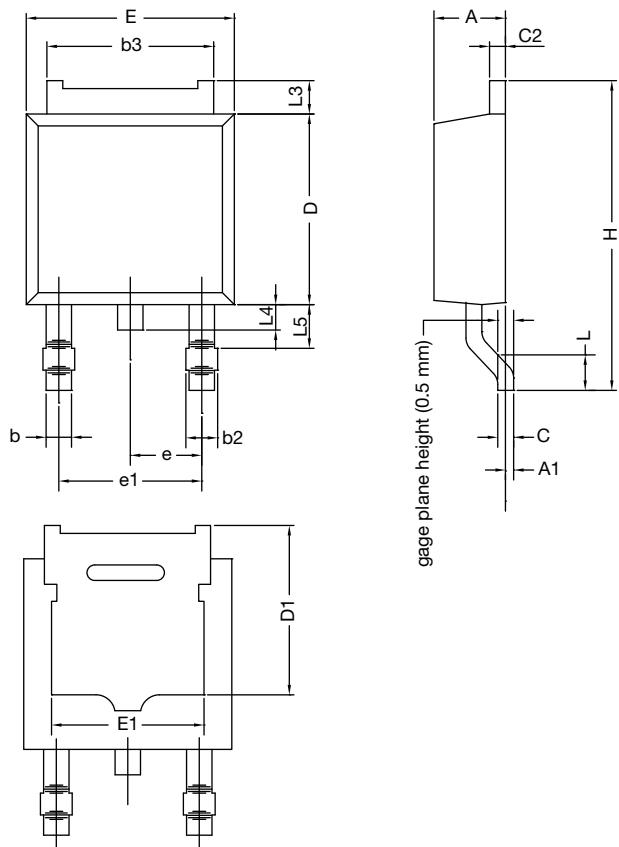
Power Derating

**Note**

- a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Normalized Thermal Transient Impedance, Junction-to-Case**

## TO-252AA Case Outline



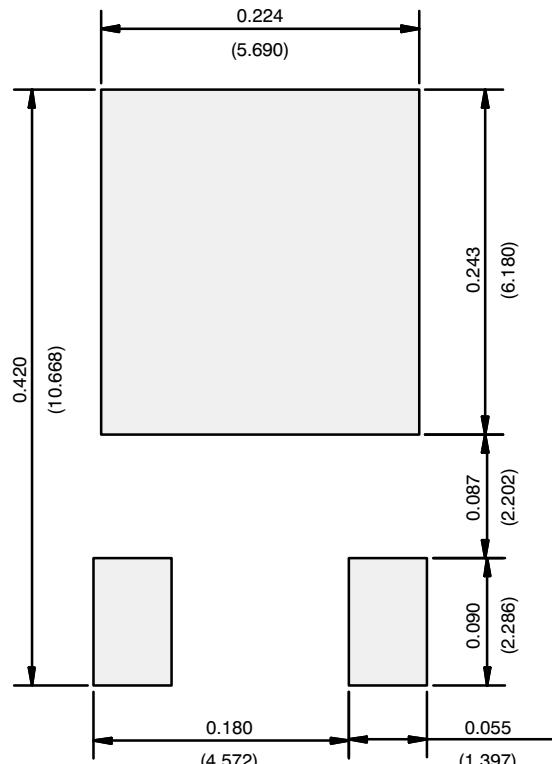
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T16-0236-Rev. P, 16-May-16  
 DWG: 5347

### Notes

- Dimension L3 is for reference only.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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