



Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSPARENT LATCHES

IDT54/74FCT373/A/C
IDT54/74FCT533/A/C
IDT54/74FCT573/A/C

FEATURES

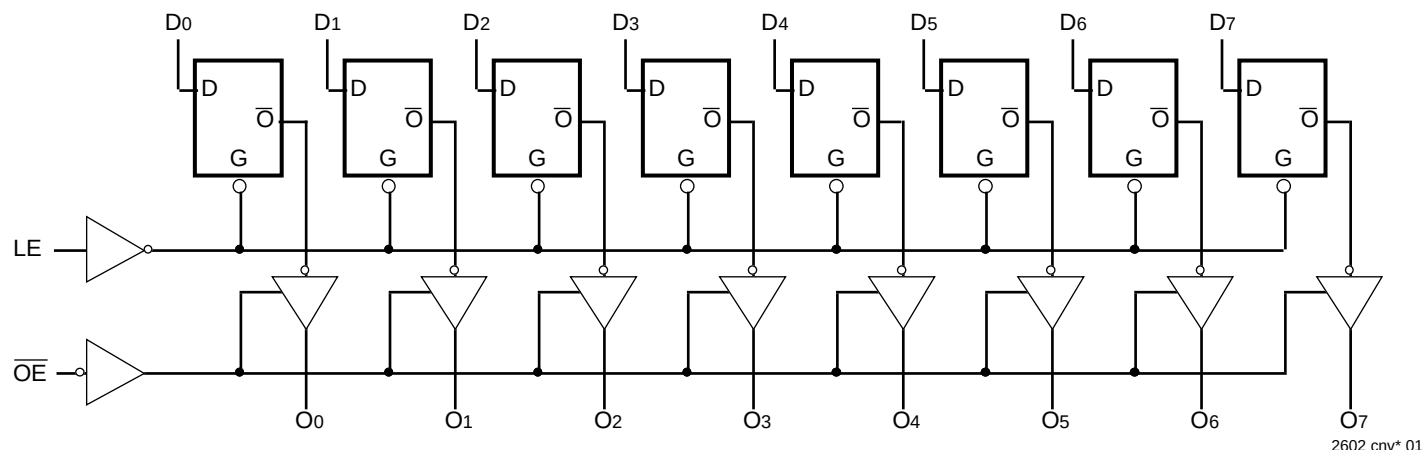
- IDT54/74FCT373/533/573 equivalent to FAST™ speed and drive
- **IDT54/74FCT373A/533A/573A up to 30% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- $I_{OL} = 48\text{mA}$ (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Octal transparent latch with 3-state output control
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

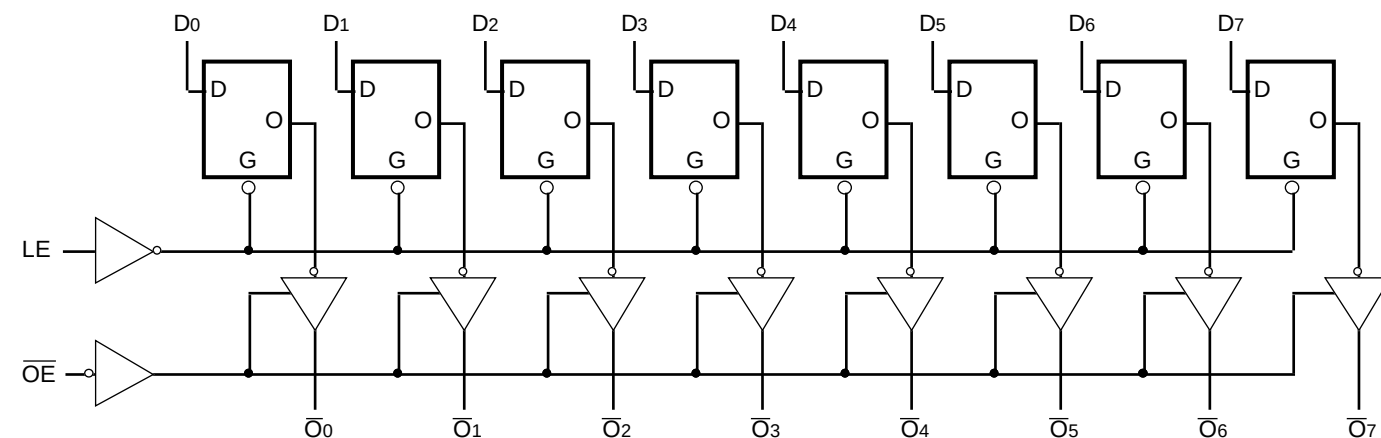
The IDT54/74FCT373/A/C, IDT54/74FCT533/A/C and IDT54/74FCT573/A/C are octal transparent latches built using an advanced dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high-impedance state.

FUNCTIONAL BLOCK DIAGRAMS

IDT54/74FCT373 AND IDT54/74FCT573



IDT54/74FCT533



The IDT logo is a registered trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

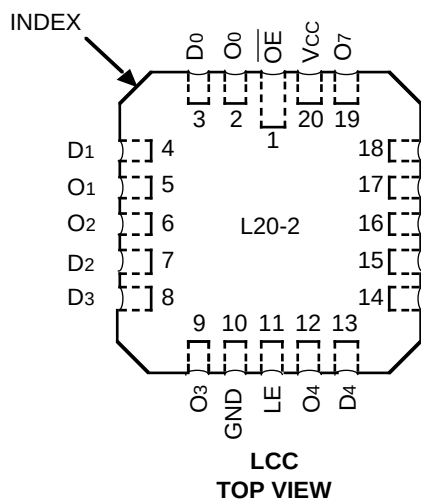
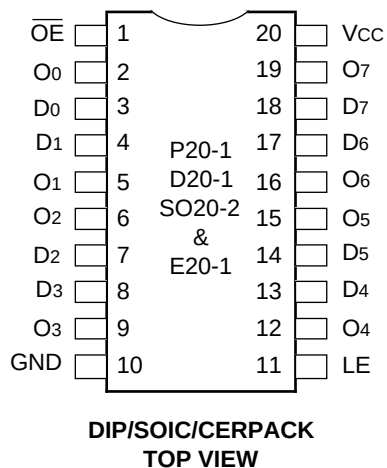
2602 cnv* 02

MILITARY AND COMMERCIAL TEMPERATURE RANGES

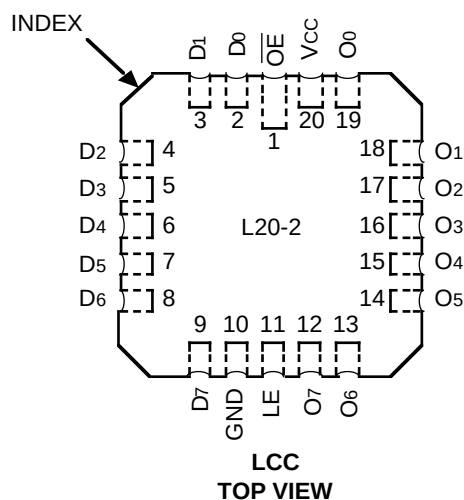
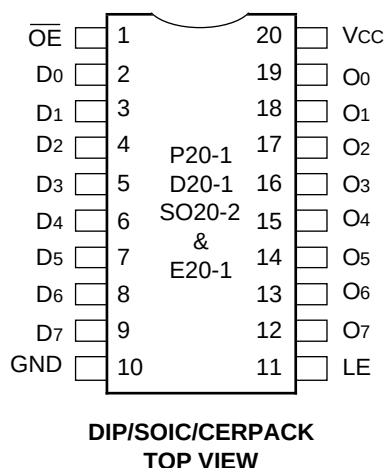
MAY 1992

PIN CONFIGURATIONS

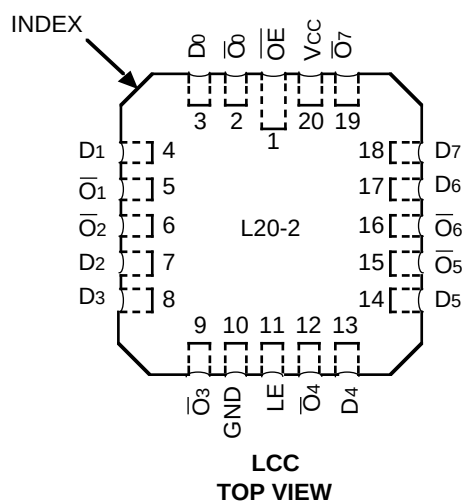
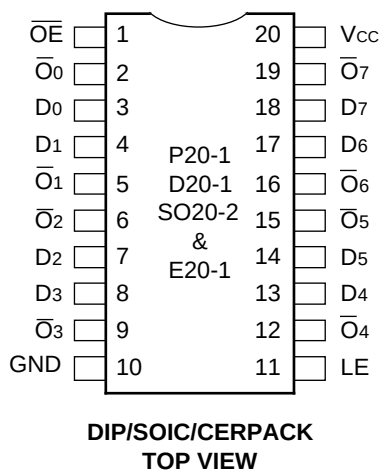
IDT54/74FCT373



IDT54/74FCT573



IDT54/74FCT533



FUNCTION TABLE (FCT533)⁽¹⁾

Inputs			Outputs
DN	LE	$\overline{OE}$	$\overline{ON}$
H	H	L	L
L	H	L	H
X	X	H	Z

NOTE:

2602 tbl 05

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

FUNCTION TABLE (FCT373 and FCT573)⁽¹⁾

Inputs			Outputs
DN	LE	$\overline{OE}$	ON
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE:

2602 tbl 06

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

PIN DESCRIPTION

Pin Names	Description
DN	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
ON	3-State Outputs
$\overline{ON}$	Complementary 3-State Outputs

2602 tbl 07

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	−0.5 to V_{CC}	−0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

2602 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	8	12	pF

NOTE:

2602 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55^\circ C$ to $+125^\circ C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	5	μA
			$V_I = 2.7V$	—	—	5 ⁽⁴⁾	
I_{IL}	Input LOW Current		$V_I = 0.5V$	—	—	-5 ⁽⁴⁾	
			$V_I = GND$	—	—	-5	
I_{OZH}	Off State (High Impedance) Output Current	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	—	10	μA
			$V_O = 2.7V$	—	—	10 ⁽⁴⁾	
I_{OZL}			$V_O = 0.5V$	—	—	-10 ⁽⁴⁾	
			$V_O = GND$	—	—	-10	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_N = -18mA$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$ ⁽³⁾ , $V_O = GND$		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V$, $V_{IN} = V_{LC}$ or V_{HC} , $I_{OH} = -32\mu A$		V_{HC}	V_{CC}	—	V
		$V_{CC} = \text{Min.}$	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}	—	
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -12mA \text{ MIL.}$	2.4	4.3	—	
			$I_{OH} = -15mA \text{ COM'L.}$	2.4	4.3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 3V$, $V_{IN} = V_{LC}$ or V_{HC} , $I_{OL} = 300\mu A$		—	GND	V_{LC}	V
		$V_{CC} = \text{Min.}$	$I_{OL} = 300\mu A$	—	GND	V_{LC} ⁽⁴⁾	
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 32mA \text{ MIL.}$	—	0.3	0.5	
			$I_{OL} = 48mA \text{ COM'L.}$	—	0.3	0.5	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

2602 tbl 03

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ $LE = V_{CC}$ One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2.0	5.0	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ $LE = V_{CC}$ Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	5.2	14.5 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

2602 tbl 04

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT373/A/C/FCT573/A/C

Symbol	Parameter	Conditions ⁽¹⁾	FCT373/573				FCT373A/573A				FCT373C/573C				Unit
			Com'l. ⁽²⁾		Mil. ⁽²⁾		Com'l. ⁽²⁾		Mil. ⁽²⁾		Com'l. ⁽²⁾		Mil. ⁽²⁾		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	1.5	4.2	1.5	5.1	ns
tPLH tPHL	Propagation Delay LE to ON		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	2.0	5.5	2.0	8.0	ns
tpZH tpZL	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
tpHZ tpLZ	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
tsu	Set-up Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

2602 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT533/A/C

Symbol	Parameter	Conditions ⁽¹⁾	FCT533				FCT533A				FCT533C				Unit
			Com'l. ⁽²⁾		Mil. ⁽²⁾		Com'l. ⁽²⁾		Mil. ⁽²⁾		Com'l. ⁽²⁾		Mil. ⁽²⁾		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay DN to $\overline{\text{ON}}$	CL = 50pF RL = 500Ω	1.5	10.0	1.5	12.0	1.5	5.2	1.5	5.6	1.5	4.7	1.5	5.1	ns
tPLH tPHL	Propagation Delay LE to $\overline{\text{ON}}$		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.8	2.0	6.9	2.0	8.0	ns
tpZH tpZL	Output Enable Time		1.5	11.0	1.5	12.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
tpHZ tPLZ	Output Disable Time		1.5	7.0	1.5	8.5	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
tsu	Set-up Time HIGH or LOW, DN to LE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, DN to LE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

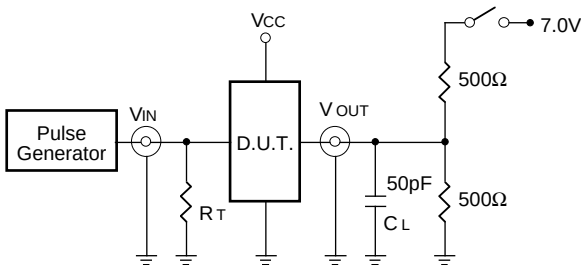
NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

2602 tbl 09

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS

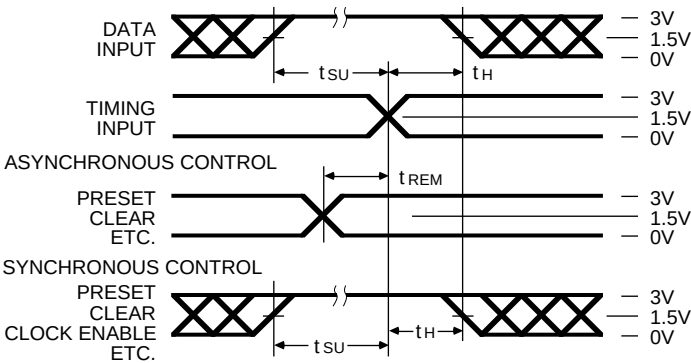


SWITCH POSITION

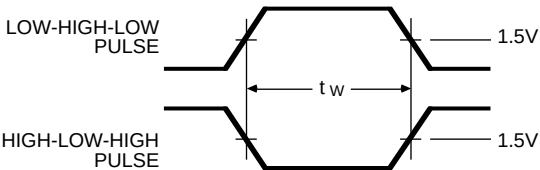
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS: 2537 tbl 10
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

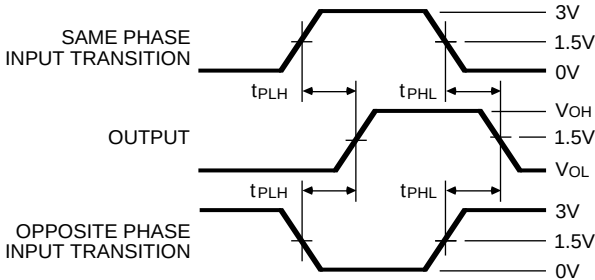
SET-UP, HOLD AND RELEASE TIMES



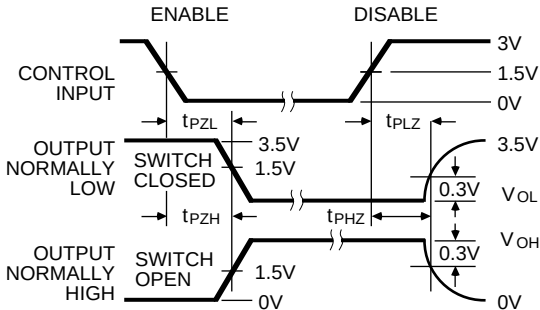
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES 2537 drw 04
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; tr ≤ 2.5ns; tr ≤ 2.5ns.

ORDERING INFORMATION

IDT	XX	FCT	XXXX	X	X		
	Temp. Range		Device Type	Package	Process		
						Blank	Commercial
						B	MIL-STD-883, Class B
						P	Plastic DIP
						D	CERDIP
						SO	Small Outline IC
						L	Leadless Chip Carrier
						E	CERPACK
						373	Non-Inverting Octal Transparent Latch
						573	Non-Inverting Octal Transparent Latch
						533	Inverting Octal Transparent Latch
						373A	Fast Non-Inverting Octal Transparent Latch
						573A	Fast Non-Inverting Octal Transparent Latch
						533A	Fast Inverting Octal Transparent Latch
						373C	Super Fast Non-Inverting Octal Transparent Latch
						573C	Super Fast Non-Inverting Octal Transparent Latch
						533C	Super Fast Inverting Octal Transparent Latch
						54	–55°C to +125°C
						74	0°C to +70°C

2602 cnv* 14