UNITRODE

application INFO available

UC1872
UC2872
UC3872

Resonant Lamp Ballast Controller

FEATURES

- Controls Different Types of Lamps: Cold Cathode Fluorescent, Neon, and Gas Discharge
- Zero Voltage Switching (ZVS) of Push-Pull Drivers
- Accurate Control of Lamp Current
- Variable Lamp Intensity Control
- 1µA Disable Current
- 4.5V to 24V Operation
- Open Lamp Detection Circuitry

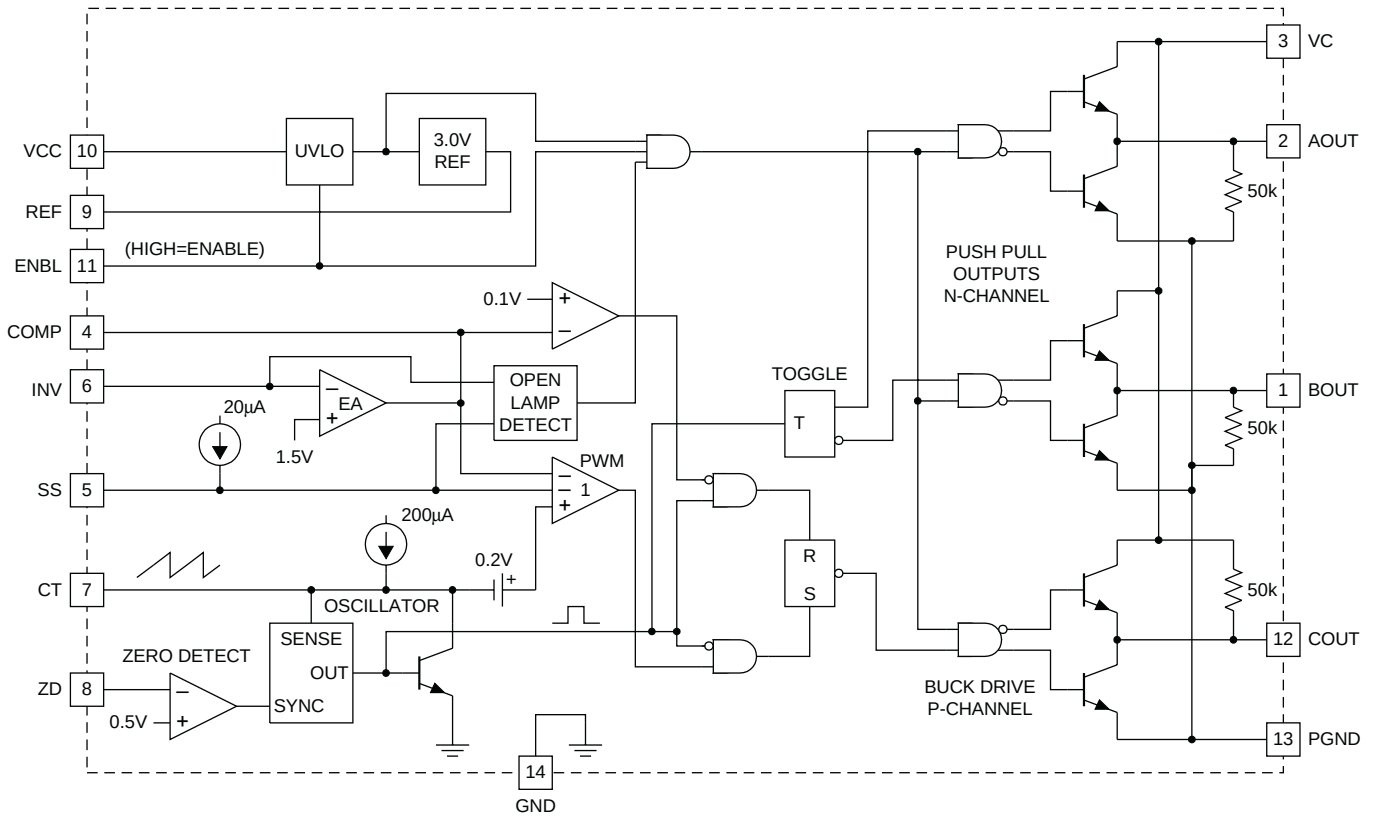
DESCRIPTION

The UC3872 is a resonant lamp ballast controller optimized for driving cold cathode fluorescent, neon, and other gas discharge lamps. The resonant power stage develops a sinusoidal lamp drive voltage, and minimizes switching loss and EMI generation. Lamp intensity adjustment is accomplished with a buck regulator, which is synchronized to the external power stage's resonant frequency. Suitable for automotive and battery powered applications, the UC3872 draws only 1µA when disabled.

Soft start and open lamp detect circuitry have been incorporated to minimize component stresses. Open lamp detection is enabled at the completion of a soft start cycle. The chip is optimized for smooth duty cycle control to 100%.

Other features include a precision 1.2% reference, undervoltage lockout, and accurate minimum and maximum frequency control.

BLOCK DIAGRAM



Note: Pin numbers shown are for DIP package.

UDG-99112

ABSOLUTE MAXIMUM RATINGS

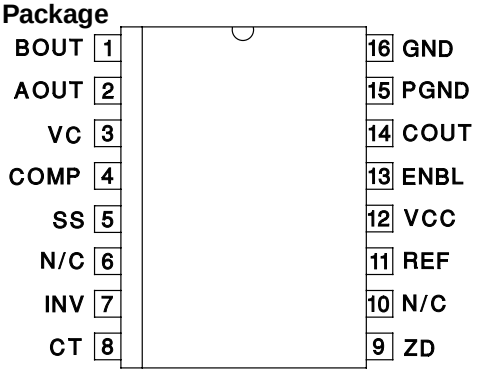
Analog Inputs . . . . . -0.3 to +10V
VCC, VC Voltage. . . . . +24V
ZD Input Current
  High Impedance Source . . . . . +10mA
ZD Input Voltage
  Low Impedance Source . . . . . +24V
Power Dissipation at T_A = 25° C 1W
Storage Temperature . . . . . -65° C to +150° C
Lead Temperature. . . . . 300° C

***Note 1**: Currents are positive into, negative out of the specified terminal.*

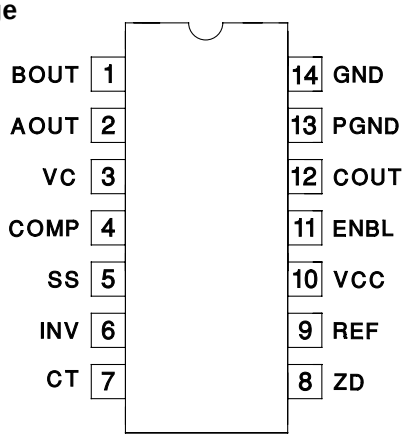
***Note 2**: Consult Packaging Section of Databook for thermal limitations and considerations of package.*

CONNECTION DIAGRAMS

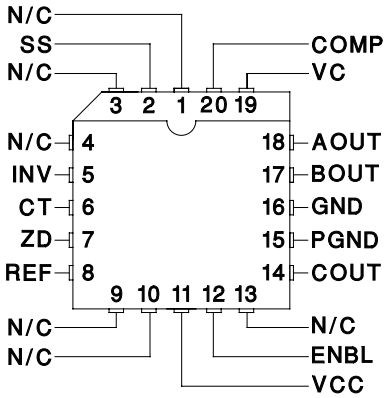
SOIC-16, SSOP-16 (TOP VIEW)
DW, M Package



DIL-14 (TOP VIEW)
N Package



PLCC-20 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_J = -55° C to +125°C for the UC1872, –40° C to +85° C for the UC2872, -0°C to +70°C for the UC3872; VCC= 5V, VC = 15V, V_{ENBL} = 5V, CT = 1nF, ZD = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_J = 25° C	2.963	3.000	3.037	V
	Over Temperature	2.940	3.000	3.060	V
Line Regulation	VCC = 4.75V to 18V			10	mV
Load Regulation	I_O = 0 to -5mA			10	mV
Oscillator Section					
Free Running Frequency	T_J = 25° C	57	68	78	kHz
Maximum Synchronization Frequency	T_J = 25° C	160	200	240	kHz
Charge Current	V_{CT} = 1.5V	180	200	220	µA
Voltage Stability				2	%
Temperature Stability			4	8	%
Zero Detect Threshold		0.46	0.5	0.56	V
Error Amp Section					
Input Voltage	V_O = 2V	1.445	1.475	1.505	V
Input Bias Current			-0.4	-2	µA
Open Loop Gain	V_O = 0.5 to 3V	65	90		dB
Output High	V_{INV} = 1.3V	3.1	3.5	3.9	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_J = –55° C to +125°C for the UC1872, –40° C to +85° C for the UC2872, 0°C to +70°C for the UC3872; VCC= 5V, VC = 15V, V_{ENBL} = 5V, CT = 1nF, ZD = 1V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amp Section (cont.)					
Output Low	V_{INV} = 1.7V		0.1	0.2	V
Output Source Current	V_{INV} = 1.3V, V_O = 2V	–350	–500		µA
Output Sink Current	V_{INV} = 1.7V, V_O = 2V	10	20		mA
Common Mode Range		0		V_{IN}-1V	V
Unity Gain Bandwidth	T_J = 25° C (Note 4)		1		MHz
Open Lamp Detect Section					
Soft Start Threshold	V_{INV} = 0V	2.9	3.4	3.8	V
Open Lamp Detect Threshold	V_{SS} = 4.2V	0.6	1.0	1.4	V
Soft Start Current	V_{SS} = 2V	10	20	40	µA
Output Section					
Output Low Level	I_{OUT} = 0, Outputs A and B		0.05	0.2	V
	I_{OUT} = 10mA		0.1	0.4	V
	I_{OUT} = 100mA		1.5	2.2	V
Output High Level	I_{OUT} = 0, Output C	13.9	14.9		V
	I_{OUT} = –10mA	13.5	14.3		V
	I_{OUT} = –100mA	12.5	13.5		V
Rise Time	T_J = 25° C, Cl = 1nF (Note 4)		30	80	ns
Fall Time	T_J = 25° C, Cl = 1nF (Note 4)		30	80	ns
Output Dynamics					
Out A and B Duty Cycle		48	49.9	50	%
Out C Max Duty Cycle	V_{INV} = 1V	100			%
Out C Min Duty Cycle	V_{INV} = 2V			0	%
Under Voltage Lockout Section					
Startup Threshold Voltage		3.7	4.2	4.5	V
Hysteresis		120	200	280	mV
Enable Section					
Input High Threshold		2			V
Input Low Threshold				0.8	V
Input Current	V_{ENBL} = 5V		150	400	µA
Supply Current Section					
VCC Supply Current	VCC = 24V		6	14	mA
VC Supply Current	VC = 24V		5	12	mA
ICC Disabled	VCC = 24V, V_{ENBL} = 0V		1	10	µA

***Note 3**: Unless otherwise specified, all voltages are with respect to ground. Currents are positive into, and negative out of the specified terminal.*

***Note 4:** Guaranteed by design. Not 100% tested in production.*

PIN DESCRIPTIONS

AOUT, BOUT: These outputs provide complementary drive signals for the push-pull N-channel MOSFETs. Each one is high for 50% of the time, switching states each time a zero-detect is sensed.

COMP: COMP is the output terminal of the error amplifier. Compensation components are normally connected between COMP and INV. Connecting a capacitor from this pin to ground limits turn on current and blanks the open lamp detect signal allowing the lamp to start.

COUT: This output directly drives the bulk regulator P-channel MOSFET. COUT turn-on is synchronized to each zero-detect, and therefore switches at twice the frequency of AOUT and BOUT. The modulator controlling COUT is designed to provide smooth control up to 100% duty cycle.

CT: A capacitor connected between this pin and GND ground sets the synchronization frequency range. The capacitor is charged with approximately 200μA, creating a linear ramp which is used by COUT's (buck regulator driver) PWM comparator.

ENBL: When ENBL is driven high the device is enabled. When ENBL is pulled low, the IC is shut down and typically draws 1μA.

GND: This pin is the ground reference point for the internal reference and all thresholds.

INV: This pin is the inverting input to the error amplifier and the input for the open lamp detect circuitry. If the voltage at INV is below the 1V open lamp detect threshold, the outputs are disabled.

PGND: This pin is the high current ground connection for the three output drivers.

REF: This pin is connected to the 3V reference voltage which is used for the internal logic. Bypass REF to ground with a 0.01μF ceramic capacitor for proper operation.

VC: VC is the power supply voltage connection for the output drivers. Bypass it to ground with a 0.1μF ceramic capacitor for proper operation.

VCC: VCC is the positive supply voltage for the chip. Its operating range is from 4.2V to 24V. Bypass VCC to ground with a 0.1μF ceramic capacitor for proper operation.

ZD: The zero-detect input senses when the transformer's primary center tap voltage falls to zero to synchronize the sawtooth voltage waveform on CT. The threshold is approximately 0.5V, providing a small amount of offset such that with propagation delay, zero-volt switching occurs. A resistor (typically 10k) should be connected between ZD and the primary center tap to limit input current at turn off.

APPLICATION INFORMATION

Figure 1 shows a complete application circuit using the UC3872 Resonant Lamp Ballast Controller. The IC provides all drive, control and housekeeping functions. The buck output voltage (transformer center-tap) provides the zero crossing and synchronization signals.

The buck modulator drives a P-channel MOSFET directly, and operates over a 0-100% duty-cycle range. The modulation range includes 100%, allowing operation with minimal headroom.

The oscillator and synchronization circuitry are shown in Figure 2. The oscillator is designed to synchronize over a 3:1 frequency range. In an actual application however, the frequency range is only about 1.5:1. A zero detect comparator senses the primary center-tap voltage, generating a synchronization pulse when the resonant waveform falls to zero. The actual threshold is 0.5 volts, providing a small amount of anticipation to offset propagation delay.

The synchronization pulse width is the time required for the 4mA current sink to discharge the timing capacitor to 0.1 volts. This pulse width limits the minimum linear control range of the buck regulator. The 200μA current source charges the capacitor to a maximum of 3 volts. A comparator blanks the zero detect signal until the capacitor voltage exceeds 1 volt, preventing multiple synchronization pulse generation and setting the maximum frequency. If the capacitor voltage reaches 3 volts (a zero detection has not occurred) an internal clock pulse is generated to limit the minimum frequency.

APPLICATION INFORMATION (cont.)

A unique protection feature incorporated in the UC3872 is the Open Lamp Detect circuit. An open lamp interrupts the current feedback loop and causes very high secondary voltage. Operation in this mode will usually breakdown the transformer's insulation, causing permanent damage to the converter. The open lamp detect circuit, shown in Figure 3 senses the lamp current feedback signal at the error amplifier's input, and shuts down the outputs if insufficient signal is present. Soft start circuitry limits initial turn-on currents and blanks the open lamp detect signal.

Other features are included to minimize external circuitry requirements. A logic level enable pin shuts down the IC, allowing direct connection to a battery. During shutdown, the IC typically draws less than 1µA. The UC3872, operating from 4.5V to 24V, is compatible with almost all battery voltages used in portable computers and automotive applications. Undervoltage lockout circuitry disables operation until sufficient supply voltage is available, and a 1% voltage reference insures accurate operation.

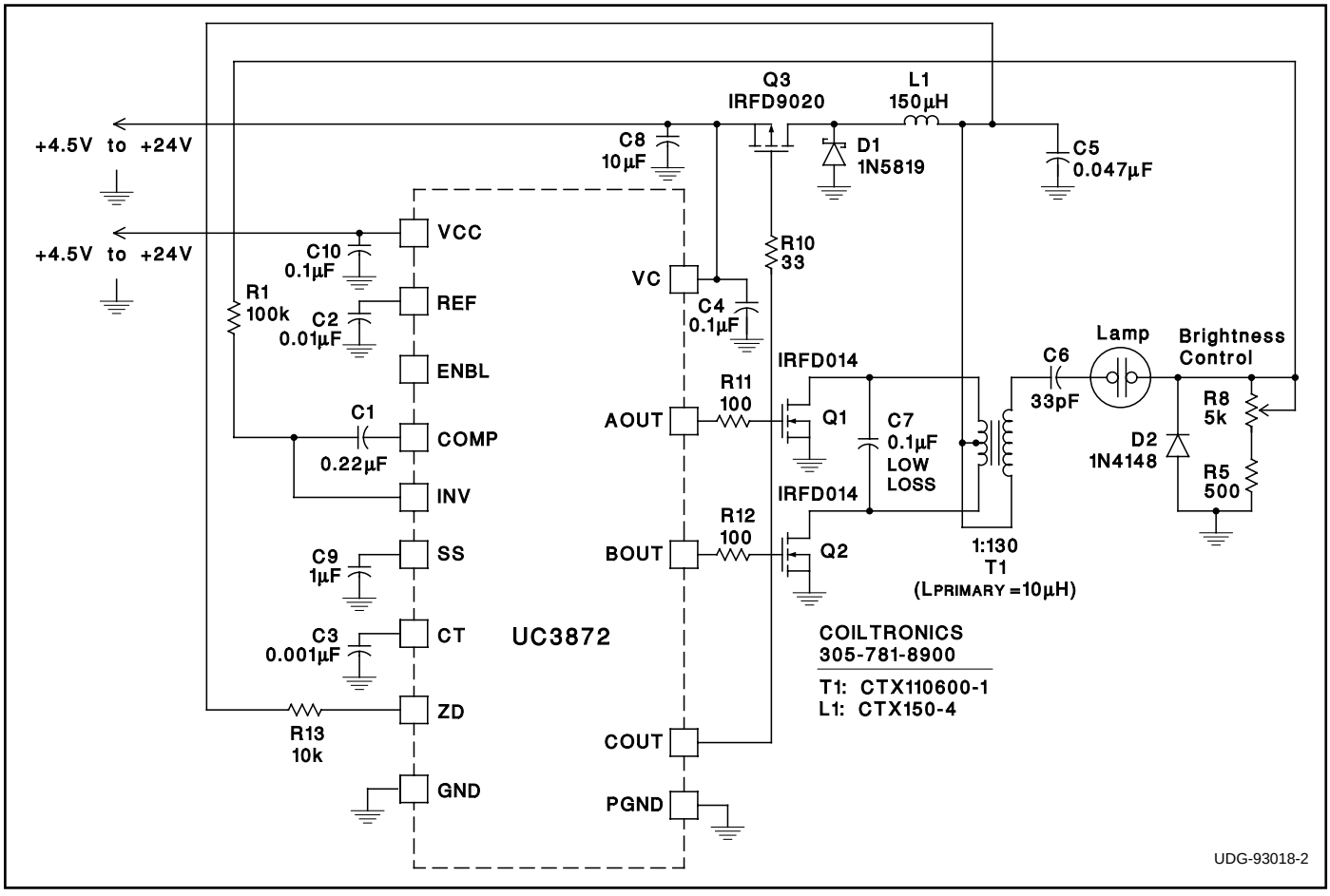


Figure 1. Typical application.

APPLICATIONS INFORMATION

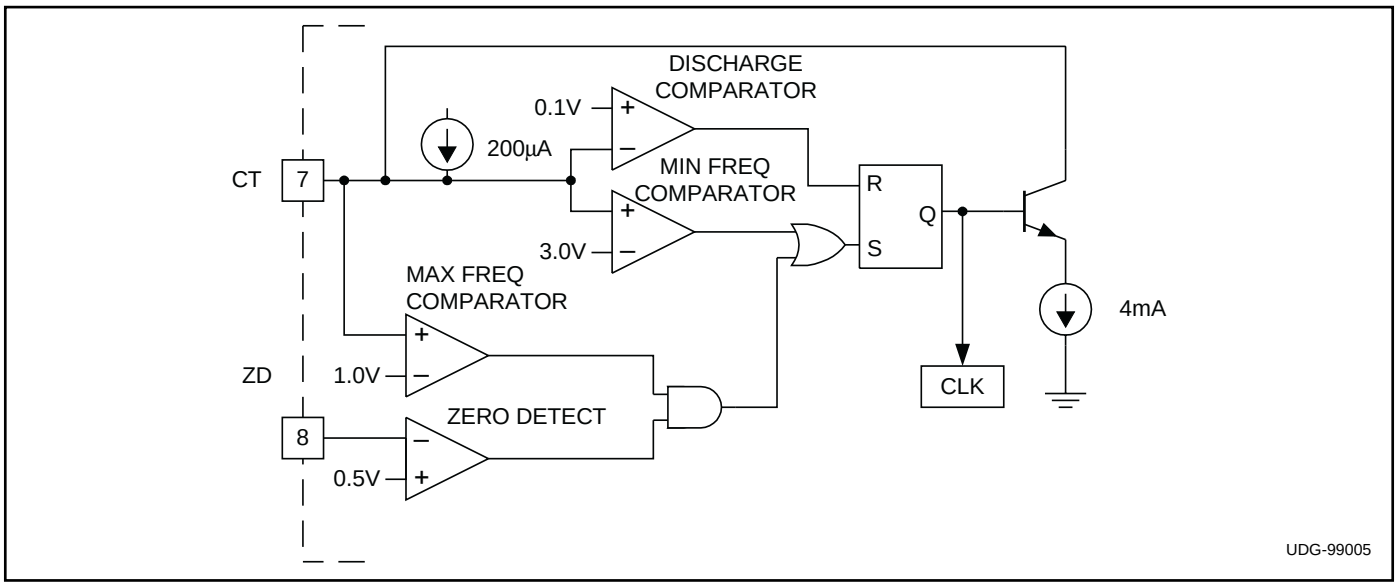


Figure 2. UC3872 oscillator section.

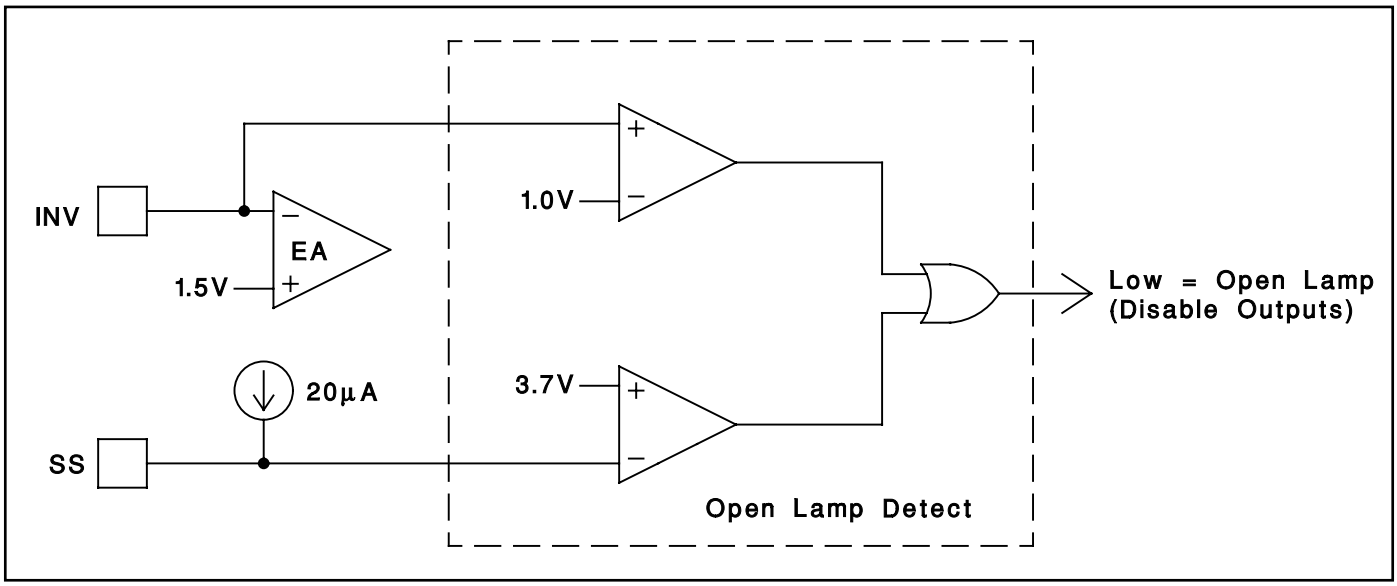


Figure 3. UC3872 open lamp detect circuitry.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC2872DW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2872DW
UC2872DW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2872DW
UC2872DWTR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2872DW
UC2872DWTR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2872DW
UC3872DW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3872DW
UC3872DW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3872DW
UC3872DWTR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3872DW
UC3872DWTR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3872DW
UC3872M	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3872M
UC3872M.A	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3872M
UC3872MG4	Active	Production	SSOP (DBQ) | 16	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3872M
UC3872MTR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3872M
UC3872MTR.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3872M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

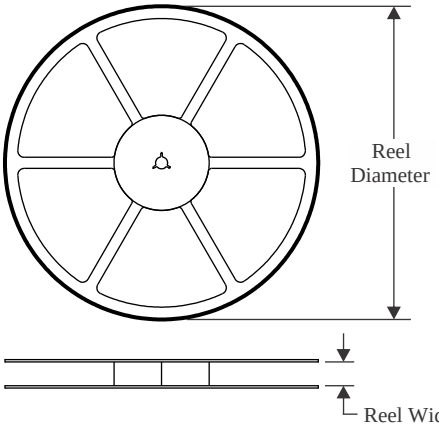
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

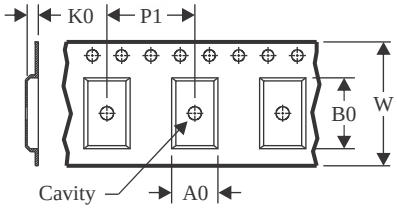
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

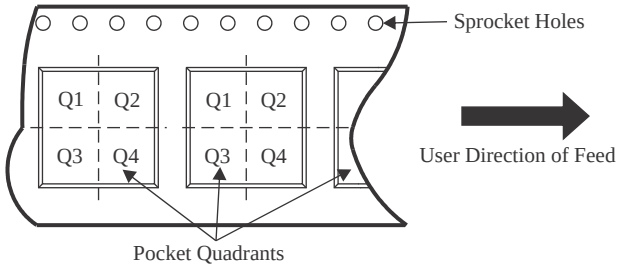


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

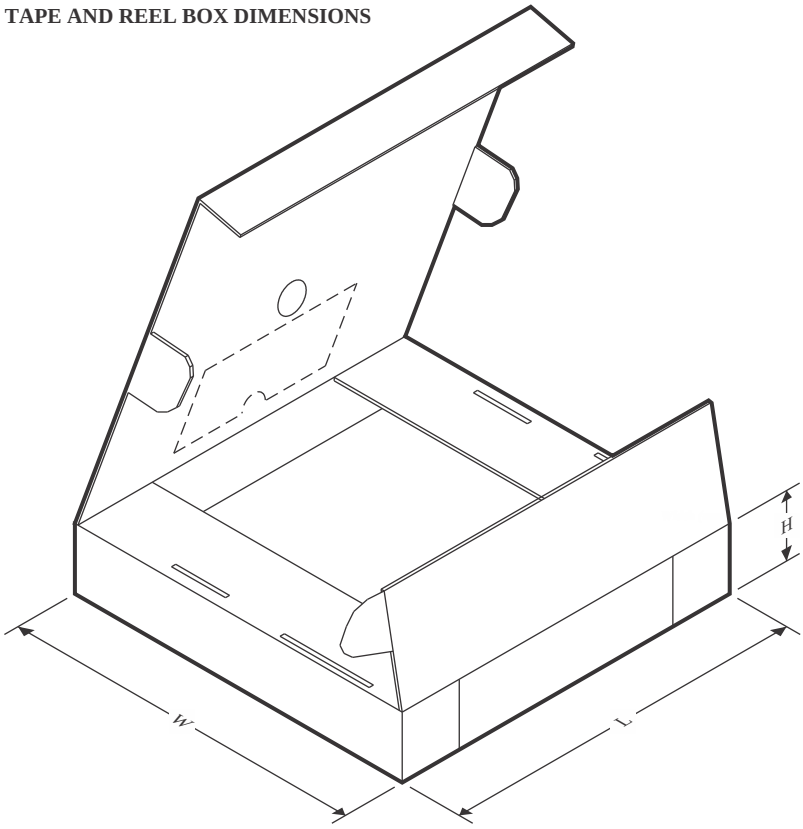
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2872DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3872DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3872MTR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

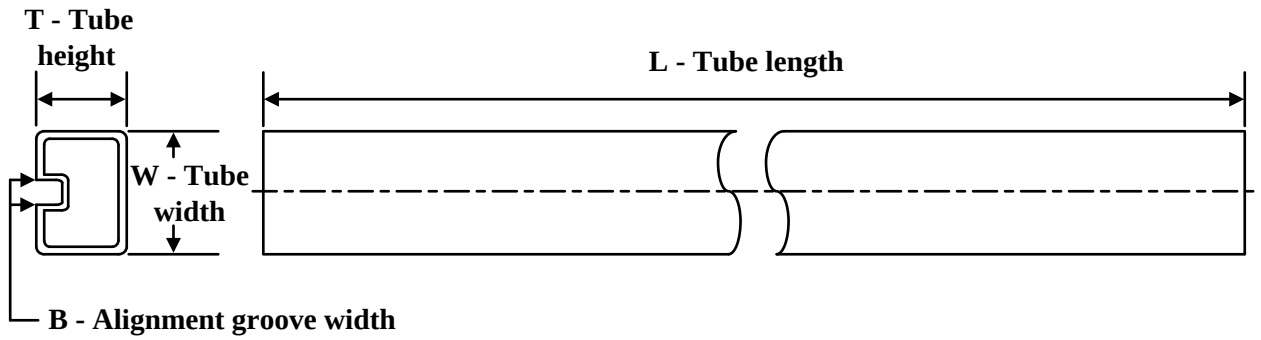
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2872DWTR	SOIC	DW	16	2000	367.0	367.0	38.0
UC3872DWTR	SOIC	DW	16	2000	356.0	356.0	35.0
UC3872MTR	SSOP	DBQ	16	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC2872DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2872DW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC3872DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3872DW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC3872M	DBQ	SSOP	16	75	506.6	8	3940	4.32
UC3872M.A	DBQ	SSOP	16	75	506.6	8	3940	4.32
UC3872MG4	DBQ	SSOP	16	75	506.6	8	3940	4.32

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