TPS25864-Q1 和 TPS25865-Q1 具有热管理和电缆补偿功能的低 EMI 双 USB Type-A 充电端口转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：T_A 范围 –40°C 至 +125°C
  - HBM ESD 分类等级 H2
  - CDM ESD 分类等级 C5
- 针对超低 EMI 要求进行了优化：
  - 符合 CISPR25 5 类标准
  - HotRod™ 封装可更大限度地减少开关节点振铃
  - 展频可降低峰值发射
- 同步降压稳压器
  - 400kHz 下的高效率：V_{IN} = 13.5V、I_{PA_BUS} = 2.4A 且 I_{PB_BUS} = 2.4A 时效率为 95.2%
  - 18mΩ/10mΩ 低 $R_{DS(ON)}$ 降压稳压器 MOSFET
  - 工作电压范围：5.5V 至 26V，可承受 36V 输入
  - 频率可调节：200kHz 至 800kHz (TPS25865-Q1)
  - 频率可调节：200kHz 至 3MHz (TPS25864-Q1)
  - 具有展频频谱抖动的 FPWM
  - 可选输出电压：5.1V、5.17V、5.3V、5.4V
- 内部电源路径：
  - 7mΩ/7mΩ 低 $R_{DS(ON)}$ 内部 USB 功率 MOSFET
  - 具有高精度的 USB 端口的电流限制： 2.73A 下为 ±10%
  - OUT：用于辅助负载的 5.1V、200mA 电源
- 线路压降补偿：2.4A 负载下为 90mV
- 符合 USB-IF 标准
  - 自动 DCP 模式：
    - 符合 BC1.2 和 YD/T 1591 2009 要求的短路模式
    - 1.2V 模式
    - 2.7V 分压器 3 模式
- 甩负荷和可编程 T_A
- 器件 T_J 范围：–40°C 至 +150°C

2 应用

- 汽车 USB 充电端口
- 汽车 USB 媒体中心

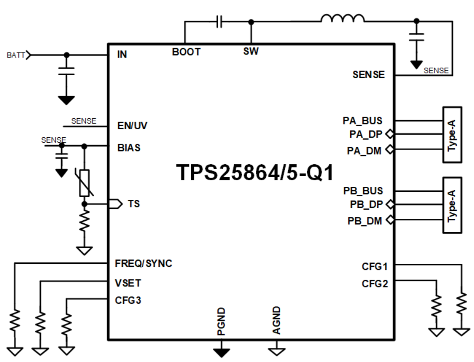
3 说明

TPS2586x-Q1 是一款集成式 USB 充电端口解决方案，其中包括一个同步高效直流/直流转换器，而且它还集成了检测和控制功能，用于在双 Type-A 端口上实施 USB 电池充电规范 1.2。

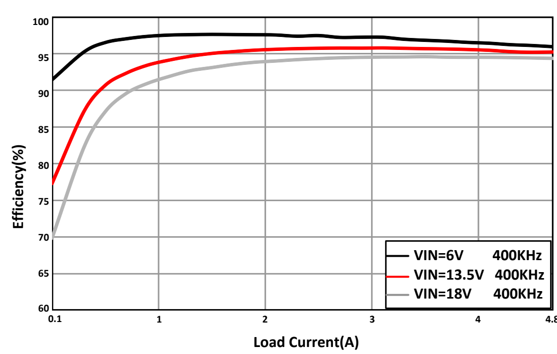
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS25865-Q1	VQFN-HR (25)	3.50mm × 4.50mm
TPS25864-Q1	VQFN-HR (25)	3.50mm × 4.50mm

(1) 如需了解所有不同可用选件的详细器件型号，请参阅数据表末尾的可订购产品附录。



简化版原理图 TPS25864-Q1、TPS25865-Q1



效率与输出电流间的关系

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (March 2021) to Revision B (September 2021)	Page
• 添加了 TPS25864-Q1 信息	1

Changes from Revision * (November 2020) to Revision A (March 2021)	Page
• 向*特性* 部分添加了 EMI 要求要点	1
• 已更新文档标题	1
• Added 图 11-3 to the *Application Curves* section	35

5 说明（续）

TPS2586x-Q1 是一款用于双 USB 端口应用的高度集成的 USB Type-A 充电控制器。

TPS2586x-Q1 集成了一个具有内部功率 MOSFET 的单片、同步、整流、降压开关模式转换器和两个具有充电端口自动检测功能的 USB 限流开关。TPS2586x-Q1 提供了一种紧凑型解决方案，可在宽输入电源电压范围内实现出色的负载和线路调节。该同步降压稳压器具有峰值电流模式控制，而且采用了内部补偿，可简化设计。对于 TPS25865-Q1，FREQ 引脚上有一个电阻器，可用于在 200kHz 和 800kHz 之间设置开关频率。对于 TPS25864-Q1，FREQ 引脚上有一个电阻器，可用于在 200kHz 和 3MHz 之间设置开关频率。在低于 400kHz 的频率下运行可实现更高的系统效率，在高于 2.1MHz 的频率下运行则可以避开 AM 无线电频带，并且能够使用较小的电感器。

TPS2586x-Q1 集成了标准电池充电（1.2 版），可提供 Type-A USB 器件（利用 USB 数据线信号来确定 USB 端口的拉电流能力）所需的电气特性。TPS2586X-Q1 还集成了一个 OUT 电源开关，可为辅助负载提供最大 200mA 的电流。由于系统集成度高且占用空间小，该器件特别适用于双端口应用。由于系统集成度高且占用空间小，该器件特别适用于双端口应用。

TPS2586x-Q1 支持智能热管理。USB 输出电压可以根据温度检测通过 TS 引脚进行调节。TPS2586x-Q1 必须在 TS 引脚上连接一个 NTC 热敏电阻以监控环境温度或 PCB 板温度，具体取决于 NTC 热敏电阻在 USB 充电模块或 PCB 板中的放置位置。选择不同的 NTC 热敏电阻和底部串联电阻可以改变用负荷的温度阈值。

TPS2586x-Q1 具有四种可选的 USB 输出电压设置：5.1V、5.17V、5.3V 和 5.4V。TPS2586x-Q1 集成了一个精密电流检测放大器，用于实现电缆压降补偿和 USB 端口电流限制。电缆补偿仅在输出电压设置为 5.17V 时可用。电缆补偿电压在 2.4A 输出电流时为 90mV。电缆补偿可使降压稳压器输出电压随负载电流线性改变，以抵消由于汽车电缆布线中的导线电阻引起的压降，从而帮助便携式设备在重载下实现最佳电流和电压充电。无论负载电流如何，在连接的便携式器件上测得的总线电压都保持大致恒定，这样，便携式器件的电池充电器就能够保持理想工作状态。

TPS2586x-Q1 针对 USB 充电和系统运行提供多种安全特性，包括外部负热敏电阻监控、逐周期电流限制、断续短路保护、欠压锁定、BUS 过流、OUT 过流以及裸片过热保护。

该器件系列可提供 25 引脚 3.5mm × 4.5mm QFN 封装。

6 Device Comparison Table

DEVICE NUMBER	TPS25864-Q1	TPS25865-Q1
Type-A ports number	Dual	Dual
NTC Thermistor Input (TS)	Yes	Yes
DC/DC converter switching frequency range	200 kHz to approximately 3 MHz	200 kHz to approximately 800 kHz
BC1.2 DCP	Yes	Yes
Apple or Samsung charging scheme	Yes	Yes
Cable compensation	Yes	Yes(1)
Selectable output voltage	Yes	Yes
External clock synchronization	Yes, range 200 kHz to approximately 3 MHz	Yes, range 200 kHz to approximately 800 kHz
Adjustable output short current limit	Yes	Yes
FPWM/PFM	FPWM	FPWM
DCDC always ON (EN pull High)	Yes	No
Spread spectrum	Yes	Yes
Package	QFN-25 3.5 mm × 4.5 mm	QFN-25 3.5 mm × 4.5 mm

(1) VSET short to GND to set 5.17-V output voltage. Compensation voltage is 90 mV when either USB port A or USB port B output 2.4-A current.

7 Pin Configuration and Functions

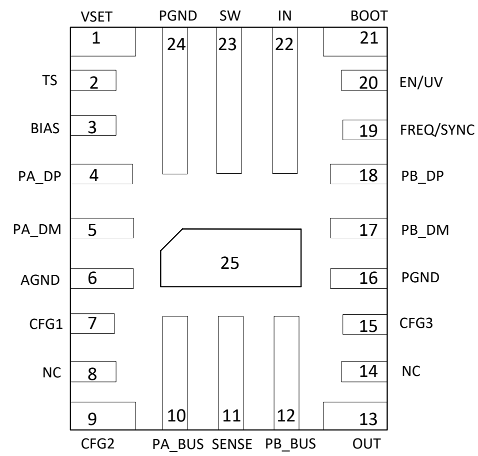


图 7-1. TPS2586x-Q1 RPQ Package 25-Pin (QFN) Top View

表 7-1. Pin Functions for TPS2586x-Q1 RPQ Package

PIN		TYPE [(1)]	DESCRIPTION
NAME	NO.		
VSET	1	A	Output Voltage Setting. Short to GND to set the 5.17-V output voltage. Float or pull up to V_{SENSE} to set 5.1-V output voltage. Tie to GND through a 40.2-KΩ resistor to set 5.3-V output voltage. Tie to GND through a 80.6-KΩ resistor to set 5.4-V output voltage.
TS	2	A	Temperature Sense terminal. Connect the TS input to the NTC thermistor.
BIAS	3	P	Input of internal bias supply. Must connect to the SENSE pin directly. Power the internal circuit.
PA_DP	4	A	D+ data line. Connect to USB Port A connector.
PA_DM	5	A	D- data line. Connect to USB Port A connector.
AGND	6	P	Analog ground terminal. Connect AGND to PGND.
CFG1	7	A	Configuration pin. For internal circuit, must connect a 5.1-KΩ resistor to AGND.
NC	8, 14	A	Makes no electrical connection.
CFG2	9	A	Configuration pin. For internal circuit, must connect a 11.8-KΩ resistor to AGND.
PA_BUS	10	P	Port A BUS output.
SENSE	11	P	Output Voltage Sensing. External load on this pin is strictly prohibited. Connect to the other side of the external inductor.
PB_BUS	12	P	Port B BUS output.
OUT	13	P	Output pin. Provide 5.1-V voltage to power external load with maximum 200-mA capability. The voltage follows the VSET setting.
CFG3	15	A	Configuration pin. For internal circuit, must connect a 5.1-KΩ resistor to AGND.
PGND	16, 24, 25	P	Power Ground terminal. Connected to the source of LS FET internally. Connect to system ground, AGND, and the ground side of the C_{IN} and C_{OUT} capacitors. The path to C_{IN} must be as short as possible.
PB_DM	17	A	D- data line. Connect to USB port B connector.
PB_DP	18	A	D+ data line. Connect to USB port B connector.
FREQ/ SYNC	19	A	Switching Frequency Program and External Clock Input. Connect a resistor from FREQ to GND to set the switching frequency.
EN/UV	20	A	Enable pin. Precision enable controls the regulator switching action. Do not float. High = on, Low = off. Can be tied to SENSE directly. Precision enable input allows adjustable UVLO by external resistor divider if tie to IN pin.

表 7-1. Pin Functions for TPS2586x-Q1 RPQ Package (continued)

PIN		TYPE [(1)]	DESCRIPTION
NAME	NO.		
BOOT	21	P	Bootstrap capacitor connection. Internally, the BOOT is connected to the cathode of the boost-strap diode. Connect the 0.1-μF bootstrap capacitor from SW to BOOT.
IN	22	P	Input power. Connected to external DC supply. Expected range of bypass capacitors is 1 μF to 10 μF, connect from IN to PGND. Can withstand up to 36 V without damage but operating is suspended if VIN is above the 26-V OVP threshold.
SW	23	P	Switching output of the regulator. Internally connected to source of the HS FET and drain of the LS FET. Connect to output inductor.

(1) A = Analog, P = Power, G = Ground.

8 Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40°C to +150°C and AGND = PGND (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Input voltage	IN to PGND	–0.3	40(2)	V
	IN to SW	–0.3	35	
	BIAS, SENSE to PGND	–0.3	6	
	EN to AGND	–0.3	11	
	FREQ/SYNC to AGND	–0.3	6	
	VSET to AGND	-0.3	6	
	AGND to PGND	–0.3	0.3	
Output voltage	SW to PGND	–0.3	35	V
	SW to PGND (less than 10 ns transients)	–3.5	35	
	BOOT to SW	–0.3	6	
	PA_BUS, PB_BUS, OUT to PGND	–0.3	6	
Voltage range	CFG1, CFG2, CFG3 to AGND	–0.3	6	V
	DP, DM to AGND	–0.3	6	
Voltage range	TS to AGND	–0.3	6	V
I/O current	DP to DM in BC1.2 DCP Mode	–35	35	mA
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) VIN rising slew rate below 2*0V/ms* if in 0-V to 40-V transient, room temperature, maximum 500-uF cap at SENSE.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000(2)	V
		Charged device model (CDM), per AEC Q100-011	Corner pins	±750(3)	
			Other pins	±750(3)	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The passing level per AEC-Q100 Classification H2.
(3) The passing level per AEC-Q100 Classification C5

8.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of -40°C to 150°C. Voltages are with respect to GND (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Input voltage	IN to PGND	5.5		26	V
		EN	0		VSENSE	
		TS	0		VSENSE	
		FREQ/SYNC when driven by external clock	0		3.3	
V_O	Output voltage	PA_BUS, PB_BUS, OUT	5		5.5	V
I_O	Output current	PA_BUS, PB_BUS	0		2.4	A
		OUT	0		0.2	A
		DP to DM Continuous current in BC1.2 DCP Mode	–15		15	mA
R_{EXT}	External resistnace	R_{VSET}	0		100	kΩ
		R_{FREQ}	0		100	kΩ
C_{EXT}	External capacitance	C_{BOOT}		0.1		uF
T_J		Operating junction temperature	–40		150	°C

8.4 Thermal Information

THERMAL METRIC[(1)] [(2)]		TPS2586x-Q1 RPQ (VQFN) 25 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	20.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Power rating at a specific ambient temperature T_A should be determined with a maximum junction temperature of 150 °C.

8.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} = 400 kHz, VSET short to GND unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (IN PIN)						
I_{SD}	Shutdown quiescent current; measured at IN pin.	VEN/UV = 0, -40℃ ≤ T_J ≤ 85℃		34	63	uA
I_Q	Operating quiescent current (DCDC disable)	V_{EN} = V_{SENSE}, CFG1&CFG3 = open, -40℃ ≤ T_J ≤ 85℃			200	µA
V_{OVLO_R}	Voltage on VIN pin when buck regulator stops switching		26.6	27.5	28.4	V
V_{OVLO_HYS}	Hysteresis			0.5		V
ENABLE AND UVLO (EN/UVLO PIN)						
$V_{EN/UVLO\_R}$	Rising threshold for not in External UVLO	$V_{EN/UV}$ rising threshold	1.26	1.3	1.34	V
$V_{EN/UVLO\_HYS}$	Hysteresis	$V_{EN/UVLO}$ falling		100		mV
BOOTSTRAP						
V_{BTST_UVLO}	Bootstrap voltage UVLO threshold			2.2		V
R_{BOOT}	Bootstrap pull-up resistence	VSENSE - BOOT = 0.1 V		7.7		Ω
BUCK REGULATOR						
$I_{L\text{-}SC\text{-}HS}$	High-side current limit	BOOT - SW = 5 V	10.2	11.4	12.6	A
$I_{L\text{-}SC\text{-}LS}$	Low-side current limit	SENSE = 5 V	8.5	10	11.5	A
$I_{L\text{-}NEG\text{-}LS}$	Low-side negative current limit	SENSE = 5 V	-7	-5	-3	A
I_{ZC}	Zero current detector threshold			0.01		A
V_{SENSE}	BUCK Output voltage	CFG1 or CFG3 pulldown resistance = 5.1KΩ, VSET float or pull up to V_{SENSE}, T_J = 25℃	-1%	5.1	+1%	V
		CFG1 or CFG3 pulldown resistance = 5.1KΩ, VSET short to AGND, T_J = 25℃	-1%	5.17	+1%	V
		CFG1 or CFG3 pulldown resistance = 5.1KΩ, R_{VSET} = 40.2KΩ, T_J = 25℃	-1%	5.3	+1%	V
		CFG1 or CFG3 pulldown resistance = 5.1KΩ, R_{VSET} = 80.6KΩ, T_J = 25℃	-1%	5.4	+1%	V

8.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} = 400 kHz, VSET short to GND unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SENSE}	BUCK Output voltage accuracy	CFG1 or CFG3 pulldown resistance = R_d, -40℃ ≤ T_J ≤ 150℃	–2		2	%
$V_{DCDC\_UVLO\_R}$	SENSE input level to enable DCDC switching	V_{SENSE} rising, CFG1 or CFG3 pull down resistance = 5.1KΩ	3.85	4	4.15	V
$V_{DCDC\_UVLO\_HYS}$	Hysteresis	V_{SENSE} falling, CFG1 or CFG3 pull down resistance = 5.1KΩ		0.4		V
V_{DROP}	Dropout voltage (V_{IN}-V_{SENSE})	V_{IN} = V_{SENSE} + $V_{DROP,}$ V_{SENS} = 5.1 V, I_{PA_BUS} = 2.4A, I_{PB_BUS} = 2.4A		300		mV
$R_{DS\text{-}ON\text{-}HS}$	High-side MOSFET ON-resistance	I_{PA_BUS} = 2.4 A, I_{PB_BUS} = 2.4 A, BOOT - SW = 5 V, -40℃≤ T_J ≤ 150℃		18	34	mΩ
$R_{DS\text{-}ON\text{-}LS}$	Low-side MOSFET ON-resistance	I_{PA_BUS} = 2.4 A, I_{PB_BUS} = 2.4 A, V_{SENSE} = 5 V, -40℃ ≤ T_J ≤150℃		9.5	18.5	mΩ
POWER SWITCH AND CURRENT LIMIT						
$R_{DS\text{-}ON\_USB}$	USB Load Switch MOSFET ON-resistance	I_{PA_BUS} = 2.4 A, I_{PB_BUS} = 2.4 A; -40℃ ≤ T_J ≤ 150℃		6.8	11.73	mΩ
$R_{DS\text{-}ON\_OUT}$	OUT Load Switch MOSFET ON-resistance	I_{OUT} = 0.3 A		230		mΩ
$V_{USBLS\_UVLO\_R}$	Voltage on SENSE pin that will enable the USB Load Switch		3.95	4.1	4.25	V
$V_{USBLS\_UVLO\_HYS}$	Hysteresis			200		mV
I_{OS_HI}	BUS output short-circuit secondary current limit		3938	4376	4814	mA
		T_J = 25℃	4157	4376	4595	mA
I_{OS_BUS}	BUS output short-circuit current limit		2461	2735	3009	mA
		T_J = 25℃	2598	2735	2872	mA
I_{OS_OUT}	OUT output short-circuit current limit	Short circuit current limit	390	450	495	mA
CABLE COMPENSATION VOLTAGE						
V_{DROP_COM}	Cable compensation voltage	I_{PA_BUS} or I_{PB_BUS} = 2.4A, VSET= GND (set 5.17V output)	70	90	110	mV
BC 1.2 DOWNSTREAM CHARGING PORT						
R_{DPM_SHORT}	DP and DM shorting resistance			70	200	Ω
DIVIDER 3 MODE						
V_{DP_DIV3}	DP output voltage		2.57	2.7	2.84	V
V_{DM_DIV3}	DM output voltage		2.57	2.7	2.84	V
R_{DP_DIV3}	DP output impedance	I_{DP_IN} = –5 µA	24	30	36	kΩ
R_{DM_DIV3}	DM output impedance	I_{DM_IN} = –5 µA	24	30	36	kΩ
1.2-V MODE						
$V_{DP\_1.2V}$	DP output voltage		1.12	1.2	1.26	V
$V_{DM\_1.2V}$	DM output voltage		1.12	1.2	1.26	V
$R_{DP\_1.2V}$	DP output impedance	I_{DP_IN} = –5 µA	84	100	126	kΩ
$R_{DM\_1.2V}$	DM output impedance	I_{DM_IN} = –5 µA	84	100	126	kΩ
FREQ/SYNC THRESHOLD						
$V_{IH\_FREQ/SYNC}$	FREQ/SYNC high threshold for external clock synchronization	Amplitude of SYNC clock AC signal (measured at FREQ/SYNC pin)	2			V
$V_{IL\_FREQ/SYNC}$	FREQ/SYNC low threshold for external clock synchronization	Amplitude of SYNC clock AC signal (measured at FREQ/SYNC pin)			0.8	V

8.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} = 400 kHz, VSET short to GND unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE SENSING						
V_{WARN_HIGH}	Temperature warning threshold rising	As percentage to V_{SENSE}	0.475	0.5	0.525	V/V
V_{WARN_HYS}	Hysteresis	As percentage to V_{SENSE}		0.1		V/V
V_{HOT_HIGH}	Temperature Hot assert threshold rising to reduce SENS voltage	As percentage to V_{SENSE}	0.618	0.65	0.683	V/V
V_{HOT_HYS}	Hysteresis	As percentage to V_{SENSE}		0.1		V/V
V_{R_VSENS}	V_{SENSE} voltage decay when Temperature Hot assert	TS pin voltage rise above 0.65 * V_{SENSE}		4.77		V
THERMAL SHUTDOWN						
T_{LS_SD}	USB Load Switch Over Temperature	Shutdown threshold		160		°C
		Recovery threshold		150		°C
T_{SD}	Thermal shutdown	Shutdown threshold		166		°C
		Recovery threshold		154		°C

8.6 Timing Requirements

Over the recommended operating junction temperature range of -40 °C to 150 °C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
BUS DISCHARGE						
POWER SWITCH TIMING						
$t_{IOS\_HI\_DEG}$	Deglitch time for USB power switch current limit enable	USB port enter overcurrent	1.228	2.048	2.867	ms
$t_{IOS\_HI\_RST}$	MFI OCP reset timing		9.6	16	22.4	ms
t_{r_USB}	PA_BUS, PB_BUS voltage rise time	C_L = 1 µF, R_L = 100 Ω (measured from 10% to 90% of final value)		1.67		ms
t_{f_USB}	PA_BUS, PB_BUS voltage fall time	C_L = 1 µF, R_L = 100 Ω (measured from 90% to 10% of final value)		0.49		ms
t_{on_USB}	PA_BUS, PB_BUS voltage turnon-time	C_L = 1 µF, R_L = 100 Ω		2.59		ms
t_{off_USB}	PA_BUS, PB_BUS voltage turnoff-time	C_L = 1 µF, R_L = 100 Ω		2.07		ms
t_{IOS_USB}	PA_BUS, PB_BUS short-circuit response time	C_L = 1 µF, R_L = 1 Ω		1		us
t_{r_OUT}	OUT voltage rise time	C_L = 1 µF, R_L = 100 Ω (measured from 10% to 90% of final value)	0.12	0.2	0.28	ms
t_{f_OUT}	OUT voltage fall time	C_L = 1 µF, R_L = 100 Ω (measured from 90% to 10% of final value)	0.16	0.22	0.28	ms
t_{on_OUT}	OUT voltage turnon-time	C_L = 1 µF, R_L = 100 Ω	0.6	1.1	1.65	ms
t_{off_OUT}	OUT voltage turnoff-time	C_L = 1 µF, R_L = 100 Ω	0.45	0.54	0.62	ms
t_{IOS_OUT}	OUT short-circuit response time	C_L = 1 µF, R_L = 1 Ω		1.4	4	us
HICCUP MODE						
T_{HICP_ON}	OUT, PA_BUS, PB_BUS output hiccup mode ON time	OC, V_{OUT}, V_{PA_BUS}, V_{PB_BUS} drop 10%	2.94	4.1	5.42	ms
T_{HICP_OFF}	OUT, PA_BUS, PB_BUS output hiccup mode OFF time	OC, OUT, PA_BUS, PB_BUS connect to GND	367	524	715	ms

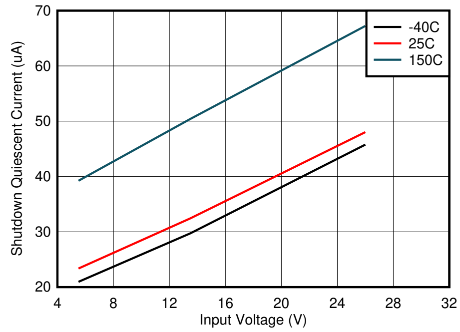
8.7 Switching Characteristics

Over the recommended operating junction temperature range of -40 °C to 150 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SW (SW PIN)						
T_{ON_MIN}	Minimum turnon-time			84		ns
T_{ON_MAX}	Maximum turnon-time, HS timeout in dropout			6		µs
T_{OFF_MIN}	Minimum turnoff time			81		ns
D_{max}	Maximum switch duty cycle			98		%
TIMING RESISTOR AND INTERNAL CLOCK						
f_{SW_RANGE}	Switching frequency range using FREQ mode (TPS25865-Q1)	9 kΩ ≤ R_{FREQ} ≤ 99 kΩ	200		800	kHz
f_{SW_RANGE}	Switching frequency range using FREQ mode (TPS25864-Q1)	9 kΩ ≤ R_{FREQ} ≤ 99 kΩ	200		3000	kHz
f_{SW}	Switching frequency	R_{FREQ} = 80.6 kΩ	228	253	278	kHz
		R_{FREQ} = 49.9 kΩ	360	400	440	kHz
f_{SW}	Switching frequency (TPS25864-Q1)	R_{FREQ} = 8.45 kΩ	1980	2200	2420	kHz
FS_{SS}	Frequency span of spread spectrum operation			±6		%
EXTERNAL CLOCK(SYNC)						
$f_{FREQ/SYNC}$	Switching frequency using external clock on FREQ/SYNC pin (TPS25865-Q1)		200		800	kHz
$f_{FREQ/SYNC}$	Switching frequency using external clock on FREQ/SYNC pin (TPS25864-Q1)		200		3000	kHz
T_{SYNC_MIN}	Minimum SYNC input pulse width	f_{SYNC} = 400kHz, $V_{FREQ/SYNC}$ > $V_{IH\_FREQ/SYNC}$, $V_{FREQ/SYNC}$ < $V_{IL\_FREQ/SYNC}$		100		ns
T_{LOCK_IN}	PLL lock time			100		µs

8.8 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 3.3 µH, C_{SENSE} = 141 µF, C_{PA_BUS} = 1 µF, C_{PB_BUS} = 1 µF, T_A = 25 °C.



$V_{EN/EULVO}$ = 0 V

图 8-1. Shutdown Quiescent Current

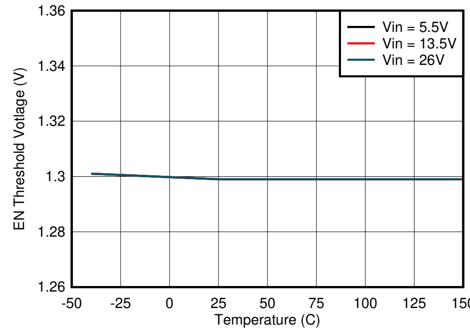
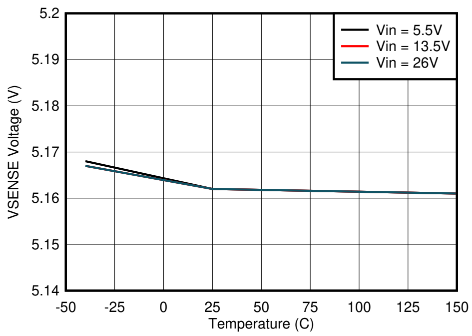
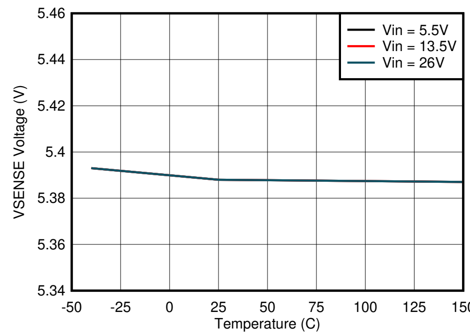


图 8-2. Precision Device Enable Threshold



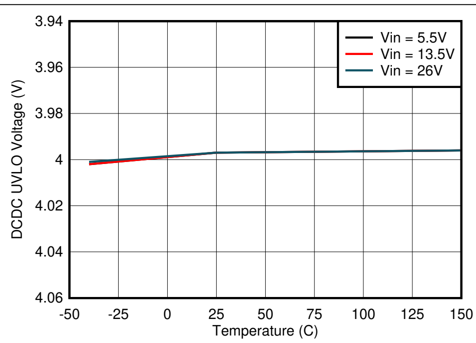
VSET = GND

图 8-3. V_{SENSE} Voltage vs Junction Temperature



R_{VSET} = 80.6 kΩ

图 8-4. V_{SENSE} Voltage vs Junction Temperature



$V_{EN/EULVO}$ = V_{SENSE}

图 8-5. DCDC UVLO Threshold

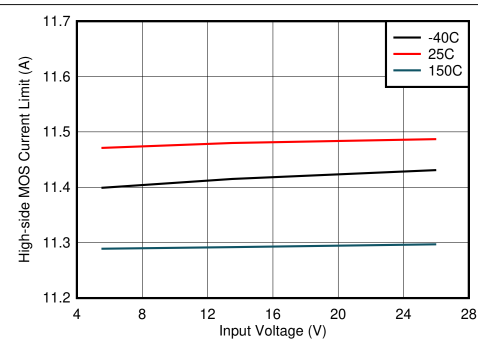


图 8-6. High-side Current Limit vs Input Voltage

8.8 Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 3.3 μH, C_{SENSE} = 141 μF, C_{PA_BUS} = 1 μF, C_{PB_BUS} = 1 μF, T_A = 25 °C.

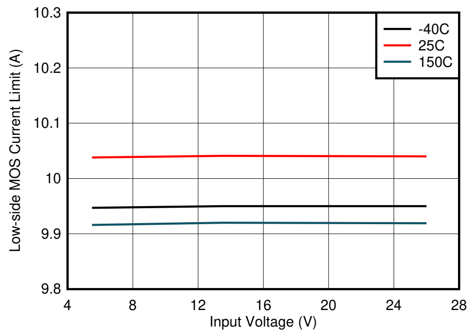
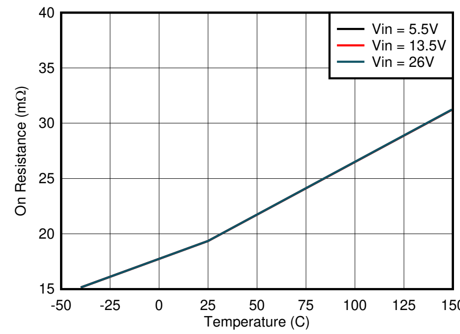
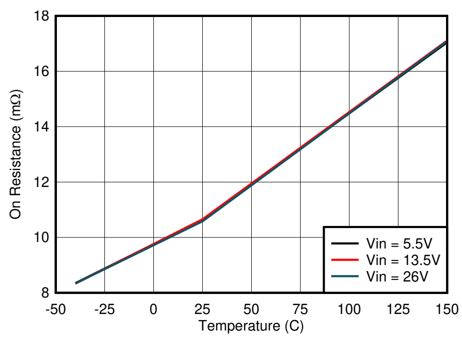


图 8-7. Low-side Current Limit vs Input Voltage



I_{PA_BUS} = 2.4 A I_{PB_BUS} = 2.4 A

图 8-8. High-side MOSFET on Resistance vs Junction Temperature



I_{PA_BUS} = 2.4 A I_{PB_BUS} = 2.4 A

图 8-9. Low-side MOSFET on Resistance vs Junction Temperature

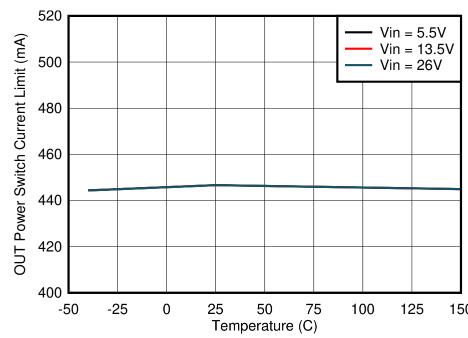
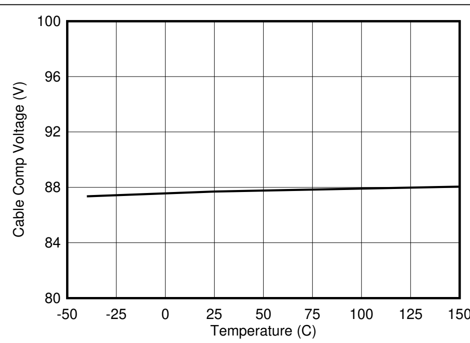


图 8-10. OUT Power Switch Current Limit vs Junction Temperature



I_{PA/B_BUS} = 2.4 A VSET = GND

图 8-11. Cable Compensation Voltage vs Junction Temperature

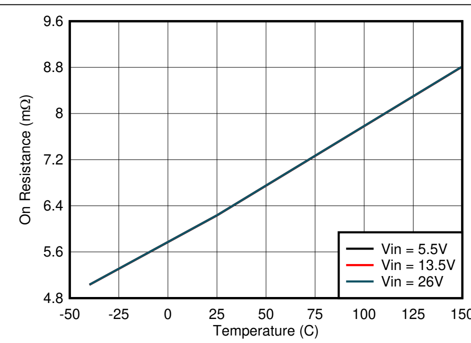


图 8-12. USB Power Switch On Resistance vs Junction Temperature

8.8 Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 3.3 μH, C_{SENSE} = 141 μF, C_{PA_BUS} = 1 μF, C_{PB_BUS} = 1 μF, T_A = 25 °C.

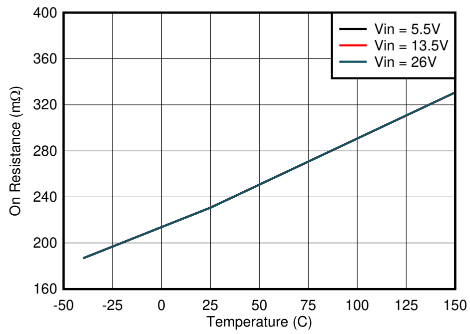
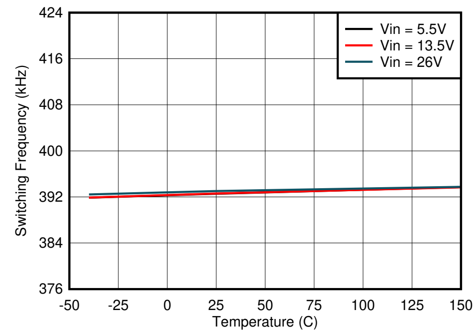


图 8-13. OUT Power Switch On Resistance vs Junction Temperature



R_{FREQ} = 49.9 kΩ

图 8-14. Switching Frequency vs Junction Temperature

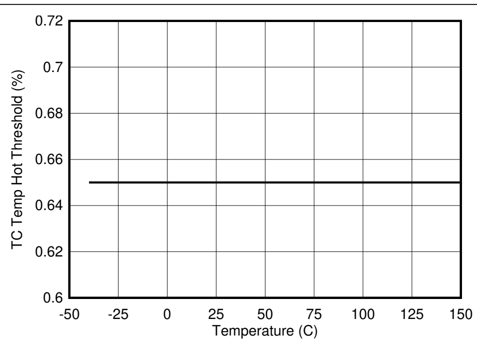


图 8-15. TS Temperature Hot Threshold vs Junction Temperature

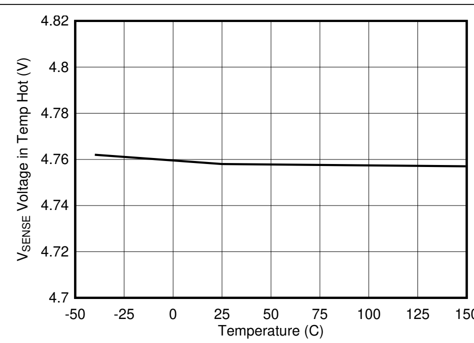


图 8-16. SENSE Voltage in Temperature Hot vs Junction Temperature

9 Parameter Measurement Information

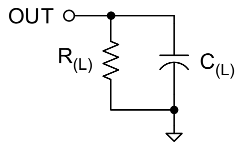


图 9-1. OUT Rise-Fall Test Load Figure

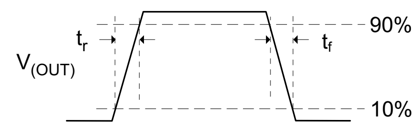


图 9-2. Power-On and Power-Off Timing

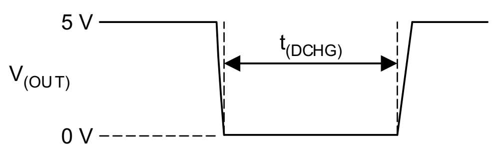


图 9-3. OUT Discharge During Mode Change

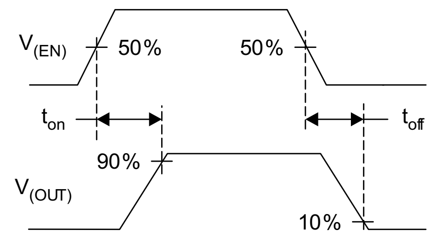


图 9-4. Enable Timing, Active-High Enable

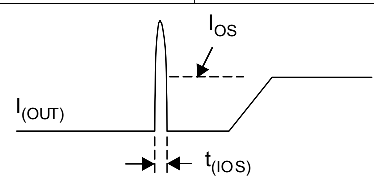


图 9-5. Output Short-Circuit Parameters

10 Detailed Description

10.1 Overview

The TPS2586x-Q1 is a full-featured solution for implementing a compact USB charging port with support BC1.2 standards. The device contain an efficient buck regulator power source. For dual Type-A ports, the TPS2586x-Q1 is capable of providing up to 5 A of output current at 5.17 V (nominal), 2.4 A for each Type-A port, 200 mA for the OUT pin. The TPS2586x-Q1 is an automotive-focused USB charging controller and offers a robust solution, so TI recommends to add adequate protection (TVS3300 equivalent or better but auto qualified) on the IN pin to protect systems from high-power transients or lightning strikes.

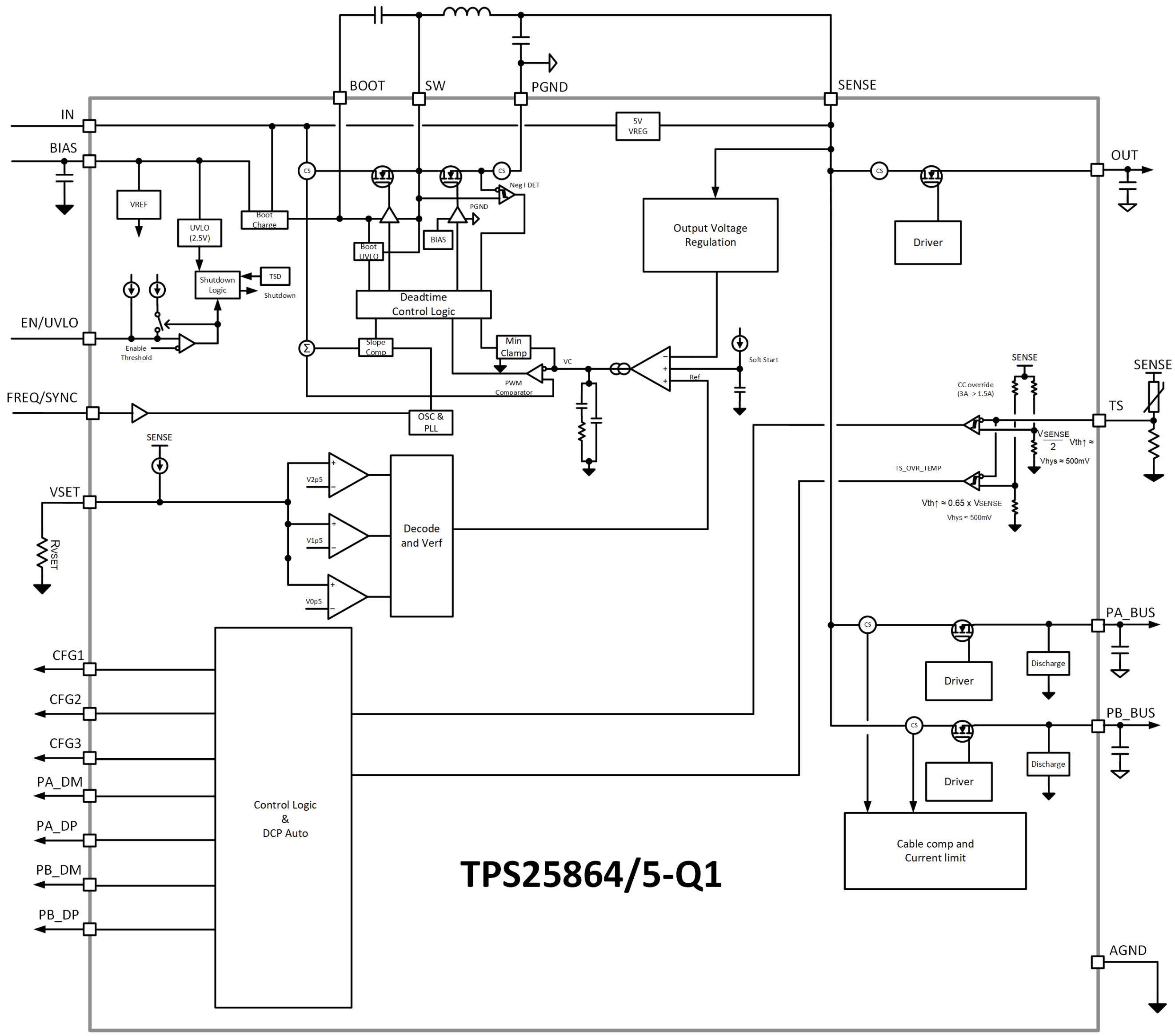
System designers can optimize efficiency or solution size through careful selection of switching frequency in the range of 200 kHz – 2400 kHz with sufficient margin to operate above or below the AM radio frequency band. TPS2586x-Q1 protects itself with internal thermal sensing circuits that monitor the operating temperature of the junction and disables operation if the temperature exceeds the Thermal Shutdown threshold, so in high ambient temperature application, the 5-A output current capability is not assured. In the TPS2586x-Q1, the buck regulator operates in forced PWM mode, ensuring fixed switching frequency regardless of load current. Spread-spectrum frequency dithering reduces harmonic peaks of the switching frequency, potentially simplifying EMI filter design and easing compliance.

Current sensing through a precision FET current sense amplifier on the USB port enables an accurate overcurrent limit setting and linear cable compensation to overcome IR losses when powering remote USB ports.

The TPS2586x-Q1 includes a TS input for user-programmable thermal protection using a negative temperature coefficient (NTC) resistor.

The device can support the legacy Battery Charging Specification Rev 1.2 (BC1.2) DCP mode with an auto-detect feature to charge not only BC1.2-compliant handheld devices, but also popular phones and tablets that incorporate their own propriety charging algorithm.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Power-Down or Undervoltage Lockout

The device is in low power mode if the IN terminal voltage is less than VUVLO, so the part is considered *dead* and all the terminals are high impedance. Once the IN voltage rises above the VUVLO threshold, the IC enters sleep mode or active mode, depending on the EN/UVLO voltage.

The voltage on the EN/UVLO pin controls the ON/OFF operation of the TPS2586x-Q1. An EN/UVLO pin voltage higher than $V_{EN/UVLO\text{-}H}$ is required to start the internal regulator. The internal USB monitoring circuitry is on when V_{IN} is within the operation range and the EN/UVLO threshold is cleared.

The EN/UVLO pin is an input and cannot be left open or floating. The simplest way to enable the operation of the TPS2586x-Q1 is to connect EN to SENSE. This connection allows self-startup of the TPS2586x-Q1 when V_{IN} is within the operation range. Note that you cannot connect the EN to IN pin directly for self-startup.

Many applications benefit from the employment of enable dividers R_{ENT} and R_{ENB} to establish a precision system UVLO level for the TPS2586x-Q1 shown in 图 10-1. The system UVLO can be used for sequencing, ensuring reliable operation, or supply protection, such as a battery discharge level. To ensure the USB port V_{BUS} is within the 5-V operating range as required for USB compliance (for the latest USB specifications and requirements, refer to *USB.org*), TI suggests that the R_{ENT} and R_{ENB} resistors be chosen such that the TPS2586x-Q1 enables when V_{IN} is approximately 6 V. Considering the dropout voltage of the buck regulator and IR losses in the system, 6 V provides adequate margin to maintain V_{BUS} within USB specifications. If system requirements, such as a warm crank (start) automotive scenario, require operation with V_{IN} < 6 V, the values of R_{ENT} and R_{ENB} can be calculated assuming a lower V_{IN}. An external logic signal can also be used to drive the EN/UVLO input when a microcontroller is present and it is desirable to enable or disable the USB port remotely for other reasons.

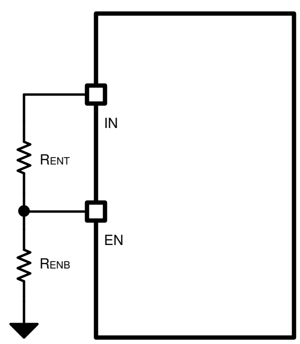


图 10-1. System UVLO by Enable Divider

UVLO configuration using external resistors is governed by the following equations:

$$R_{ENT} = \left(\frac{V_{IN(ON)}}{V_{EN/UVLO\_H}} - 1 \right) \times R_{ENB} \tag{1}$$

$$V_{IN(OFF)} = V_{IN(ON)} \times \left(1 - \frac{V_{EN/UVLO\_HYS}}{V_{EN/UVLO\_H}} \right) \tag{2}$$

For example:

$V_{IN(ON)}$ = 6 V

R_{ENT} = 20 kΩ

$$R_{ENB} = [(V_{EN\text{-}VOUT\text{-}H}) / (V_{IN(ON)} - V_{EN})] \times R_{ENT} \tag{3}$$

R_{ENB} = 5 kΩ

Therefore, $V_{IN(OFF)}$ = 5.5 V

10.3.2 Input Overvoltage Protection (OVP) - Continuously Monitored

The operation voltage range of the TPS2586x-Q1 is up to 26 V. If the input source applies an overvoltage, the buck regulator HSFET/LSFET turns off immediately. Thus, the USB ports and OUT pin loses their power as well. Once the overvoltage returns to a normal voltage, the buck regulator continues switching and provides power on the USB ports and OUT pin.

During the overvoltage condition, the internal regulator regulates the SENSE voltage at 5 V, so the SENSE always has power for the internal bias circuit and external NTC pullup reference.

10.3.3 Buck Converter

The following operating description of the TPS2586x-Q1 refers to the *Functional Block Diagram*.
The TPS2586x-Q1 integrates a monolithic, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs and USB current-limit switches with charging ports auto-detection. The TPS2586x-Q1 offers a compact solution that achieves up to 5 A of continuous output current with excellent load and line regulation over a wide input supply range. The TPS2586x-Q1 supplies a regulated output voltage by turning on the high-side (HS) and low-side (LS) NMOS switches with controlled duty cycle. During high-side switch ON time, the SW pin voltage swings up to approximately V_{IN}. The inductor current, i_L, increases with linear slope (V_{IN} – V_{OUT}) / L. When the HS switch is turned off by the control logic, the LS switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the LS switch with a slope of –V_{OUT} / L. The control parameter of a buck converter is defined as Duty Cycle D = t_{ON} / T_{SW}, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period, shown in 图 10-2. The regulator control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

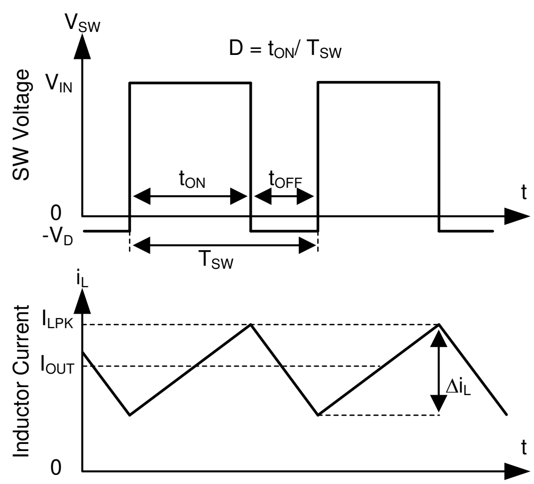


图 10-2. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The TPS2586x-Q1 operates in a fixed-frequency, peak-current-mode control to regulate the output voltage. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the ON time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, making it easy to design, and provides stable operation with a reasonable combination of output capacitors. The TPS2586x-Q1 operates in FPWM mode for low output voltage ripple, tight output voltage regulation, and constant switching frequency.

10.3.4 FREQ/SYNC

The switching frequency of the TPS2586x-Q1 can be programmed by the resistor, R_{FREQ}, from the FREQ/SYNC pin and AGND pin. To determine the FREQ resistance for a given switching frequency, use 方程式 4:

$$R_{FREQ}(k\Omega) = 26660 \times f_{SW}^{-1.0483}(kHz) \tag{4}$$

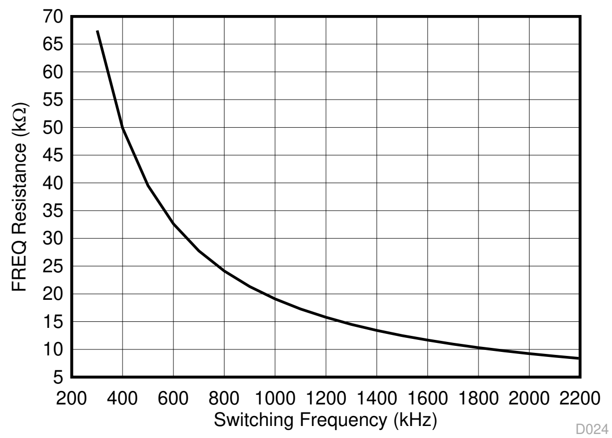


图 10-3. FREQ Set Resistor vs Switching Frequency

The normal method of setting the buck regulator switching frequency is by selecting an appropriate value FREQ resistor. The typical FREQ resistors value are listed in 表 10-1. Please note that TPS25865-Q1 can only support frequency up to 800 kHz.

表 10-1. Setting the Switching Frequency With FREQ

FREQ (KΩ)	SWITCHING FREQUENCY (KHz)
80.6	253
49.9	400
19.1	1000
8.87	2100
8.45	2200

The FREQ/SYNC pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by AC coupling a positive edge into the FREQ/SYNC pin. When using a low impedance signal source, the frequency setting resistor, FREQ, is connected in parallel with an AC coupling capacitor, C_{COUP}, to a termination resistor, R_{TERM} (for example, 50 Ω). The two resistors in series provide the default frequency setting resistance when the signal source is turned off. A 10-pF ceramic capacitor can be used for C_{COUP}. The AC coupled peak-to-peak voltage at the FREQ/SYNC pin must exceed the SYNC amplitude threshold of 1.2 V (typical) to trip the internal synchronization pulse detector, and the minimum SYNC clock HIGH and LOW time must be longer than 100 ns (typical). A 2.5 V or higher amplitude pulse signal coupled through a 1-nF capacitor, C_{SYNC}, is a good starting point. 图 10-4 shows the device synchronized to an external system clock. The external clock must be off before startup to allow proper startup sequencing.

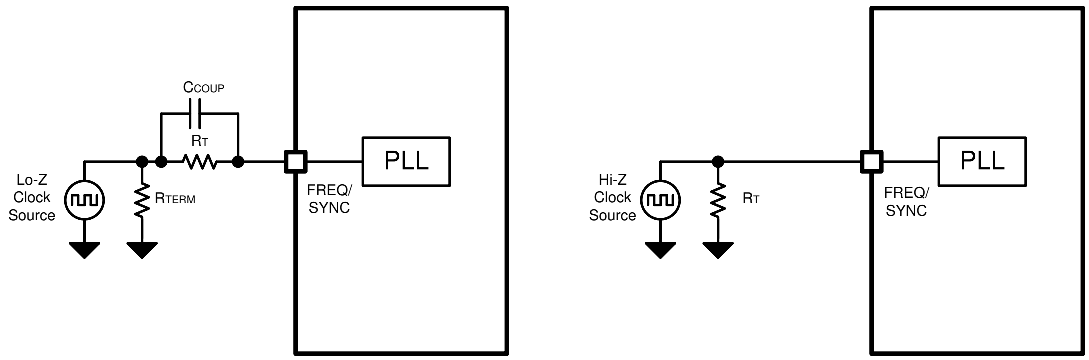


图 10-4. Synchronize to External Clock

TPS25864-Q1 switching action can be synchronized to an external clock from 200 KHz to 3 MHz. TPS25865-Q1 switching action can be synchronized to an external clock from 200 KHz to 800 kHz. Note the higher switching frequency results in more power loss on IC, causing the junction temperature and also the board temperature rising. Then, the device can enter load shedding under high ambient temperature.

10.3.5 Bootstrap Voltage (BOOT)

The TPS2586x-Q1 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the low-side switch conducts. The recommended value of the BOOT capacitor is 100 nF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended for stable performance over temperature and voltage. The BOOT rail has a UVLO to protect the chip from operation with too little bias and is typically 2.2 V. If the BOOT capacitor voltage drops below the UVLO threshold, the device initiates a charging sequence using the low-side FET before attempting to turn on the high-side device.

10.3.6 Minimum ON-Time, Minimum OFF-Time

Minimum ON-time, T_{ON_MIN}, is the smallest duration of time that the HS switch can be on. T_{ON_MIN} is typically 84 ns in the TPS2586x-Q1. Minimum OFF-time, T_{OFF_MIN}, is the smallest duration that the HS switch can be off. T_{OFF_MIN} is typically 81 ns in the TPS2586x-Q1. In CCM (FPWM) operation, T_{ON_MIN} and T_{OFF_MIN} limit the voltage conversion range given in a selected switching frequency.

The minimum duty cycle allowed is:

$$D_{MIN} = T_{ON\_MIN} \times f_{SW} \tag{5}$$

And the maximum duty cycle allowed is:

$$D_{MAX} = 1 - T_{OFF\_MIN} \times f_{SW} \tag{6}$$

Given fixed T_{ON_MIN} and T_{OFF_MIN}, the higher the switching frequency, the narrower the range of the allowed duty cycle.

Given an output voltage, the choice of the switching frequency affects the allowed input voltage range, solution size, and efficiency. The maximum operation supply voltage can be found by:

$$V_{IN\_MAX} = \frac{V_{OUT}}{\left(f_{SW} \times T_{ON\_MIN}\right)} \tag{7}$$

At lower supply voltage, the switching frequency is limited by T_{OFF_MIN}. The minimum V_{IN} can be approximated by:

$$V_{IN\_MIN} = \frac{V_{OUT}}{\left(1 - f_{SW} \times T_{OFF\_MIN}\right)} \quad (8)$$

Considering power losses in the system with heavy load operation, V_{IN_MAX} is higher than the result calculated in 方程式 7.

If minimum ON-time or minimum OFF-time do not support the desired conversion ratio, frequency is reduced, automatically allowing regulation to be maintained during load dump and with very low dropout during cold crank even with high operating-frequency setting.

10.3.7 Internal Compensation

The TPS2586x-Q1 is internally compensated. The internal compensation is designed such that the loop response is stable over the specified operating frequency and output voltage range. TPS25865-Q1 is optimized for transient response over the range of 200 kHz ≤ fsw ≤ 800 kHz.TPS25864-Q1 is optimized for transient response over the range of 200 kHz ≤ fsw ≤ 3 MHz.

10.3.8 Selectable Output Voltage (VSET)

The TPS2586x-Q1 provides four different output voltage options. The voltage can be set by an external resistor across the VSET pin. The normal method of setting the buck output voltage is by selecting an appropriate value VSET resistor as shown in 表 10-2.

表 10-2. VSET Configuration vs BUS Output Voltage

VSET CONFIGURATION	V_{SENSE}
Float or pull up to V_{SENSE}	5.1 V
Short to GND	5.17 V
R_{VSET} = 40.2 KΩ	5.3 V
R_{VSET} = 80.6 KΩ	5.4 V

Note that the VSET has an internal weak 20-µA current source to overdrive the pin to SENSE. If this pin is floated, the voltage on this pin approaches the SENSE voltage, and sets the output voltage to 5.1 V. TI does not recommend to float this pin if there is external noise from the PCB board because the noise interferes with the VSET internal logic block.

10.3.9 Current Limit and Short Circuit Protection

For maximum versatility, the TPS2586x-Q1 includes both a precision, fixed current limit as well cycle-by-cycle current limit to protect the USB port from extreme overload conditions. The cycle-by-cycle current limit serves as a backup means of protection.

10.3.9.1 USB Switch Current Limit

Because the TPS2586x-Q1 integrates two USB current-limit switches, it provides current limit to prevent USB port overheating. The USB current limit threshold is fixed at 2.73 A with a maximum ±10% variation overtemperature on each USB port to follow the Type-A specification. The TPS2586x-Q1 provides built-in soft-start circuitry that controls the rising slew rate of the output voltage to limit inrush current and voltage surges.

The TPS2586x-Q1 engages the two-level current limit scheme, which has one typical current limit, I_{OS_BUS}, and the secondary current limit, I_{OS_HI}. The secondary current limit, I_{OS_HI}, is 1.6x the primary current limit, I_{OS_BUS}.The secondary current limit acts as the current limit threshold for a deglitch time, tIOS_HI_DEG, then the USB power switch current limit threshold is set back to I_{OS_BUS}.

The secondary current limit, I_{OS_HI}, allows the USB port pull out a larger current for a short time during transient overload conditions, which can bring benefits for USB port special overload testing like MFi OCP. In a normal application, once the device is powered on and USB port is not in UVLO, the USB port current limit threshold is overridden by the secondary current limit, I_{OS_HI}, so the USB port can output as high as a 1.6 × I_{OS_BUS} current for typically 2 ms. After the deglitch time, $t_{IOS\_HI\_DEG}$, the current limit threshold is set back to the typical current with I_{OS_BUS}. The secondary current limit threshold does not resume until after the $t_{IOS\_HI\_RST}$ deglitch time, which is typically 16 ms. If there is an inrush current higher than the I_{OS_HI} threshold, the current limit is set back to I_{OS_BUS} immediately, without waiting for a $t_{IOS\_HI\_DEG}$.

The TPS2586x-Q1 responds to overcurrent conditions by limiting output current to I_{OS_BUS} as shown in previous equation. When an overload condition occurs, the device maintains a constant output current and the output voltage reduces accordingly. Three possible overload conditions can occur:

- The first condition is when a short circuit or overload is applied to the USB output when the device is powered up or enabled. There can be inrush current and once it triggers the approximate 8-A threshold. A fast turnoff circuit is activated to turn off the USB power switch within t_{IOS_USB} before the current limit control loop is able to respond (shown in 图 10-5). After the fast turnoff is triggered, the USB power switch current-sense amplifier is over-driven during this time and momentarily disables the internal N-channel MOSFET to turn off USB port. The current-sense amplifier then recovers and ramps the output current with a soft start. If the USB port is still in overcurrent condition, the short circuit and overload hold the output near zero potential with respect to ground and the power switch ramps the output current to I_{OS_BUS}. If the overcurrent limit condition lasts longer than 4.1 ms, the corresponding USB channel enters hiccup mode with 524 ms of off-time and 4.1 ms of on-time.

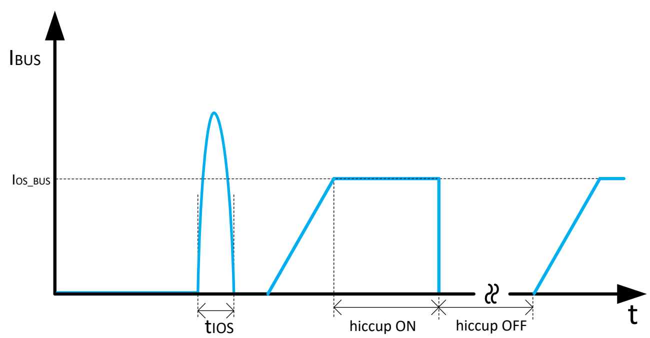


图 10-5. Response Time to BUS Short-Circuit

- The second condition is the load current increases above I_{OS_BUS} but below the I_{OS_HI} setting. The device allows the USB port to output this large current for $t_{IOS\_HI\_DEG}$, without limiting the USB port current to I_{OS_BUS}. After the $t_{IOS\_HI\_DEG}$ deglitch time, the device limits the output current to I_{OS_BUS} and works in a constant current-limit mode. If the load demands a current greater than I_{OS_BUS}, the USB output voltage decreases to $I_{OS\_BUS} \times R_{LOAD}$ for a resistive load, which is shown in 图 10-6. If the overcurrent limit condition lasts longer than 4.1 ms, the corresponding USB channel enters hiccup mode with 524 ms of off-time and 4.1 ms of on-time. Another USB channel still works normally.

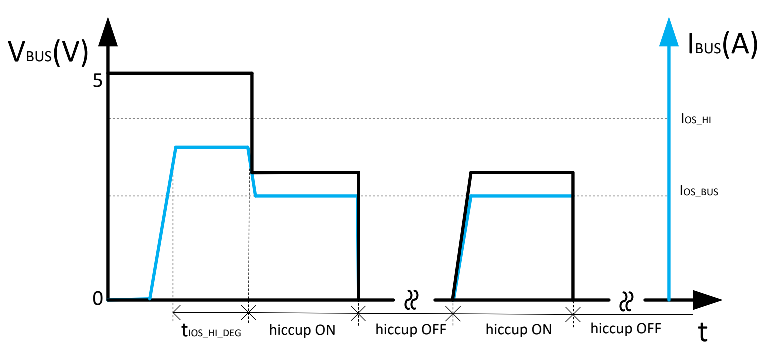


图 10-6. BUS Overcurrent Protection

- The third condition is the load current increases just over the I_{OS_HI} setting. In this case, the load current does not trigger the fast turnoff. The USB power switch current limit threshold is set back to the primary current limit, I_{OS_BUS}, immediately. If the load still demands a current greater than I_{OS_BUS}, the USB output voltage decreases to $I_{OS\_BUS} \times R_{LOAD}$ for a resistive load, which is shown in 图 10-7. If the overcurrent limit condition lasts longer than 4.1 ms, the corresponding USB channel enters hiccup mode with 524 ms of off-time and 4.1 ms of on-time. Another USB channel still works normally.

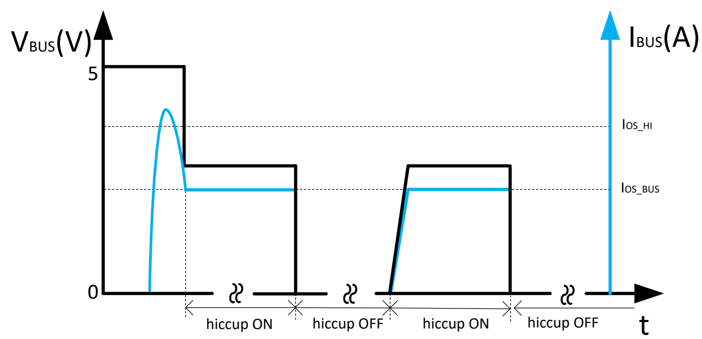


图 10-7. BUS Overcurrent Protection: Two-Level Current Limit

The TPS2586x-Q1 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the previously mentioned cases. Thermal limiting turns off the internal NFET and starts when the NFET junction temperature exceeds 160°C (typical). The device remains off until the NFET junction temperature cools 10°C (typical) and then restarts. This extra thermal protection mechanism can help prevent further junction temperature rise, which can cause the device to turn off due to junction temperature exceeding the main thermal shutdown threshold, T_{SD}.

10.3.9.2 Interlocking for Two-Level USB Switch Current Limit

The TPS2586x-Q1 has two USB ports. Because the secondary current limit, I_{OS_HI}, is 1.6x of the primary current limit, I_{OS_BUS}, if the two USB ports pull out large current at the same time, then the DC-DC regulator is overloaded, and DC-DC regulator output voltage can be crashed. To avoid these potential issues, the TPS2586x-Q1 adopts the interlocking scheme to manage the current limits of the two USB ports.

For interlocking, if one USB port current is beyond the primary current limit threshold, I_{OS_BUS}, then another USB port current limit threshold is overridden to the primary current limit, I_{OS_BUS}, immediately. With this control scheme, the TPS2586x-Q1 only allows one USB port to output a large current, which can be as high as 1.6x of the primary current limit, I_{OS_BUS}, at the same time. Ensure the DC-DC regulator has enough energy to sustain its output voltage.

10.3.9.3 Cycle-by-Cycle Buck Current Limit

There is a buck regulator cycle-by-cycle current limit on both the peak and valley of the inductor current.

High-side MOSFET overcurrent protection is implemented by the nature of the peak current mode control. The HS switch current is sensed when the HS is turned on after a set blanking time. The HS switch current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. The peak current of HS switch is limited by a clamped maximum peak current threshold, I_{HS_LIMIT}, which is constant. The peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

The current going through LS MOSFET is also sensed and monitored. When the LS switch turns on, the inductor current begins to ramp down. The LS switch does not turn OFF at the end of a switching cycle if its current is above the LS current limit, I_{LS_LIMIT}. The LS switch is kept ON so that the inductor current keeps ramping down until the inductor current ramps below the LS current limit, I_{LS_LIMIT}. Then, the LS switch is turned OFF and the HS switch is turned on after a dead time. This action is somewhat different than the more typical peak current limit and results in 方程式 9 for the maximum load current.

$$I_{OUT\_MAX} = I_{LS\_LIMIT} + \frac{(V_{IN} - V_{OUT})}{2 \times f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}} \tag{9}$$

10.3.9.4 OUT Current Limit

The TPS2586x-Q1 can provide 200-mA current at the OUT pin to power the auxiliary loads, such as USB HUB, LEDs. The input of the OUT power switch comes from the buck regulator output, so the OUT voltage is the same with the SNESE voltage but deducts the OUT $R_{DS\text{-}ON}$ voltage loss.

If the OUT current reaches the current limit level, the OUT pin MOSFET works in a constant current-limit mode. If the overcurrent limit condition lasts longer than 4.1 ms, it enters hiccup mode with 4.1 ms of on-time and 524 ms of off-time.

10.3.10 Cable Compensation

When a load draws current through a long or thin wire, there is an IR drop that reduces the voltage delivered to the load. In the vehicle from the voltage regulator output V_{OUT} to V_{BUS} (input voltage of portable device), the total resistance of PCB trace, connector, and cable resistances causes an IR drop at the portable device input, so the charging current of most portable devices is less than their expected maximum charging current. The voltage drop is shown in 图 10-8.

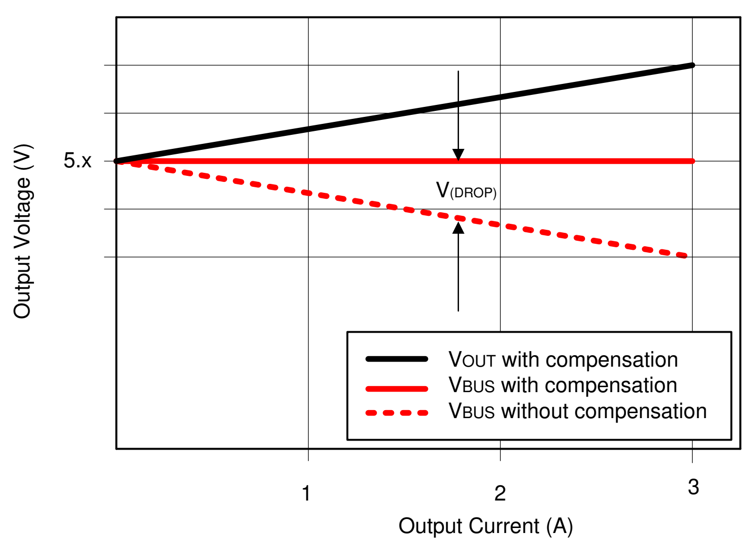


图 10-8. Voltage Drop

To handle this case, the TPS2586x-Q1 has a built-in cable compensation function where the droop compensation linearly increases the voltage at the SENSE pin of the TPS2586x-Q1 as load current increases, to maintain a fairly constant output voltage at the load-side voltage.

For the TPS2586x-Q1, the internal comparator compares the current-sense output voltage of the two current-limit switches and uses the larger current-sense output voltage to compensate for the line drop voltage. The cable compensation amplitude increases linearly as the load current increases. The cable compensation also has an upper limitation. The cable compensation at output currents greater than 2.4 A is 90 mV and is shown in 图 10-9. Note the cable compensation only works when you short the VSET to GND. For the other VSET configuration, the cable compensation is not available.

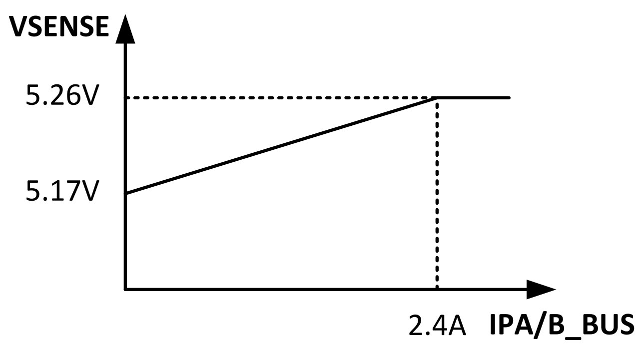


图 10-9. Dual Ports Cable Compensation

10.3.11 Thermal Management With Temperature Sensing (TS) and OTSD

The TS input pin allows for user-programmable thermal protection (for the TS pin thresholds, see the *Electrical Characteristics* section). The TS input pin threshold is ratiometric with V_{SENSE}. The external resistor divider setting, V_{TS}, must be connected to the TPS2586x-Q1 SENSE pin to achieve accurate results (refer to the 图 10-10).

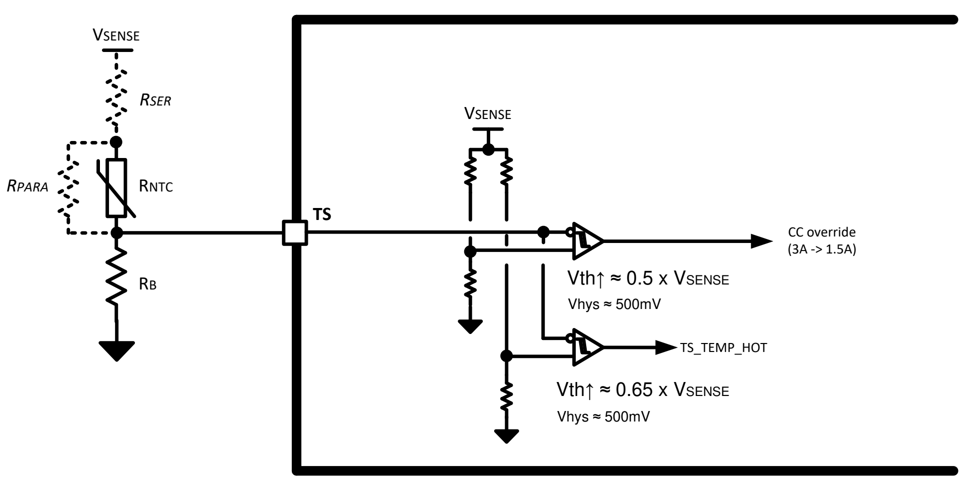


图 10-10. TS Input

If the overtemperature condition happens, causing V_{TS} = 0.65 × V_{SENSE}, the TPS2586x-Q1 reduces the BUCK regulator output voltage to 4.77 V.

If the Overtemperature condition persists, causing T_J to reach the OTSD threshold, then the device thermal shuts down.

The NTC thermistor must be placed near the hottest point on the PCB. In most cases, this placement is close to the SW node of the TPS2586x-Q1, near the buck inductor.

10.3.12 Thermal Shutdown

The device has an internal overtemperature shutdown threshold, T_{SD}, to protect the device from damage and overall safety of the system. When the device temperature exceeds T_{SD}, the device is turned off when thermal shutdown activates. Once the die temperature falls below 154°C (typical), the device re-initiates the power-up sequence controlled by the internal soft-start circuitry.

10.3.13 USB Specification Overview

All USB ports are capable of providing a 5-V output, making them a convenient power source for operating and charging portable devices. USB specification documents outline specific power requirements to ensure interoperability. In general, a USB 2.0 port host port is required to provide up to 500 mA; a USB 3.0 or USB 3.1 port is required to provide up to 900 mA; ports adhering to the USB Battery Charging 1.2 Specification provide up to 1500 mA; newer Type-C ports can provide up to 3000 mA. Though USB standards governing power requirements exist, some manufacturers of popular portable devices created their own proprietary mechanisms to extend allowed available current beyond the 1500-mA maximum per BC 1.2. While not officially part of the standards maintained by the USB-IF, these proprietary mechanisms are recognized and implemented by manufacturers of USB charging ports.

The TPS2586x-Q1 device supports four of the most-common USB-charging schemes found in popular hand-held media and cellular devices:

- USB Battery Charging Specification BC1.2 DCP mode
- Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider 3 mode
- 1.2-V mode

10.3.14 USB Port Operating Modes

10.3.14.1 Dedicated Charging Port (DCP) Mode

A DCP only provides power and does not support data connection to an upstream port. As shown in the following sections, a DCP is identified by the electrical characteristics of the data lines. TPS2586x-Q1 only emulates one state, DCP-auto state. In the DCP-auto state, the device charge-detection state machine is activated to selectively implement charging schemes involved with the shorted, Divider 3 and 1.2-V modes. The shorted DCP mode complies with BC1.2 and Chinese Telecommunications Industry Standard YD/T 1591-2009, whereas the Divider 3 and 1.2-V modes are employed to charge devices that do not comply with the BC1.2 DCP standard.

10.3.14.1.1 DCP BC1.2 and YD/T 1591-2009

Both standards specify that the D+ and D – data lines must be connected together with a maximum series impedance of 200 Ω, as shown in 图 10-11.

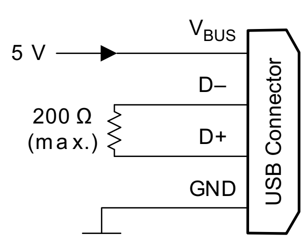


图 10-11. DCP Supporting BC1.2 and YD/T 1591-2009

10.3.14.1.2 DCP Divider-Charging Scheme

The device supports Divider 3, as shown in 图 10-12. In the Divider 3 charging scheme, the device applies 2.7 V and 2.7 V to D+ and D – data lines.

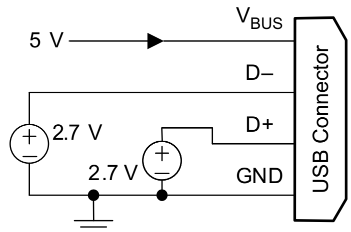


图 10-12. Divider 3 Mode

10.3.14.1.3 DCP 1.2-V Charging Scheme

The DCP 1.2-V charging scheme is used by some hand-held devices to enable fast charging at 2 A. The TPS2586x-Q1 device supports this scheme in DCP-auto state before the device enters BC1.2 shorted mode. To simulate this charging scheme, the D+ and D – lines are shorted and pulled up to 1.2 V for a fixed duration. Then the device moves to DCP shorted mode as defined in the BC1.2 specification and as shown in 图 10-13.

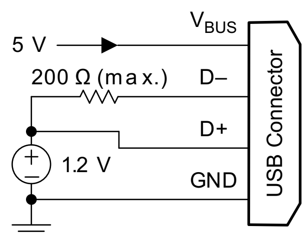


图 10-13. 1.2-V Mode

10.3.14.2 DCP Auto Mode

The TPS2586x-Q1 device integrates an auto-detect state machine that supports all the DCP charging schemes as shown in 图 10-14. The auto-detect state machine starts in the Divider 3 scheme. If a BC1.2 or YD/T 1591-2009 compliant device is attached, the TPS2586x-Q1 device responds by turning the power switch back on without output discharge and operating in 1.2-V mode briefly before entering BC1.2 DCP mode. Then, the auto-detect state machine stays in that mode until the device releases the data line, in which case, the auto-detect state machine goes back to the Divider 3 scheme. When a Divider 3-compliant device is attached, the TPS2586x-Q1 device stays in the Divider 3 state.

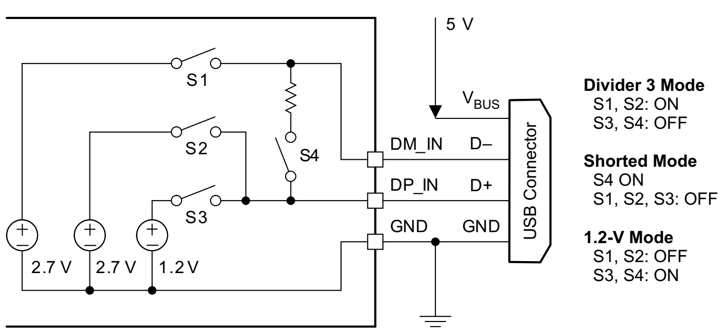


图 10-14. DCP Auto Mode

10.4 Device Functional Modes

10.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the TPS2586x-Q1. When V_{EN} is below 1.2 V (typical), the device is in shutdown mode. The TPS2585x-Q1 also employs V_{IN} overvoltage lock out protection and V_{SENSE} undervoltage lock out protection. If V_{IN} voltage is above its respective OVLO level, V_{OVLO}, or V_{SENSE} voltage is below its respective UVLO level, V_{DCDC_UVLO}, the DC/DC converter turns off.

10.4.2 Active Mode

The TPS2586x-Q1 is in active mode when V_{EN} is above the precision enable threshold and V_{SENSE} is above its respective UVLO levels. The simplest way to enable the TPS2586x-Q1 is to connect the EN pin to SENSE pin. This connection allows self startup when the input voltage is in the operating range (5.5 V to 26 V) and a UFP detection is made.

In active mode, the TPS25865-Q1 buck regulator does not operate unless CFG1/3 resistors are attached, the TPS25854-Q1 buck regulator operates even though CFG1/3 resistors are not attached. Then the buck regulator operates with Forced Pulse Width Modulation (FPWM), also referred to as Forced Continuous Conduction Mode (FCCM). This operation ensures the buck regulator switching frequency remains constant under all load conditions. FPWM operation provides low output voltage ripple, tight output voltage regulation, and constant switching frequency. Built-in spread-spectrum modulation aids in distributing spectral energy across a narrow band around the switching frequency programmed by the FREQ/SYNC pin. Under light load conditions the inductor current is allowed to go negative. A negative current limit of $I_{L\text{-}NEG\text{-}LS}$ is imposed to prevent damage to the regulator's low side FET. During operation, the TPS2586x-Q1 synchronizes to any valid clock signal on the FREQ/SYNC input.

11 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

11.1 Application Information

The TPS2586x-Q1 is a step down DC-to-DC regulator and USB charge port controller. The TPS2586x-Q1 is typically used in automotive systems to convert a DC voltage from the vehicle battery to 5-V DC with a maximum output current of 5 A in dual Type-A ports applications. The TPS2586x-Q1 engages a high efficiency buck converter, letting the device operate at as high as 85°C ambient temperature with full load. The following design procedure can be used to select components for the TPS2586x-Q1.

11.2 Typical Applications

The TPS2586x-Q1 only requires a few external components to convert from a wide voltage range supply to a 5-V output to power USB devices. 图 11-1 shows the TPS2586x-Q1 typical application schematic for Dual Type-A charging ports under 400-kHz operating frequency.

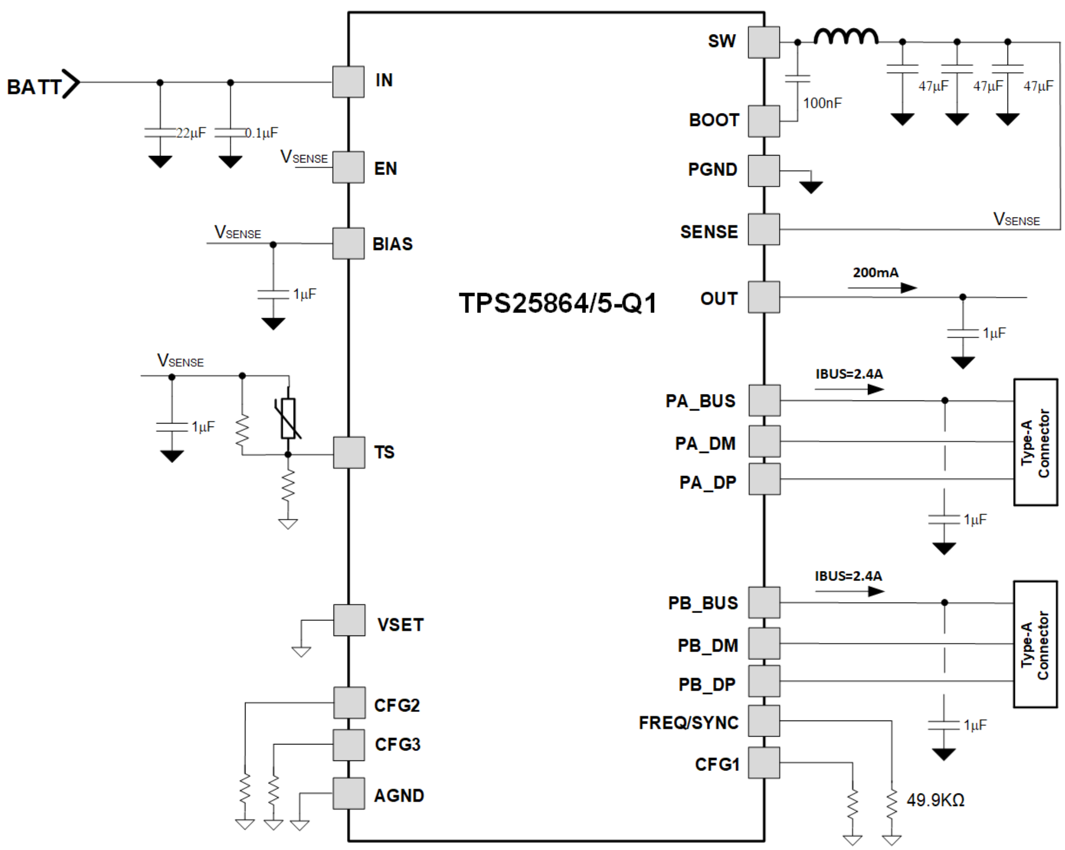


图 11-1. TPS2586x-Q1 Typical Application Circuit for 400-KHz f_{SW}

As a quick start guide, 表 11-1 provides typical component values for some of the most common configurations. The values given in 表 11-1 are typical. Other values can be used to enhance certain performance criterion as required by the application. The integrated buck regulator of TPS2586x-Q1 is internally compensated and optimized for a reasonable selection of external inductance and capacitance. The external components have to fulfill the needs of the application, but also the stability criteria of the control loop of the device.

表 11-1. L and C_{OUT} Typical Values

f_{SW}	V_{OUT} WITHOUT CABLE COMPENSATION	L	C_{HF} + C_{IN}	C_{BOOT}	RATED C_{OUT}
400 KHZ	5.17 V	3.3 µH	1 × 100 nF + 1 × 47 µF	1 × 100 nF	3 × 47 µF
2.1 MHz	5.17 V	0.68 µH	1 × 100 nF + 1 × 22 µF	1 × 100 nF	3 × 22 µF

1. The inductance value is calculated based on max V_{IN} = 18 V.
2. All the C_{OUT} values are after derating and use low ESR ceramic capacitors.
3. The C_{OUT} is the buck regulator output capacitors at the SENSE pin.

11.2.1 Design Requirements

The detailed design procedure is described based on a design example. For this design example, use the parameters listed in 表 11-2 as the input parameters.

表 11-2. Design Example Parameters

Input voltage, V_{IN}	13.5-V typical, range from 8 V to 18 V
Output voltage, V_{SENSE}	5.17 V
Maximum output current	5 A
Switching frequency, f_{SW}	400 KHz

11.2.2 Detailed Design Procedure

11.2.2.1 Output Voltage Setting

The output voltage of TPS2586x-Q1 is programmed by the VSET pin, and if short VSET to GND sets the output voltage at 5.17 V and enables the cable compensation function, the output voltage increases linearly with increasing load current. Refer to List item for more details on output voltage setting. Cable compensation can be used to increase the voltage on the SENSE pin linearly with increasing load current. Refer to List item.referenceTitle for more details on cable compensation setting. If cable compensation is not desired, use a 0-Ω R_{IMON} resistor.

11.2.2.2 Switching Frequency

The recommended switching frequency of the TPS2586x-Q1 is in the range of 250 KHz – 400 KHz for high efficiency. Choose R_{FREQ} = 49.9 kΩ for 400-KHz operation. To choose a different switching frequency, refer to 表 10-1.

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, and hence, a more compact design. In automotive USB charging applications, switching frequency tends to operate at either 400 kHz below the AM band, or 2.1 MHz above the AM band. In this example, 400 kHz is chosen.

11.2.2.3 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the rated current. The inductance is based on the desired peak-to-peak ripple current, Δi_L. Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use 方程式 11 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} must be 20% to 40%. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current must still be used. During an instantaneous short or overcurrent operation event, the RMS and peak inductor current can be high. The inductor current rating must be higher than the current limit of the device.

$$\Delta i_L = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times L \times f_{SW}} \tag{10}$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \tag{11}$$

In general, choose lower inductance in switching power supplies because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. Too low of an inductance can generate too large of an inductor current ripple such that overcurrent protection at the full load can be falsely triggered. This low inductance also generates more conduction loss and inductor core loss. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak current mode control, TI recommends to not have too small of an inductor current ripple. A larger peak current ripple improves the comparator signal to noise ratio.

For this design example, choose K_{IND} = 0.3, and find an inductance of approximately 3.58 μH. Select the next standard value of 3.3 μH.

11.2.2.4 Output Capacitor Selection

The output capacitor or capacitors, C_{OUT}, must be chosen with care because it directly affects the steady state output voltage ripple, loop stability, and the voltage overshoot/undershoot during load current transients.

The value of the output capacitor and its ESR, determine the output voltage ripple and load transient performance. The output capacitor is usually limited by the load transient requirements rather than the output voltage ripple if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a fast large load increase happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The control loop of the regulator usually needs four or more clock cycles to respond to the output voltage droop. The output capacitance must be large enough to supply the current difference for four clock cycles to maintain the output voltage within the specified range. 表 11-3 can be used to find output capacitors for a few common applications. In this example, good transient performance is desired giving 3 × 47-μF ceramic as the output capacitor.

表 11-3. Selected Output Capacitor

FREQUENCY	C_{OUT}	SIZE and COST	TRANSIENT PERFORMANCE
400 KHz	3 × 47-μF ceramic	Small size	Good
400 KHz	2 × 47-μF ceramic	Small size	Minimum
400 KHz	4 × 22 μF + 1 × 260 μF, < 50-mΩ electrolytic	Larger size, low cost	Good
400 KHz	1 × 4.7 μF + 2 × 10 μF + 1 × 260 μF, < 50-mΩ electrolytic	Lowest cost	Minimum
2.1 MHz	3 × 22 μF ceramic	Small size	Good
2.1 MHz	2 × 47 μF ceramic	Small size	Better
2.1 MHz	2 × 22 μF ceramic	Smallest size	Minimum

11.2.2.5 Input Capacitor Selection

The TPS2586x-Q1 device requires a high frequency input decoupling capacitor or capacitors, depending on the application. A high-quality ceramic capacitor type X5R or X7R with sufficient voltage rating is recommended. The ceramic input capacitors provide a low impedance source to the converter in addition to supplying the ripple current and isolating switching noise from other circuits. The typical recommended value for the high frequency decoupling capacitor is 10 μF of ceramic capacitance. This capacitance must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple, maintain the input voltage during load transients, or both. In addition, a small case size 100-nF ceramic capacitor must be used at IN and PGND, immediately adjacent to the converter. This action provides a high frequency bypass for the control circuits internal to the device. For this example a 10-µF, 50-V, X7R (or better) ceramic capacitor is chosen, and the 100-nF ceramic capacitor must also be rated at 50 V with an X7R or better dielectric.

Additionally, an electrolytic capacitor on the input in parallel with the ceramics can be required, especially if long leads from the automotive battery to the IN pin of the TPS2586x-Q1, cold or warm engine crank requirements, and so forth. The moderate ESR of this capacitor is used to provide damping to the voltage spike due to the lead inductance of the cable or the trace.

11.2.2.6 Bootstrap Capacitor Selection

The TPS2586x-Q1 design requires a bootstrap capacitor (C_{BOOT}). The recommended capacitor is 100 nF and rated 16 V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability.

11.2.2.7 Undervoltage Lockout Set-Point

The system undervoltage Lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. 方程式 12 can be used to determine the V_{IN} UVLO level.

$$V_{IN\_RISING} = V_{ENH} \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \tag{12}$$

The EN rising threshold (V_{ENH}) for the TPS2586x-Q1 is set to be 1.3 V (typical). Choose 10 kΩ for R_{ENB} to minimize input current from the supply. If the desired V_{IN} UVLO level is at 6 V, then the value of R_{ENT} can be calculated using 方程式 13:

$$R_{ENT} = \left(\frac{V_{IN\_RISING}}{V_{ENH}} - 1 \right) \times R_{ENB} \tag{13}$$

方程式 13 yields a value of 36.1 kΩ. The resulting falling UVLO threshold equals 5.5 V and can be calculated by 方程式 14, where EN hysteresis (V_{EN_HYS}) is 0.1 V (typical).

$$V_{IN\_FALLING} = \left(V_{ENH} - V_{EN\_HYS} \right) \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \tag{14}$$

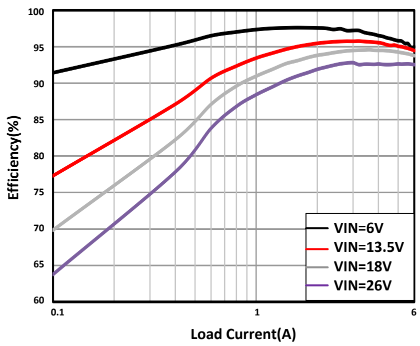
Note that it cannot connect EN to IN pin directly for self-startup. Because the voltage rating of EN pin is 11 V, tying it to VIN directly damages the device. The simplest way to enable the operation of the TPS2586x-Q1 is to connect the EN to V_{SENSE}. This connection allows the automatic startup when VIN is within the operation range.

11.2.2.8 Cable Compensation Set-Point

The TPS2586x-Q1 must short the VSET pin to ground to enable the cable compensation. With that setting, the buck regulator increases its output voltage linearly as the load current increases, and the voltage compensation at the currents of the USB ports greater than 2.4 A is 90 mV.

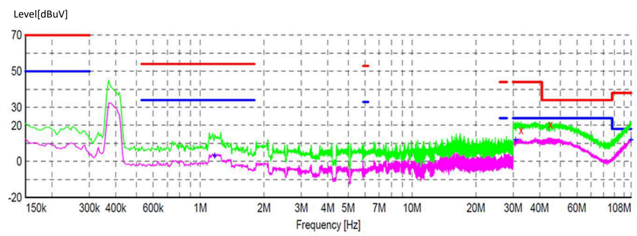
11.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 3.3 μH, C_{SENSE} = 141 μF, C_{PA_BUS} = 1 μF, C_{PB_BUS} = 1 μF, T_A = 25 °C.



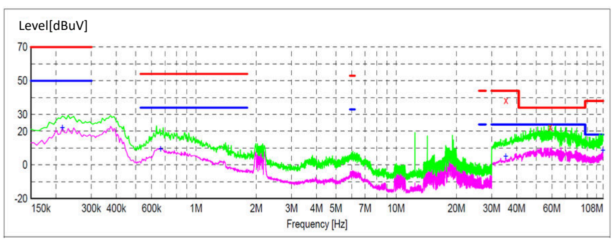
VSET = GND f_{SW} = 400 kHz L = 3.3 uH

图 11-2. Buck Only Efficiency



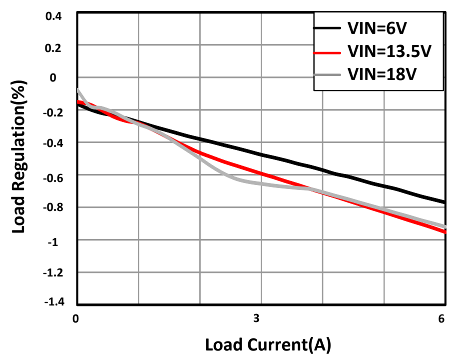
PA_BUS = 2.4A, PB_BUS = 2.4A f_{SW} = 400 kHz L = 3.3 uH

图 11-3. 400-khz EMI Results (Without CM Filter)



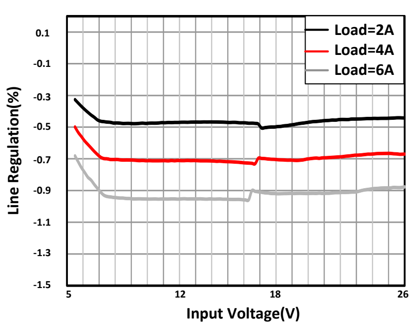
Load = 6A f_{SW} = 2100 kHz L = 0.68 uH

图 11-4. 2.1-Mhz EMI Results (Without CM Filter)



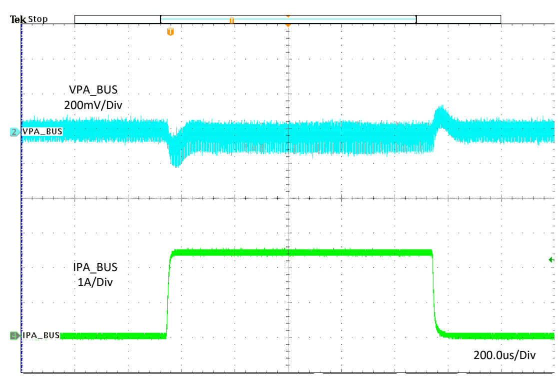
VSET = GND f_{SW} = 400 kHz

图 11-5. Load Regulation



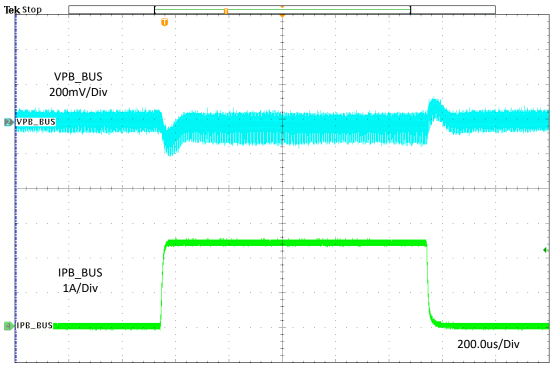
VSET = GND f_{SW} = 400 kHz

图 11-6. Line Regulation



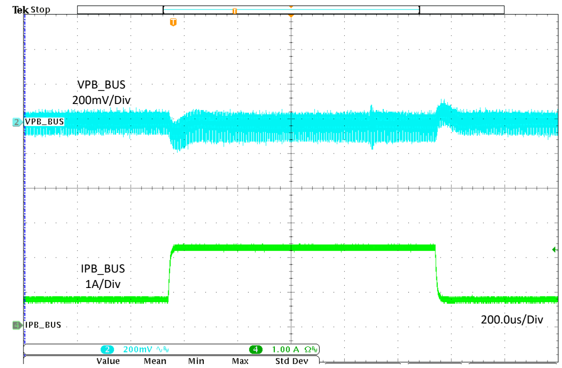
VSET = V_{SENSE} I_{PA_BUS} = 0 A to 2.4 A I_{PB_BUS} = 2.4 A f_{SW} = 400 KHZ

图 11-7. Load Transient Without Cable Compensation



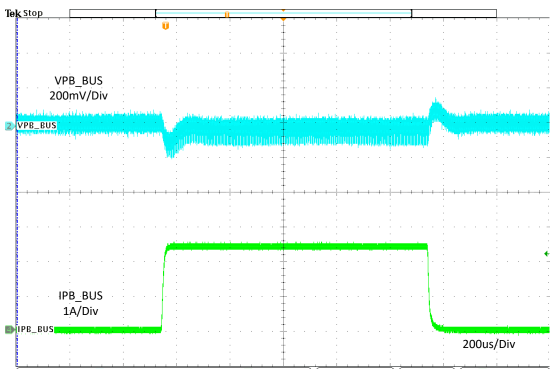
VSET = V_{SENSE} | I_{PB_BUS} = 0 A to 2.4 A | I_{PA_BUS} = 2.4 A | f_{SW} = 400 kHZ

图 11-8. Load Transient Without Cable Compensation



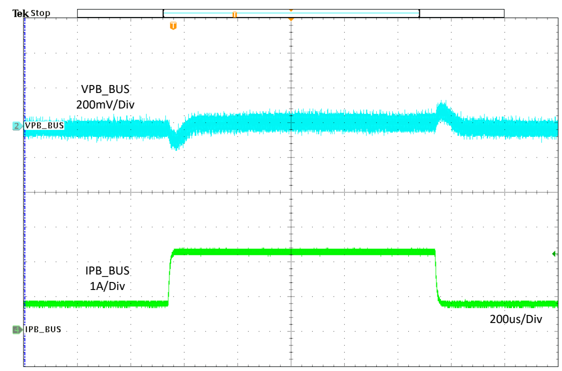
VSET = V_{SENSE} | I_{PB_BUS} = 0.75 A to 2.25 A | I_{PA_BUS} = 0 A | f_{SW} = 400 kHZ

图 11-9. Load Transient Without Cable Compensation



VSET = GND | I_{PB_BUS} = 0 A to 2.4 A | I_{PA_BUS} = 2.4 A | f_{SW} = 400 kHZ

图 11-10. Load Transient With Cable Compensation



VSET = GND | I_{PB_BUS} = 0.75 A to 2.25 A | I_{PA_BUS} = 0 A | f_{SW} = 400 kHZ

图 11-11. Load Transient With Cable Compensation

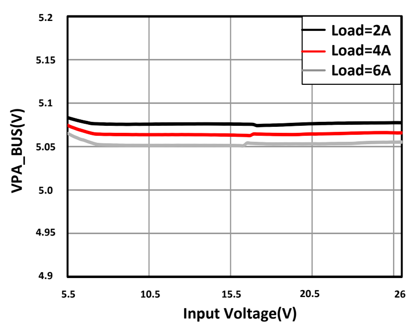
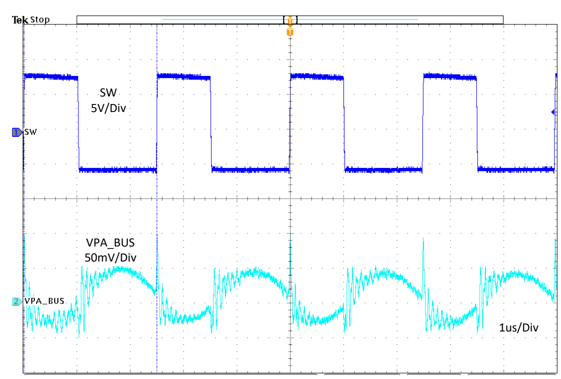
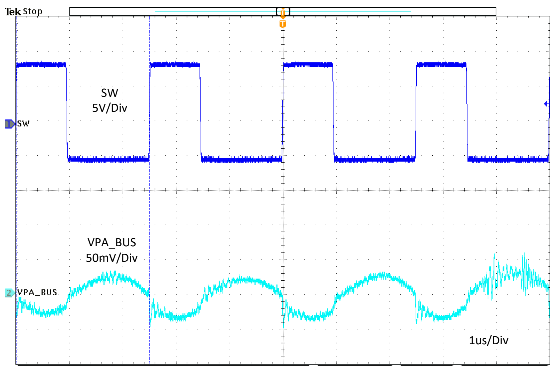


图 11-12. Dropout Characteristic



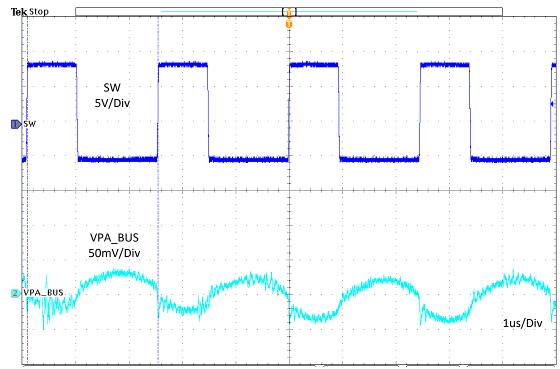
VSET = GND | I_{PA_BUS} = 2.4 A | I_{PB_BUS} = 2.4 A | f_{SW} = 400 kHZ

图 11-13. 4.8-A Output Ripple



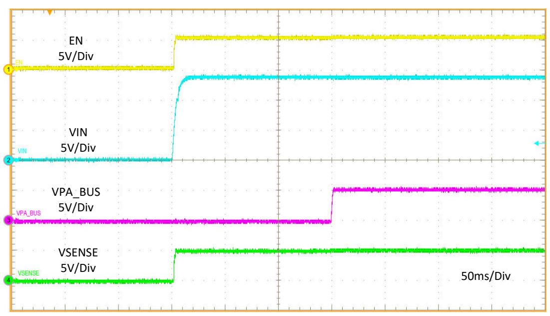
VSET = GND I_{PA_BUS} = 0.1 A I_{PB_BUS} = 0 A f_{SW} = 400 kHZ

图 11-14. 100-mA Output Ripple



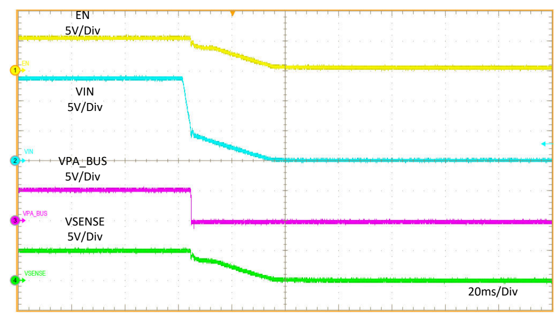
VSET = GND I_{PA_BUS} = 0 A I_{PB_BUS} = 0 A f_{SW} = 400 kHZ

图 11-15. No Load Output Ripple



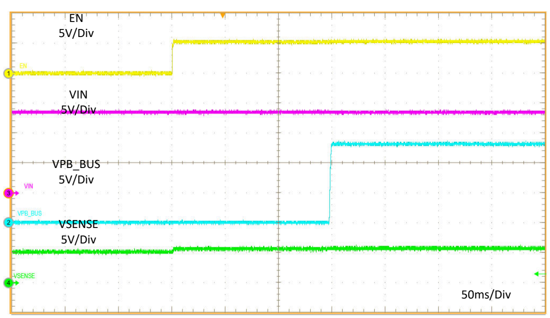
VIN = 0 V to 13.5 I_{PA_BUS} = 2.4 A

图 11-16. Startup Relate to VIN



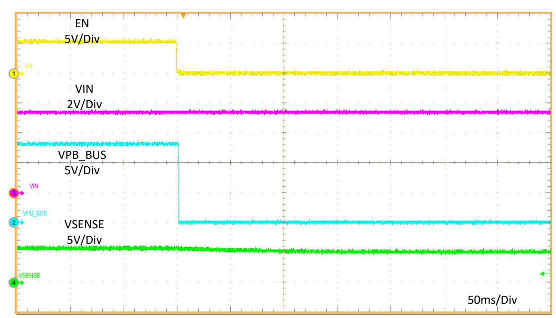
VIN = 13.5 V to 0 V I_{PA_BUS} = 2.4 A

图 11-17. Shutdown Relate to VIN



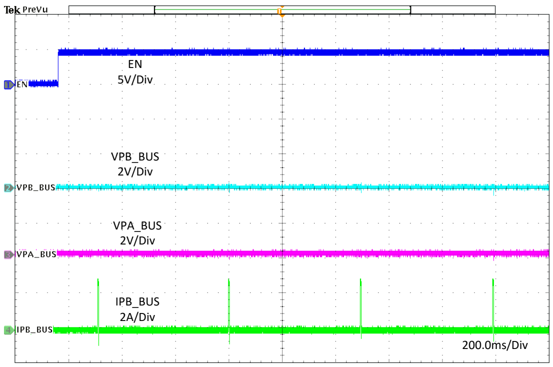
EN = 0 V to 5 V I_{PB_BUS} = 2.4 A

图 11-18. Startup Relate to EN



EN = 5 V to 0 V I_{PB_BUS} = 2.4 A

图 11-19. Shutdown Relate to EN



EN to High PA_BUS = GND PB_BUS = GND

图 11-20. Enable Into Short

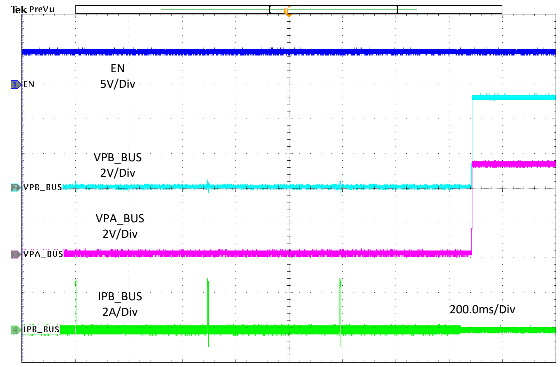
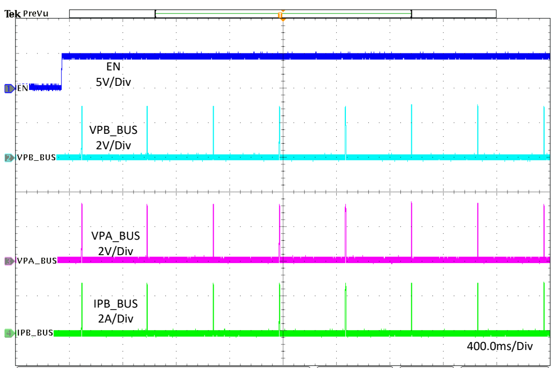


图 11-21. Short Circuit Recovery



EN to High PA_BUS = 1 Ω PB_BUS = 1 Ω

图 11-22. Enable Into 1-Ω Load

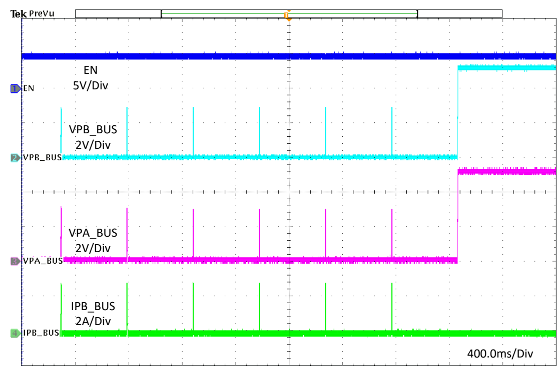


图 11-23. 1-Ω Load Recovery

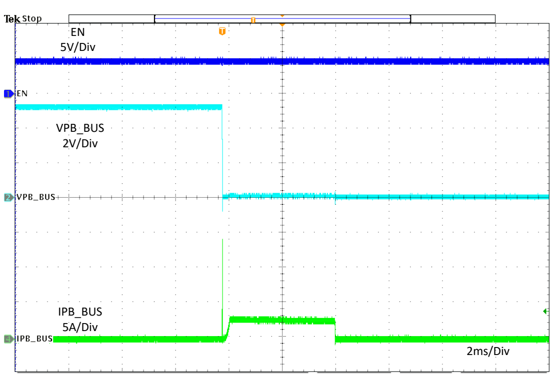
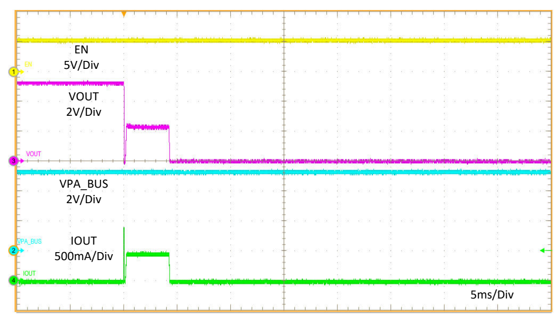
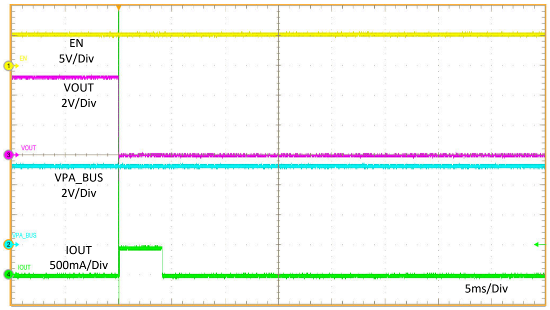


图 11-24. VBUS Hot Short to GND



OUT = 5.1 Ω PA/B_BUS NO LOAD

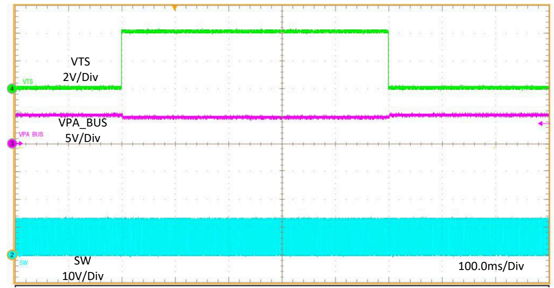
图 11-25. OUT short to 5.1-Ω Load



OUT = GND

PA/B_BUS NO LOAD

图 11-26. OUT Hot Short to GND



V_{TS} = 0 V to 4 V

图 11-27. Thermal Sensing - NTC Temperature HOT Behavior

12 Power Supply Recommendations

The input supply must be able to withstand the maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the TPS2586x-Q1 supply voltage that it causes a false UVLO fault triggering and system reset. If the TPS2586x-Q1 is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. An additional bulk capacitance can be required in addition to the ceramic input capacitors. The amount of bulk capacitance is not critical, but a 100-μF electrolytic capacitor is a typical choice.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharge through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then a Schottky diode between the input supply and the output must be used.

13 Layout

13.1 Layout Guidelines

The PCB layout of any bulk converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the converter is dependent on the PCB layout to a great extent. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The input bypass capacitor, C_{IN}, must be placed as close as possible to the IN and PGND pins. The high frequency ceramic bypass capacitors at the input side provide a primary path for the high di/dt components of the pulsing current. Use a wide VIN plane on a lower layer to connect both of the VIN pairs together to the input supply. Grounding for both the input and output capacitors must consist of localized top-side planes that connect to the PGND pin and PAD.
2. Use ground plane in one of the middle layers as noise shielding and heat dissipation path.
3. Use wide traces for the C_{BOOT} capacitor. Place the C_{BOOT} capacitor as close to the device with short, wide traces to the BOOT and SW pins.
4. The SW pin connecting to the inductor must be as short as possible, and just wide enough to carry the load current without excessive heating. Short, thick traces or copper pours (shapes) must be used for a high current conduction path to minimize parasitic resistance. The output capacitors must be placed close to the V_{SENSE} end of the inductor and closely grounded to PGND pin and exposed PAD.
5. R_{FREQ} resistors must be placed as close as possible to the FREQ pins and connected to AGND. If needed, these components can be placed on the bottom side of the PCB with signals routed through small vias, and the traces need far away from noisy nets like SW, BOOT.
6. Make V_{IN}, V_{SENSE}, and ground bus connections as wide as possible. This action reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
7. Provide enough PCB area for proper heat sinking. Enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with 2-ounce copper; and no less than 1 ounce. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes. Note that the package of this device dissipates heat through all pins. Wide traces must be used for all pins except where noise considerations dictate minimization of area.
8. Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 150°C.

13.2 Layout Example

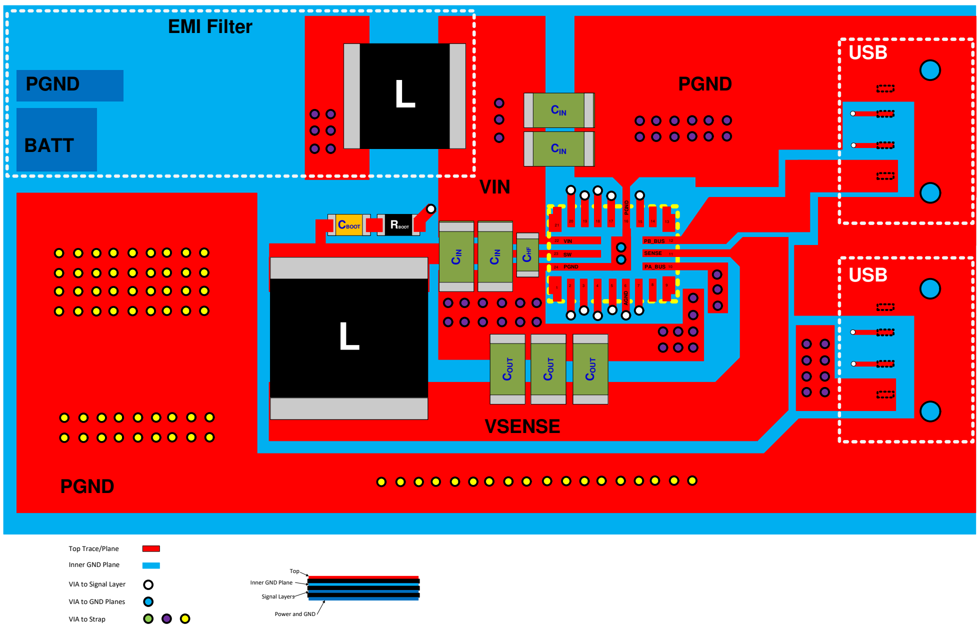


图 13-1. Layout Example

13.3 Ground Plane and Thermal Considerations

TI recommends to use one of the middle layers as a solid ground plane. Ground plane provides shielding for sensitive circuits and traces. Ground plane also provides a quiet reference potential for the control circuitry. The AGND and PGND pins must be connected to the ground plane using vias right next to the bypass capacitors. The PGND pin is connected to the source of the internal low-side MOSFET switch, and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as VIN and SW traces, must be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and must be used for sensitive routes.

TI recommends to provide adequate device heat sinking by using the PAD of the IC as the primary thermal path. Use a minimum 4 × 2 array of 12-mil thermal vias to connect the PAD to the system ground plane heat sink. The vias must be evenly distributed under the PAD. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top of 2 oz / 1 oz / 1 oz / 2 oz. Four layer boards with enough copper thickness provide low current conduction impedance, proper shielding, and lower thermal resistance.

The thermal characteristics of the TPS2586x-Q1 are specified using the parameter θ_{JA}, which characterizes the junction temperature of silicon to the ambient temperature in a specific system. Although the value of θ_{JA} is dependent on many variables, it still can be used to approximate the operating junction temperature of the device. To obtain an estimate of the device junction temperature, one can use the following relationship:

$$T_J = P_D \times \theta_{JA} + T_A \tag{15}$$

where

- T_J = Junction temperature in °C
- $P_D = V_{IN} \times I_{IN} \times (1 - \text{Efficiency}) - 1.1 \times I_{OUT}{}^2 \times DCR$ in Watt
- DCR = Inductor DC parasitic resistance in Ω
- θ_{JA} = Junction-to-ambient thermal resistance of the device in °C/W
- T_A = Ambient temperature in °C

The maximum operating junction temperature of the TPS2586x-Q1 is 150°C. θ_{JA} is highly related to PCB size and layout, as well as environmental factors such as heat sinking and air flow.

14 Device and Documentation Support

14.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

14.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

14.3 Trademarks

HotRod™ and TI E2E™ are trademarks of Texas Instruments.
所有商标均为其各自所有者的财产。

14.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com/legal/termsofsale.html) 或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25864QRPQRQ1	Active	Production	VQFN-HR (RPQ) | 25	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-45 to 125	T25864
TPS25864QRPQRQ1.A	Active	Production	VQFN-HR (RPQ) | 25	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-45 to 125	T25864
TPS25865QRPQRQ1	Active	Production	VQFN-HR (RPQ) | 25	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	T25865
TPS25865QRPQRQ1.A	Active	Production	VQFN-HR (RPQ) | 25	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	T25865

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

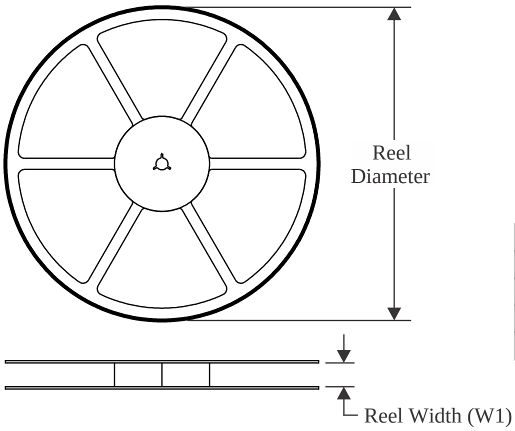
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

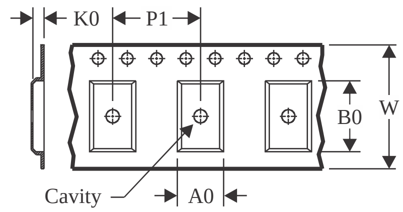
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

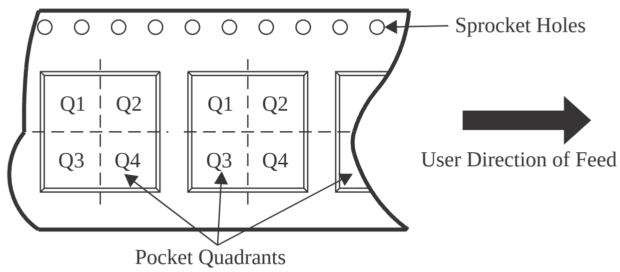


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

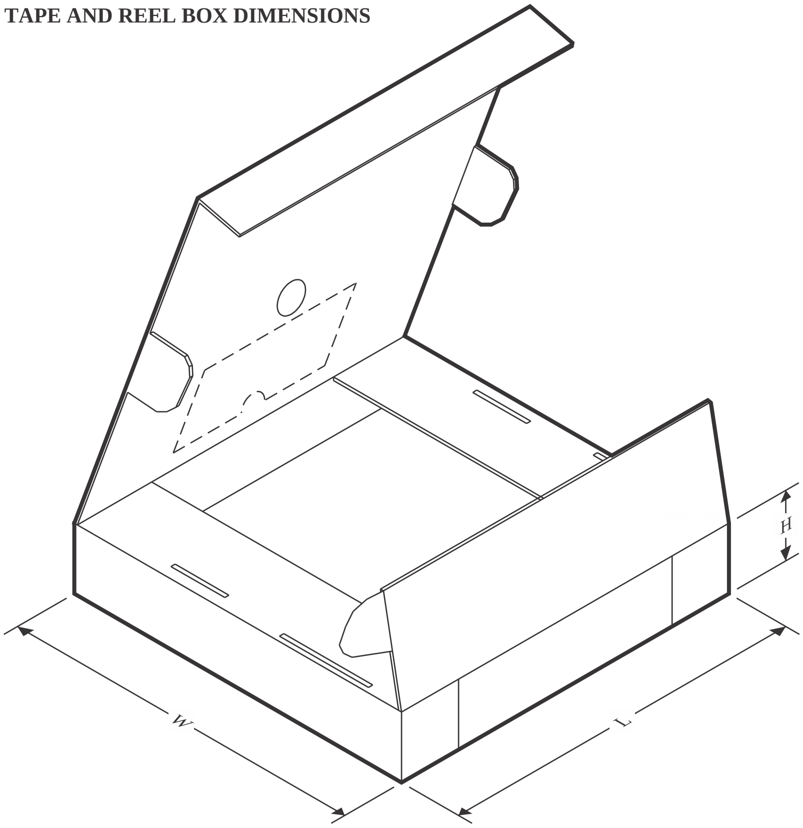
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25864QRPQRQ1	VQFN-HR	RPQ	25	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1
TPS25865QRPQRQ1	VQFN-HR	RPQ	25	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

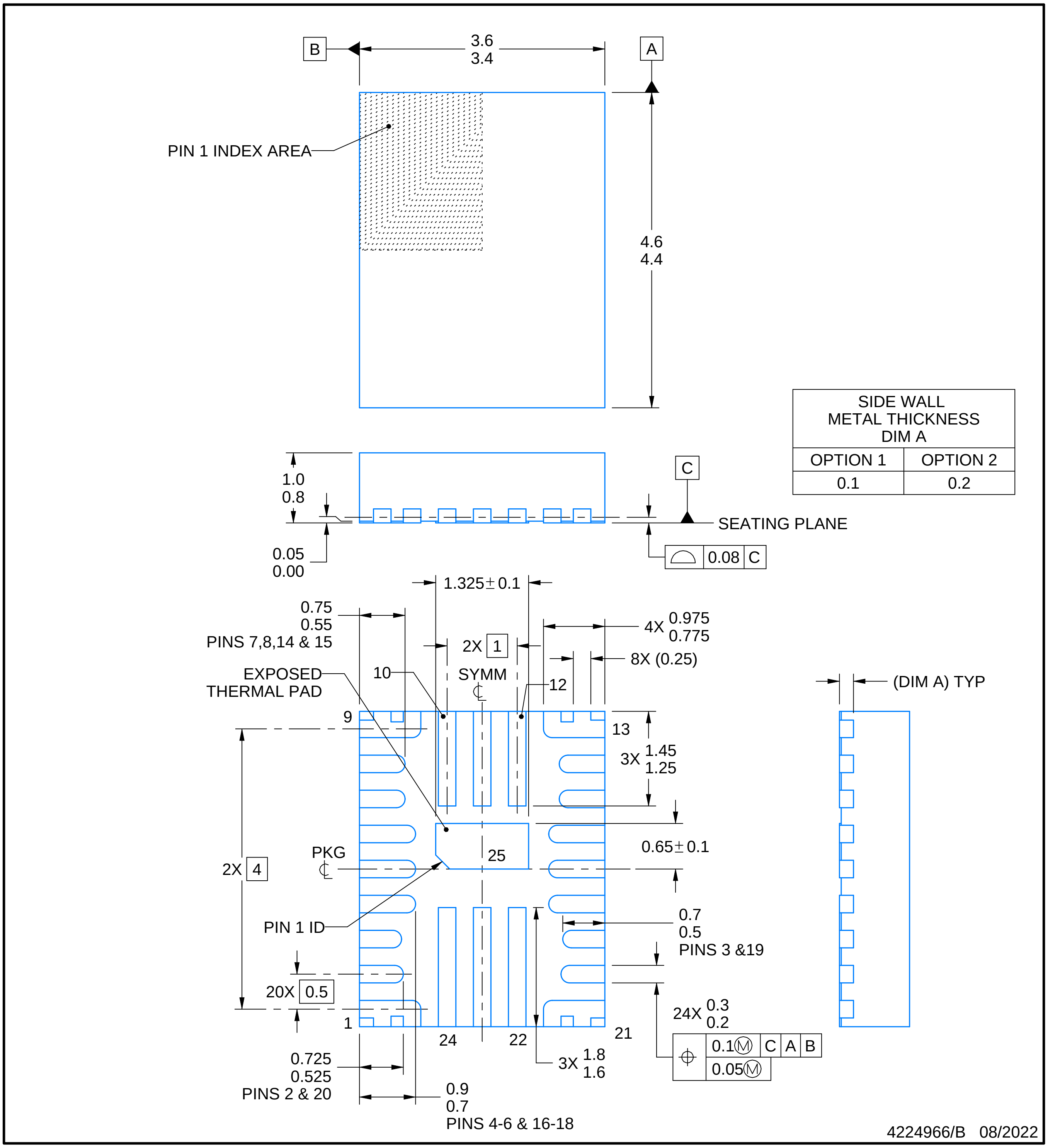
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25864QRPQRQ1	VQFN-HR	RPQ	25	3000	367.0	367.0	38.0
TPS25865QRPQRQ1	VQFN-HR	RPQ	25	3000	367.0	367.0	38.0

PACKAGE OUTLINE

RPQ0025A

VQFN - 1 mm max height

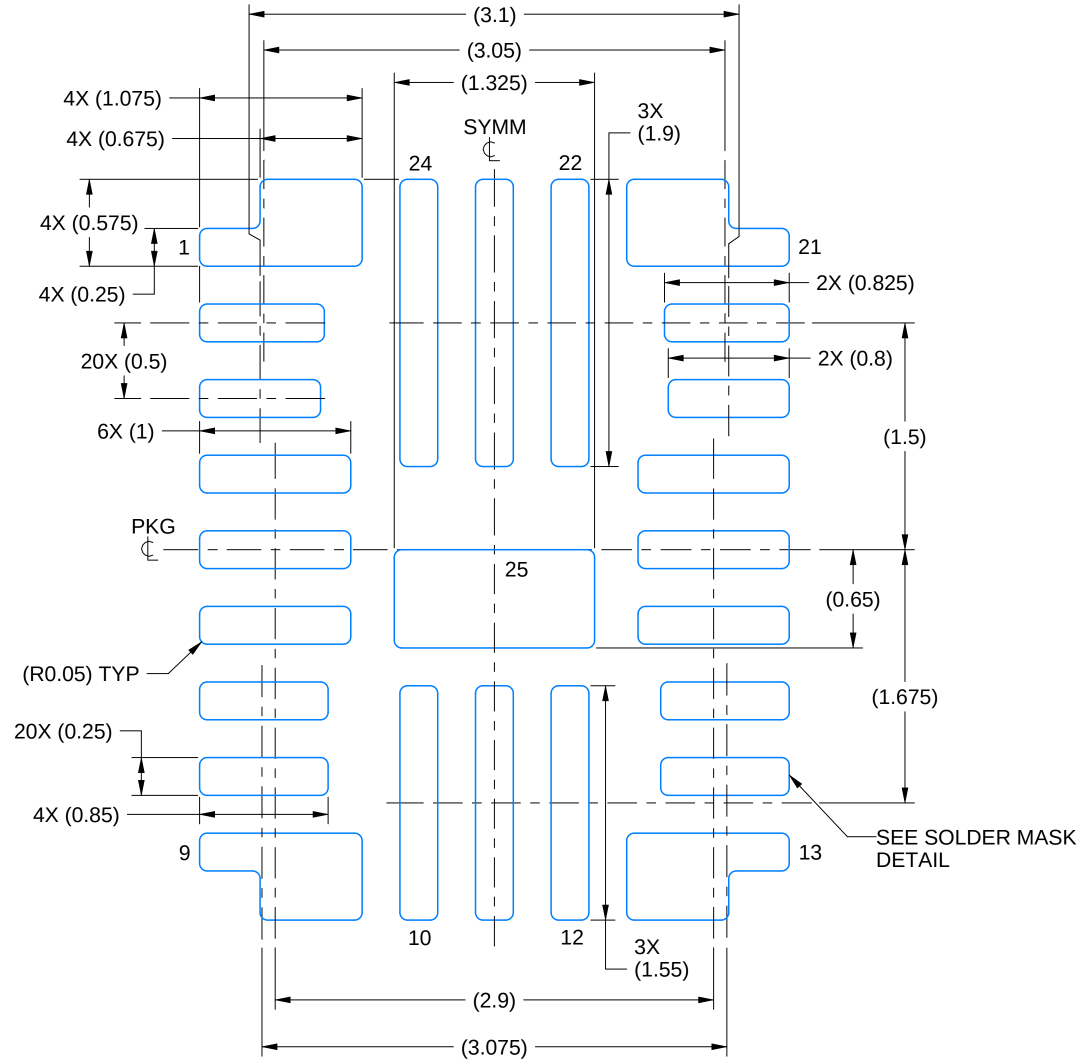
PLASTIC QUAD FLATPACK - NO LEAD



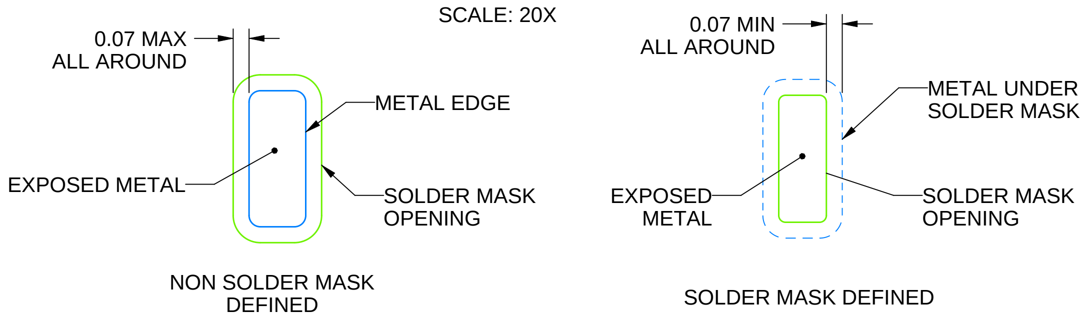
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

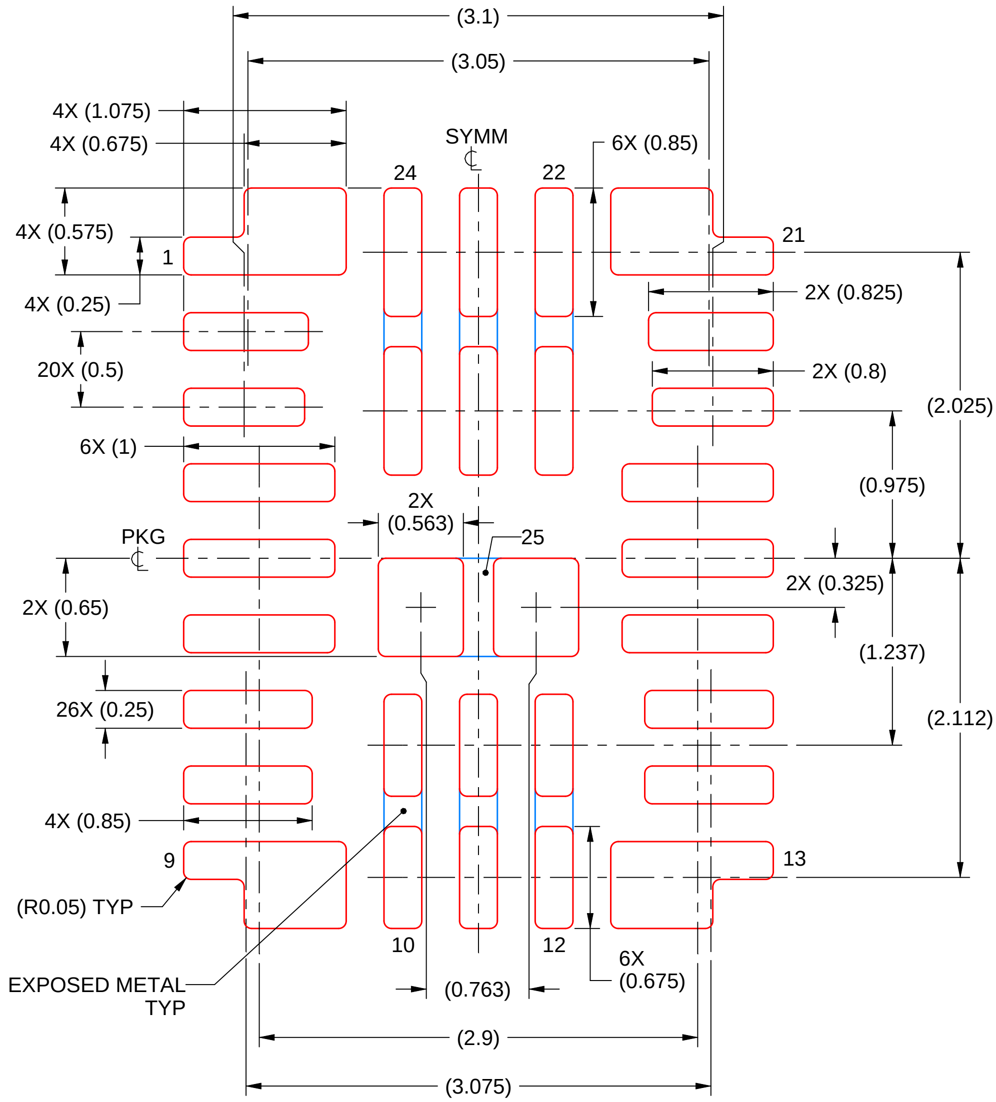


SOLDER MASK DETAILS

4224966/B 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 25
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224966/B 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265