

General Description

The LTA8181, LTA8182 and LTA8184 (LTA818x) are a family of zero-drift, low power, rail-to-rail output operational amplifiers capable of operating on wide supplies ranging from +4.5 V (± 2.25 V) to +48 V (± 24 V). The LTA818x op-amps use Linearin's proprietary auto-zeroing techniques to offer outstanding dc precision and ac performance, including low offset voltage (25 μ V maximum), near zero-drift over time and temperature, 4 MHz bandwidth, and 0.32 μ V_{PP} input voltage noise at 0.1 Hz to 10 Hz. These high-precision, low-quiescent-current op-amps offer high input impedance and rail-to-rail output swing within 10 mV of the rails. The input common-mode range includes the negative rail.

The single version LTA8181 device is available in micro-size MSOP-8L, SOT-23-5L, and SOIC-8L packages. The dual version LTA8182 device is offered in MSOP-8L and SOIC-8L packages. The quad version LTA8184 device is offered in SOIC-14L and TSSOP-14L packages. All versions are specified for operation from -40°C to $+125^{\circ}\text{C}$.

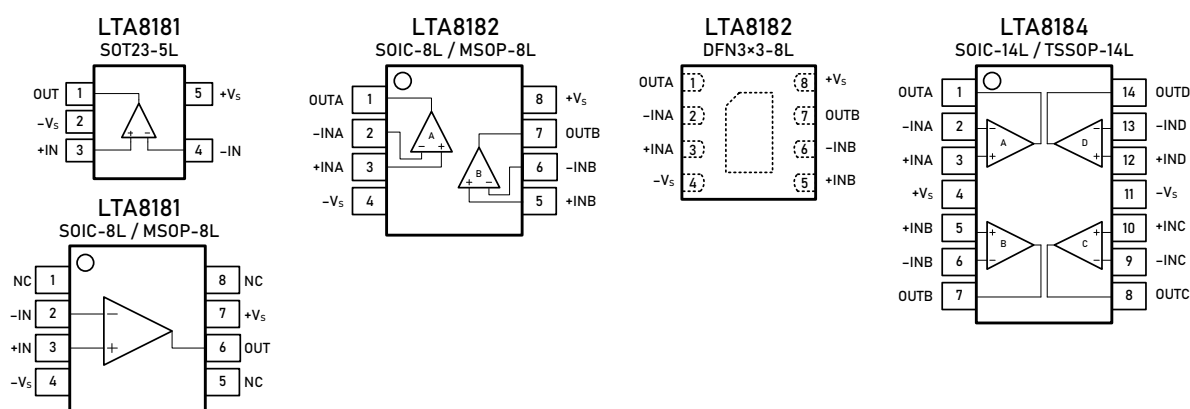
Features and Benefits

- High DC Precision
 - ± 25 μ V (maximum) V_{OS} with a Drift of ± 50 nV/ $^{\circ}\text{C}$
 - CMRR: 132 dB
 - PSRR: 135 dB
 - A_{VOL} : 136 dB
 - V_n : 0.32 μ V_{PP} (0.1 to 10 Hz)
- Wide Supply: ± 2.25 V to ± 24 V, 4.5 V to 48 V
- Gain Bandwidth: 4 MHz
- Slew Rate: 2.6 V/ μ s
- Low Quiescent Current: 600 μ A per amplifier
- Low Bias Current: ± 150 pA
- Rail-to-Rail Output Operation

Applications

- High-Side and Low-Side Current Sensing
- Transducer Amplifiers
- Precision Active Filters
- Programmable Logic Controllers
- Test and Measurement Equipment
- Multiplexed Data-Acquisition Systems
- Tracking Amplifier in Power Modules
- Power Delivery: UPS, Server, and Merchant Network Power

Pin Configuration (Top View)



Pin Description

Symbol	Description
-IN	Inverting input of the amplifier. The voltage range is from V_{S-} to $V_{S+} - 1.5$ V.
+IN	Non-inverting input of the amplifier. This pin has the same voltage range as -IN.
+V _S	Positive power supply. The voltage is from 4.5 V to 48 V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is from 4.5 V to 48 V.
-V _S	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 4.5 V to 48 V.
OUT	Amplifier output.
NC	No connection

Ordering Information ⁽¹⁾

Type Number	Package Name	Package Quantity	Eco Class ⁽²⁾	Marking Code ⁽³⁾
LTA8181XT5/R6	SOT23-5L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	Z81
LTA8181XS8/R8	SOIC-8L	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	ZHV81
LTA8181XV8/R6	MSOP-8L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	ZHV81
LTA8182XS8/R8	SOIC-8L	Tape and Reel, 4 000	Green (RoHS & no Sb/Br)	ZHV82
LTA8182XV8/R6	MSOP-8L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	ZHV82
LTA8182XF8/R6	DFN3x3-8L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	ZHV82
LTA8184XS14/R5	SOIC-14L	Tape and Reel, 2 500	Green (RoHS & no Sb/Br)	ZHV84
LTA8184XT14/R6	TSSOP-14L	Tape and Reel, 3 000	Green (RoHS & no Sb/Br)	ZHV84

(1) Please contact to your Linearin representative for the latest availability information and product content details.

(2) Eco Class - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & Halogen Free).

(3) There may be multiple device markings, a varied marking character of "x" , or additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

Limiting Value – In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Absolute Maximum Rating
Supply Voltage, V_{S+} to V_{S-}	60 V
Signal Input Terminals: Voltage, Current	$-V_S - 0.3$ V to $+V_S + 0.3$ V, ± 10 mA
Output Short-Circuit	Continuous
Storage Temperature Range, T_{stg}	-65 to $+150$ °C
Junction Temperature, T_J	150 °C
Lead Temperature Range (Soldering 10 sec)	260 °C

ESD Rating

Parameter	Item	Value	Unit
Electrostatic Discharge Voltage	Human body model (HBM), per MIL-STD-883J / Method 3015.9 ⁽¹⁾	2 000	V
	Charged device model (CDM), per ESDA/JEDEC JS-002-2014 ⁽²⁾	2 000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

Electrical Characteristics

$V_S = 4.5 \text{ V to } 48 \text{ V}$, $T_A = +25 \text{ }^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S/2$, and $R_L = 10 \text{ k}\Omega$ connected to $V_S/2$, unless otherwise noted. Boldface limits apply over the specified temperature range, $T_A = -40 \text{ }^\circ\text{C to } +125 \text{ }^\circ\text{C}$.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
OFFSET VOLTAGE						
Input offset voltage	V _{OS}			±8	±25	μV
Offset voltage drift	V _{OS} TC	T _A = −40 to +125 °C		±50		μV/°C
Power supply rejection ratio	PSRR	V _S = 4.5 to 48 V, V _{CM} = 0.1 V		135		dB
		T _A = −40 to +125 °C		122		
INPUT BIAS CURRENT						
Input bias current	I _B			150		pA
		T _A = +85 °C		600		
		T _A = +125 °C		3000		
Input offset current	I _{OS}			300		pA
NOISE						
Input voltage noise	V _n	f = 0.1 to 10 Hz		0.32		μV _{P-P}
Input voltage noise density	e _n	f = 1 kHz		15		nV/√Hz
		f = 10 kHz		15		
Input current noise density	I _n	f = 1 kHz		10		fA/√Hz
INPUT VOLTAGE						
Common-mode voltage range	V _{CM}		−V _S		+V _S −1.5	V
Common-mode rejection ratio	CMRR	V _{S−} < V _{CM} < V _{S+} −1.5 V		132		dB
		V _{S−} +0.5 < V _{CM} < V _{S+} −1.5 V		143		
		V _{S−} +0.5 < V _{CM} < V _{S+} −1.5 V, V _S = ±20 V, T _A = −40 to +125 °C		124		
INPUT IMPEDANCE						
Input capacitance	C _{IN}	Differential		3		pF
		Common mode		4.5		
OPEN-LOOP GAIN						
Open-loop voltage gain	A _{VOL}	V _{S−} +0.5 < V _O < V _{S+} −0.5 V		136		dB
		V _{S−} +0.5 < V _O < V _{S+} −0.5 V, T _A = −40 to +125 °C		126		
FREQUENCY RESPONSE						
Gain bandwidth product	GBW			4		MHz
Slew rate	SR	G = +1		2.6		V/μs
Total harmonic distortion + noise	THD+N	G = +1, f = 1 kHz, V _O = 3 V _{RMS}		0.0001		%
Settling time	t _S	To 0.1%, V _S = 40 V, G = +1, 5 V step		5		μs
		To 0.01%, V _S = 40 V, G = +1, 5 V step		8		
Overload recovery time	t _{OR}	V _{IN} × Gain > V _S		1.5		μs

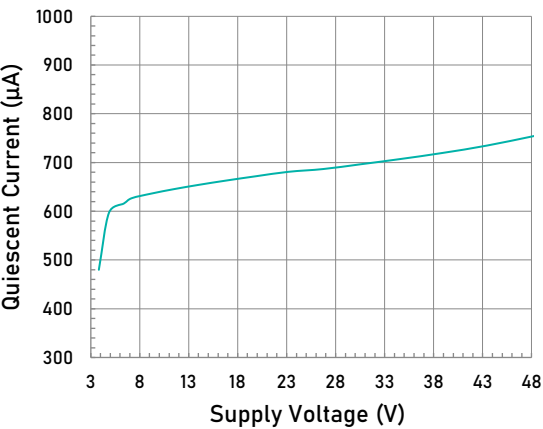
Electrical Characteristics (continued)

$V_S = 4.5\text{ V to }48\text{ V}$, $T_A = +25\text{ }^{\circ}\text{C}$, $V_{CM} = V_{OUT} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, unless otherwise noted.
Boldface limits apply over the specified temperature range, $T_A = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$.

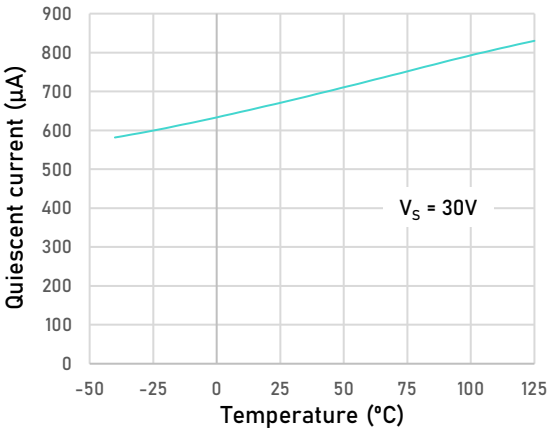
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
OUTPUT						
High output voltage swing	V _{OH}	R _L = 10 kΩ		+V _S -100		mV
		R _L = 2 kΩ		+V _S -270		
Low output voltage swing	V _{OL}	R _L = 10 kΩ		-V _S +60		mV
		R _L = 2 kΩ		-V _S +250		
Short-circuit current	I _{SC}			±45		mA
POWER SUPPLY						
Operating supply voltage	V _S	T _A = -40 to +125 °C	4.5		48	V
Quiescent current (per amplifier)	I _q	V _S = 5 V		600		μA
		V _S = 36 V		690		
THERMAL CHARACTERISTICS						
Operating temperature range	T _A		-40		+125	°C
Package Thermal Resistance	θ _{JA}	SOT23-5L		190		°C/W
		MSOP-8L		201		
		SOIC-8L		125		
		TSSOP-14L		112		
		SOIC-14L		115		

Typical Performance Characteristics

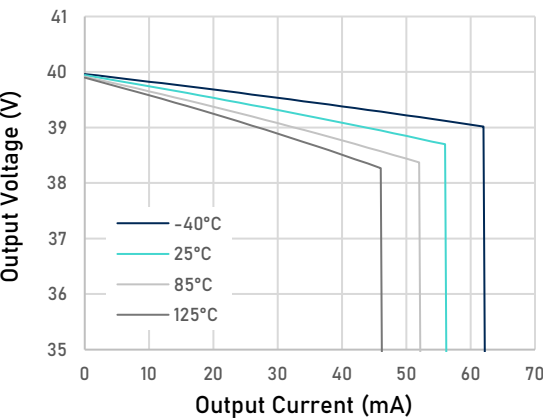
At $T_A = +25^\circ\text{C}$, $V_{CM} = V_S/2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, unless otherwise noted.



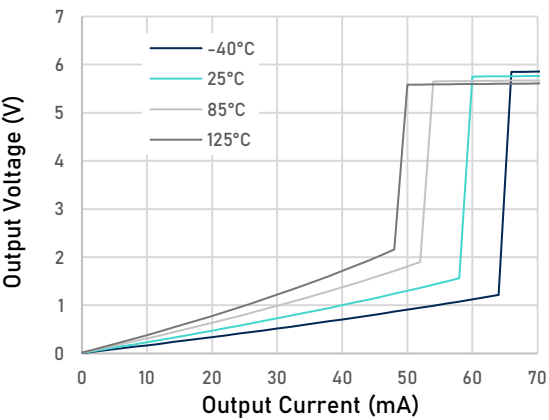
Quiescent Current as a function of Supply Voltage



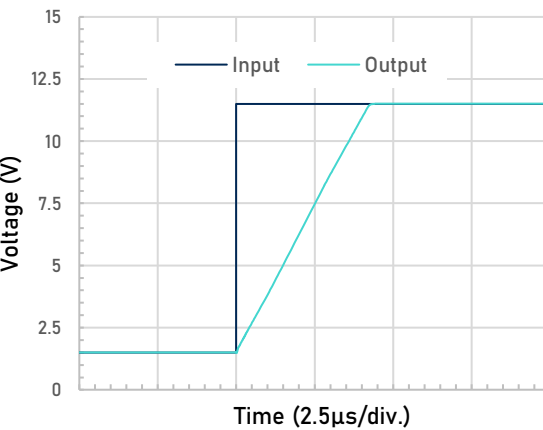
Quiescent Current as a function of Temperature



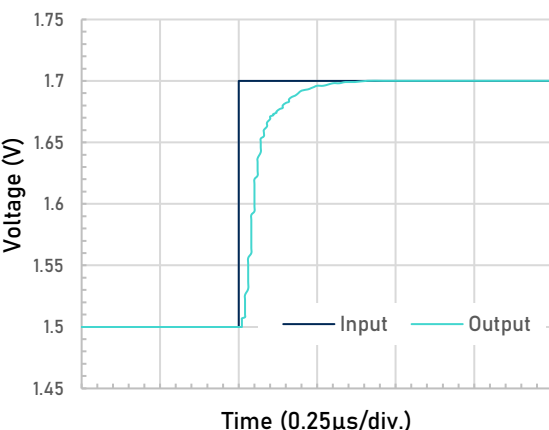
Output Voltage Swing as a function of Output Current (Sourcing, $V_S = 40\text{ V}$)



Output Voltage Swing as a function of Output Current (Sinking, $V_S = 40\text{ V}$)



Large-Signal Step Response(Failing)



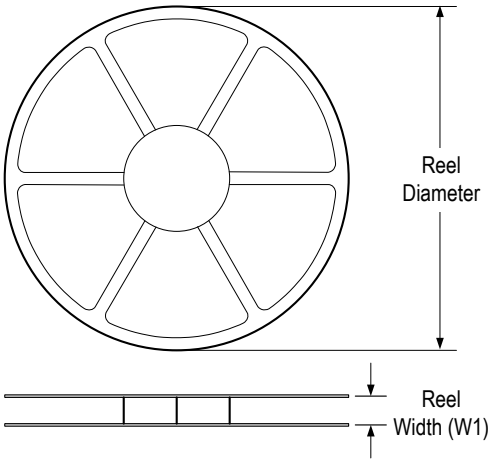
Small-Signal Step Response

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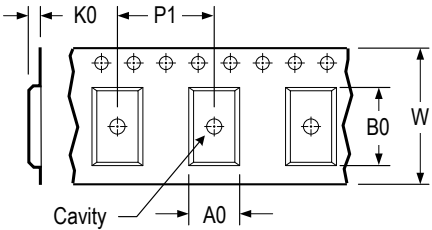


Tape and Reel Information

REEL DIMENSIONS

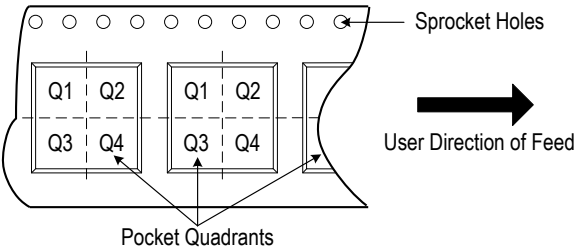


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

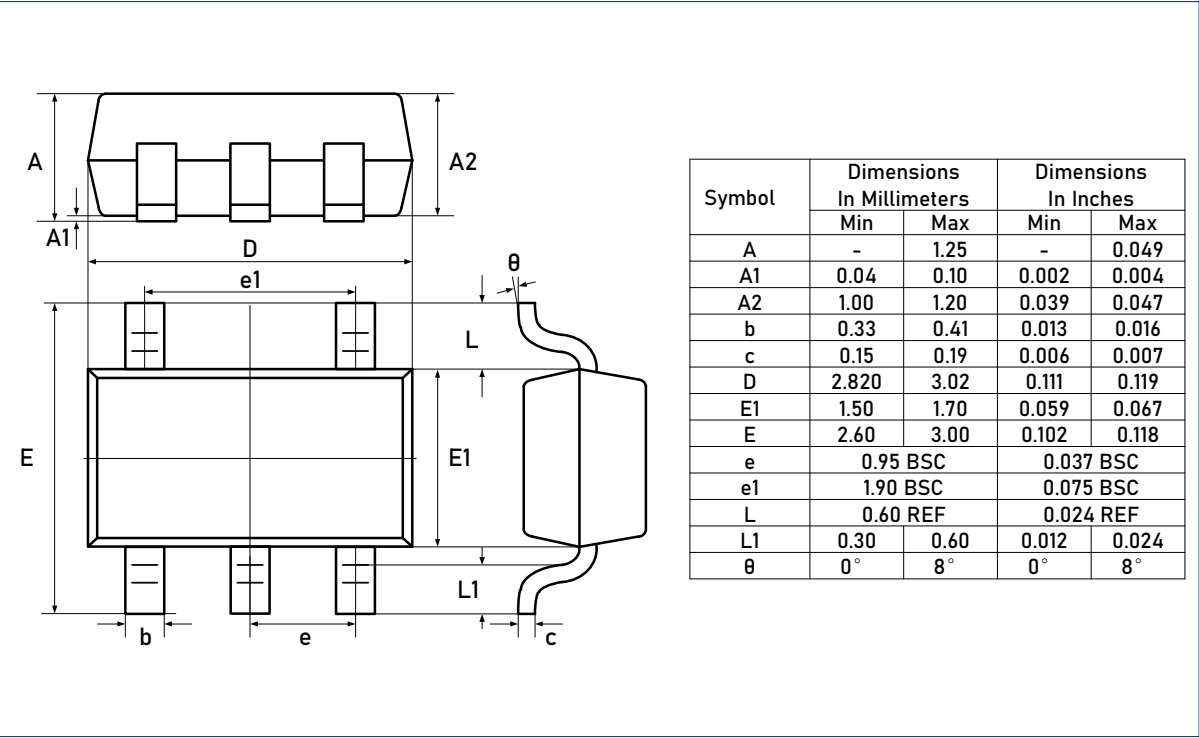


* All dimensions are nominal

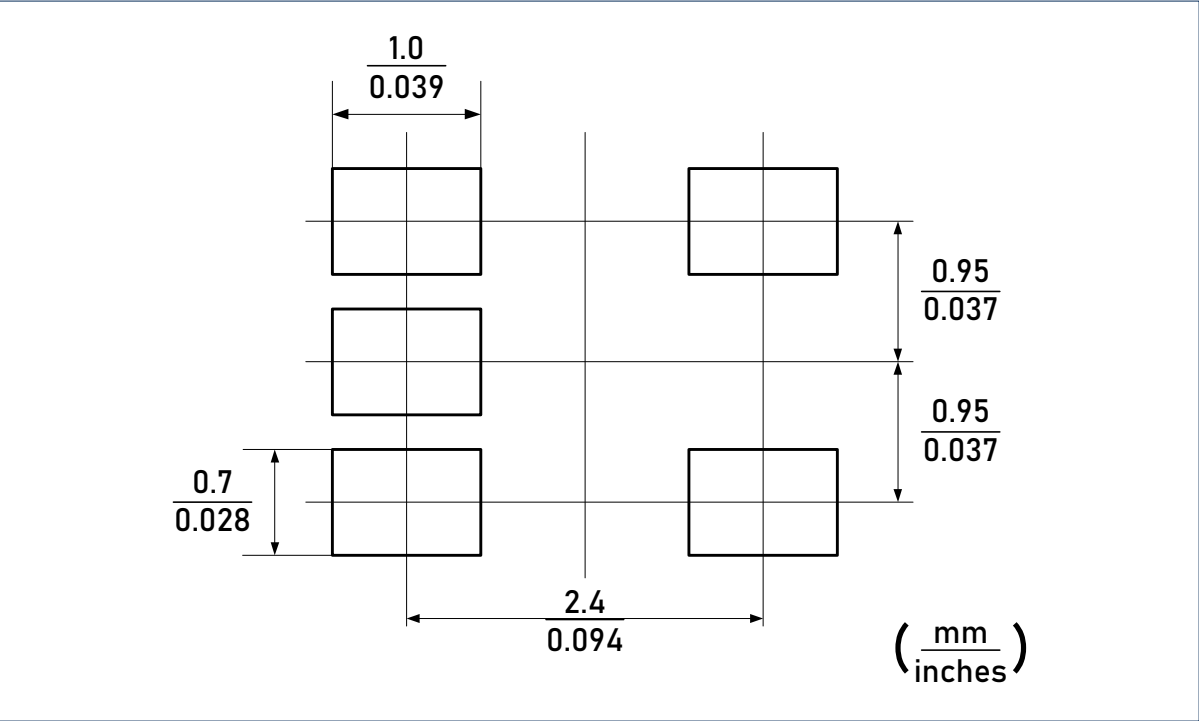
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
LTA8181XT5/R6	SOT23	5	3 000	178	9.0	3.3	3.2	1.5	4.0	8.0	Q3

Package Outlines

DIMENSIONS, SOT23-5L



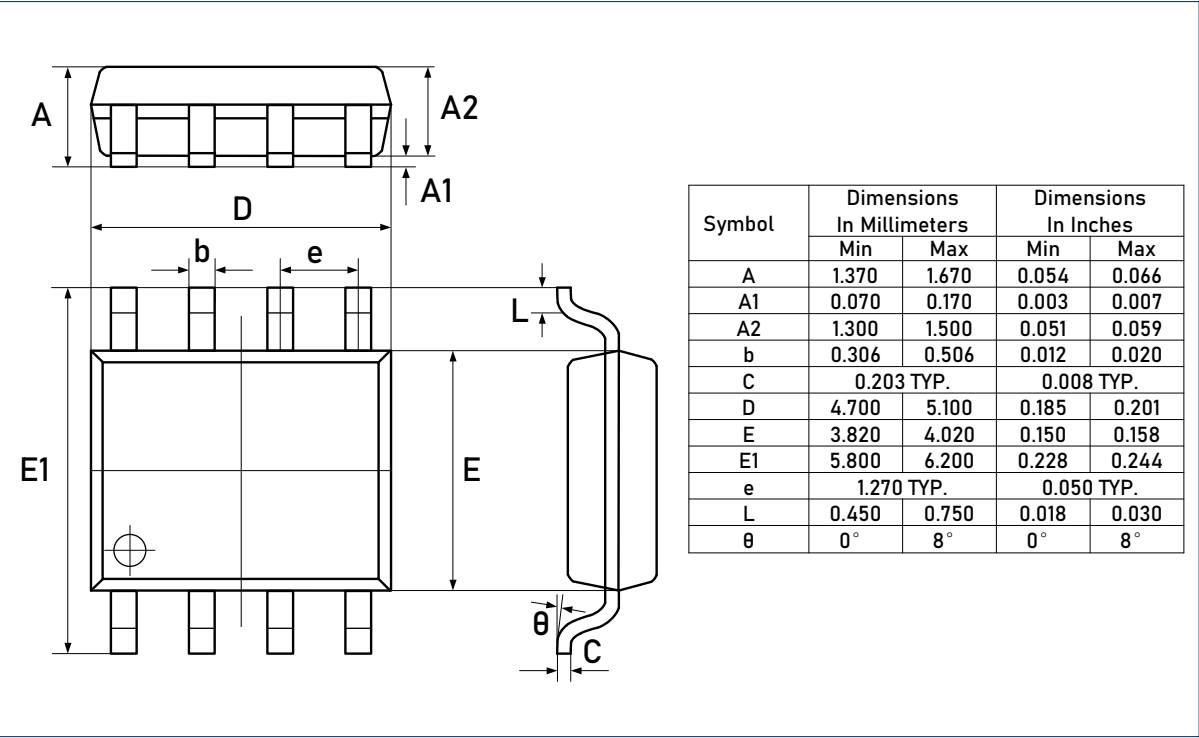
RECOMMENDED SOLDERING FOOTPRINT, SOT23-5L



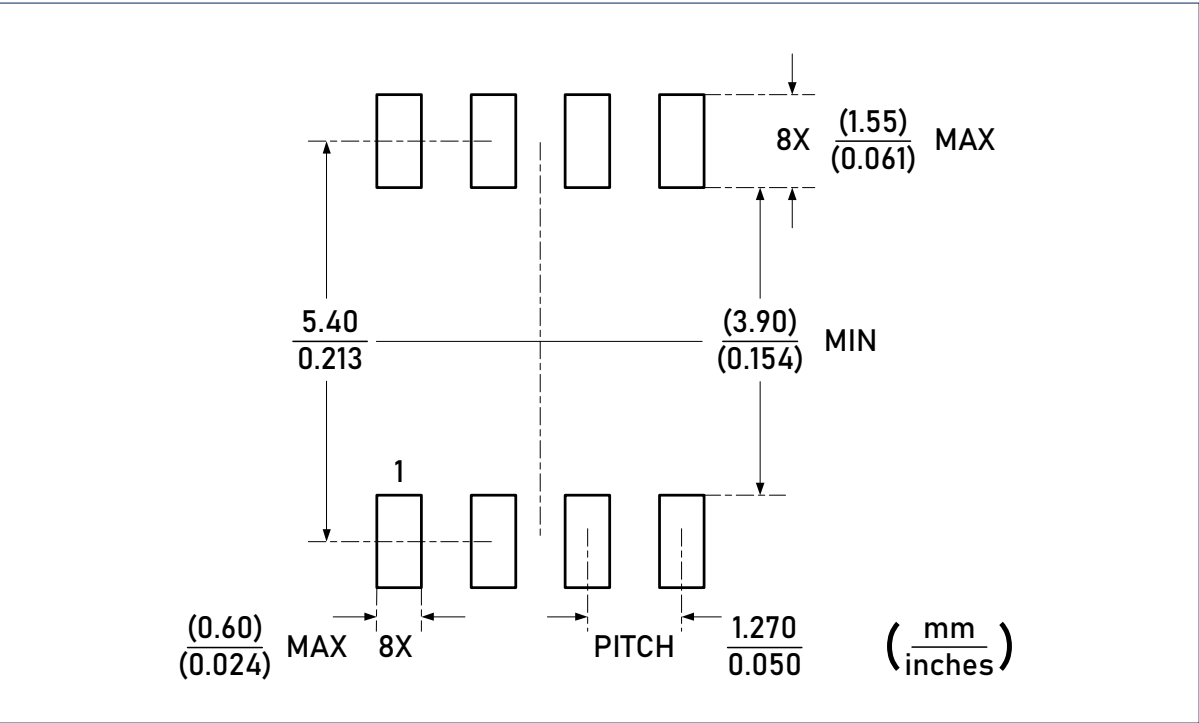
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Package Outlines (continued)

DIMENSIONS, SOIC-8L



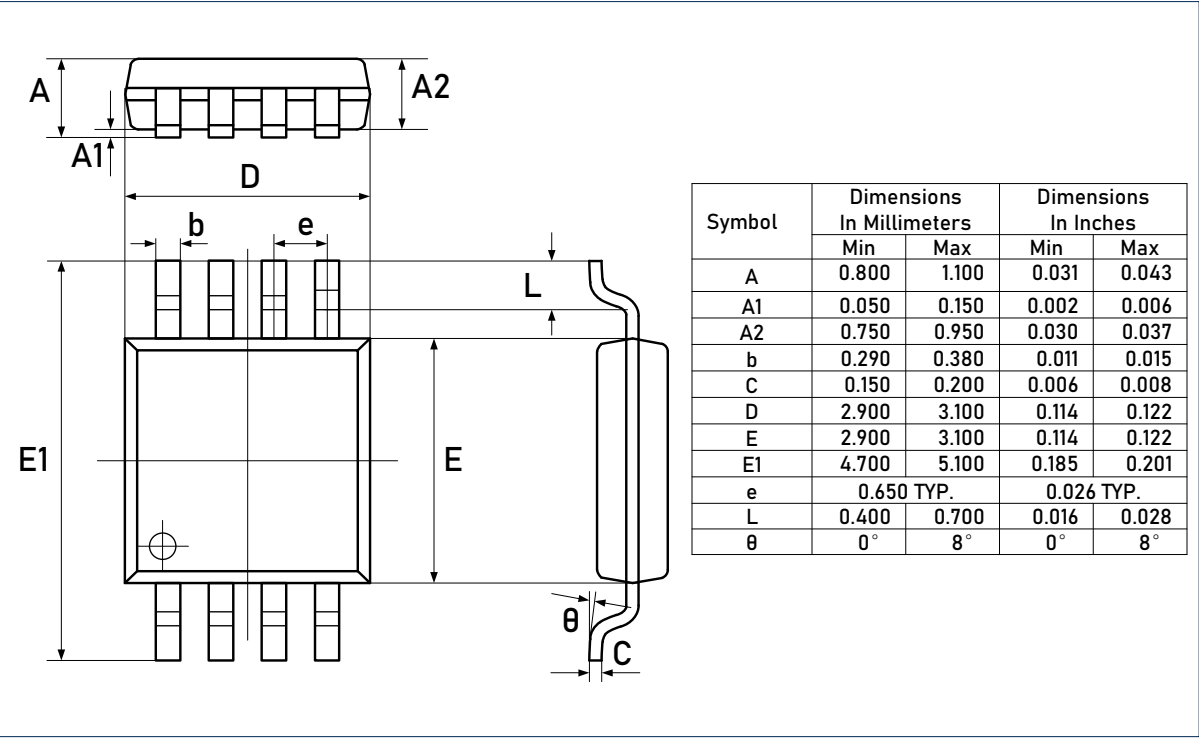
RECOMMENDED SOLDERING FOOTPRINT, SOIC-8L



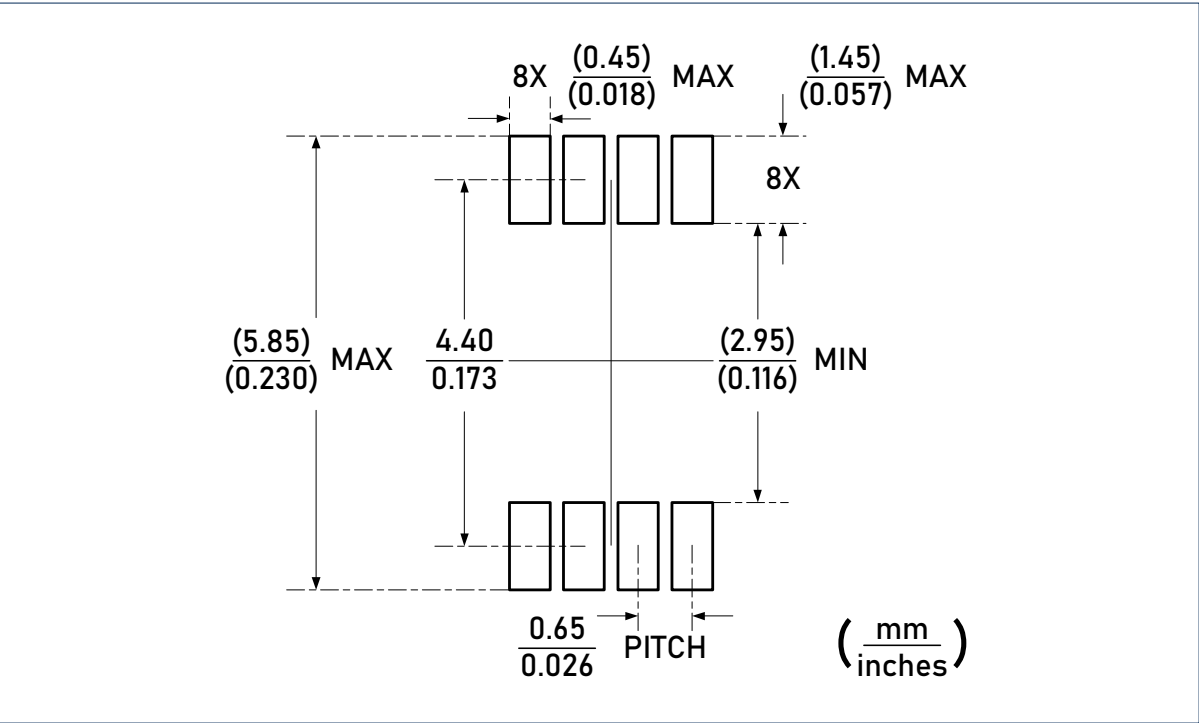
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Package Outlines (continued)

DIMENSIONS, MSOP-8L



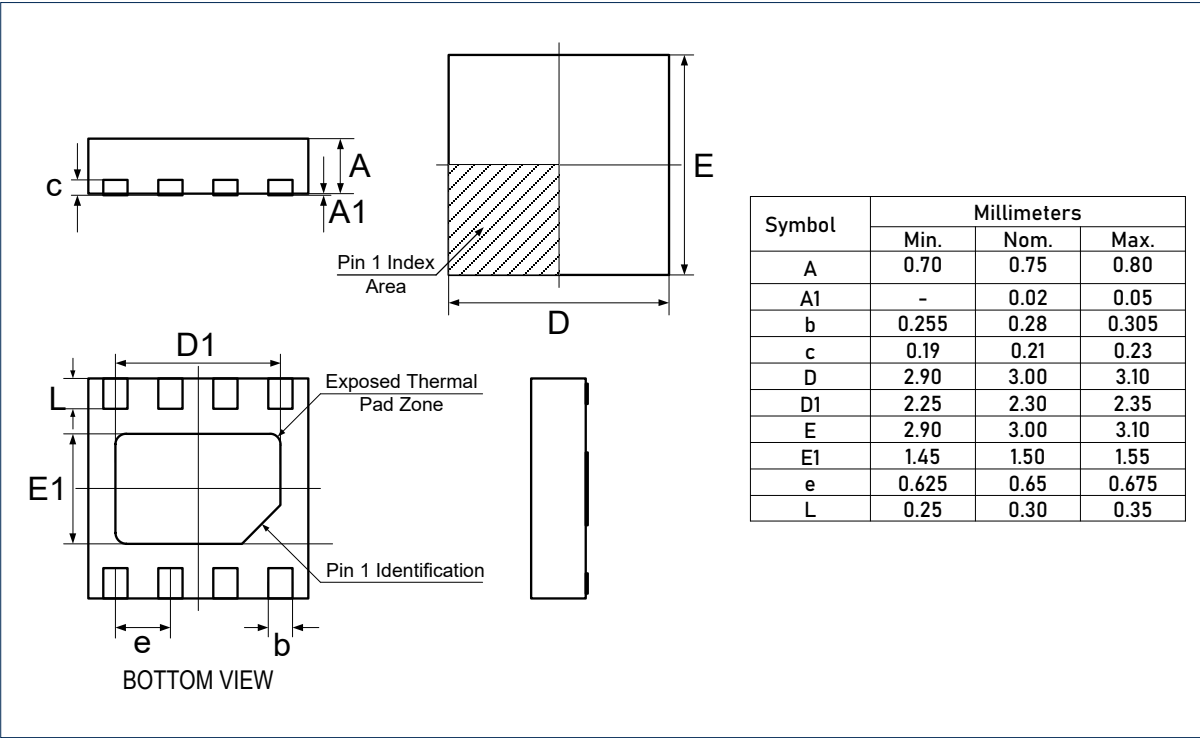
RECOMMENDED SOLDERING FOOTPRINT, MSOP-8L



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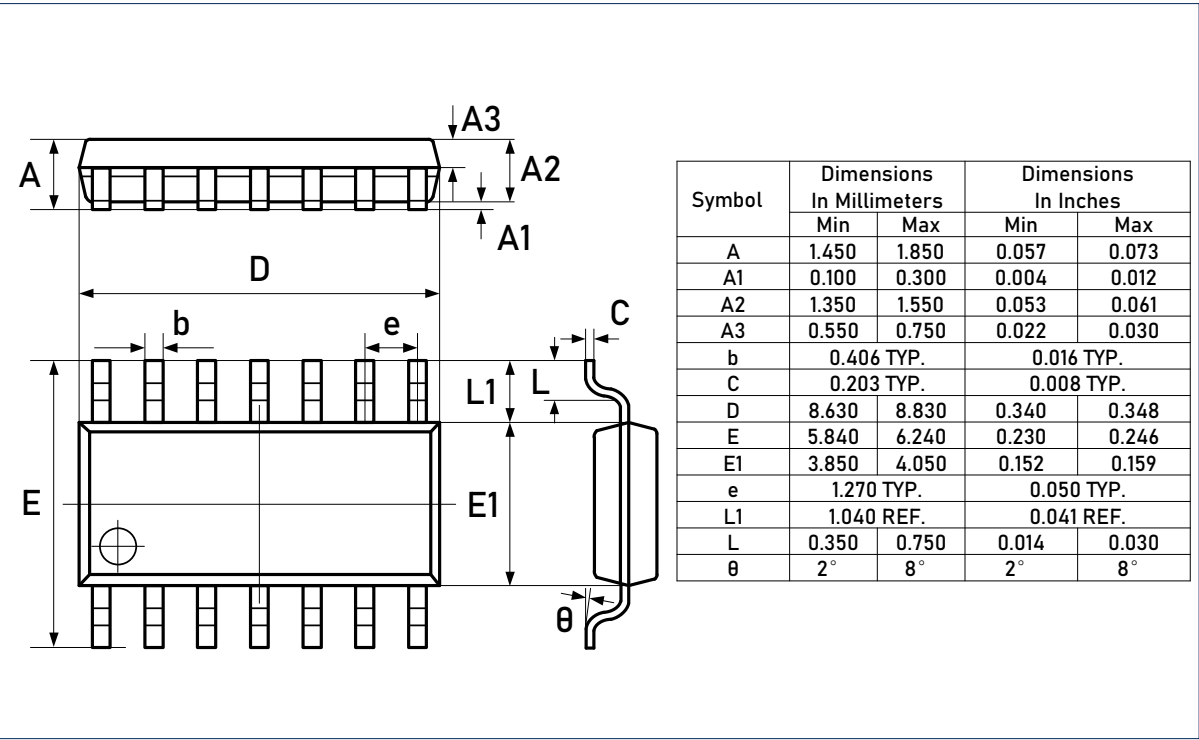
Package Outlines (continued)

DIMENSIONS, DFN3x3-8L

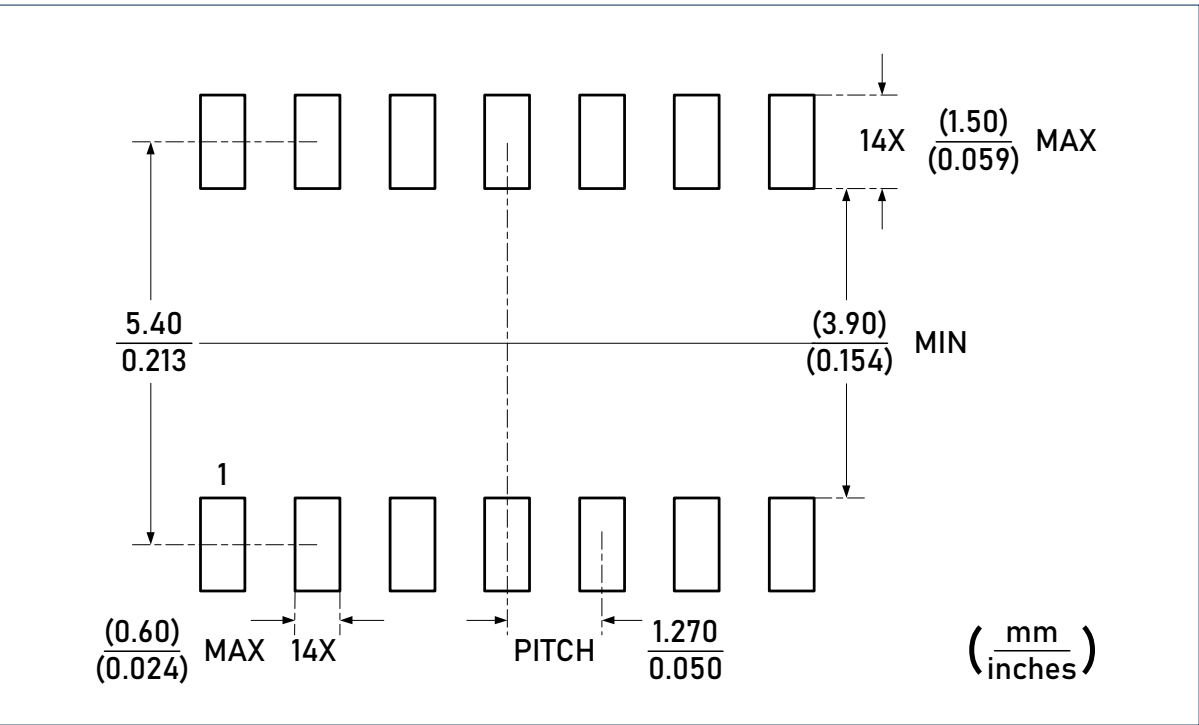


Package Outlines (continued)

DIMENSIONS, SOIC-14L

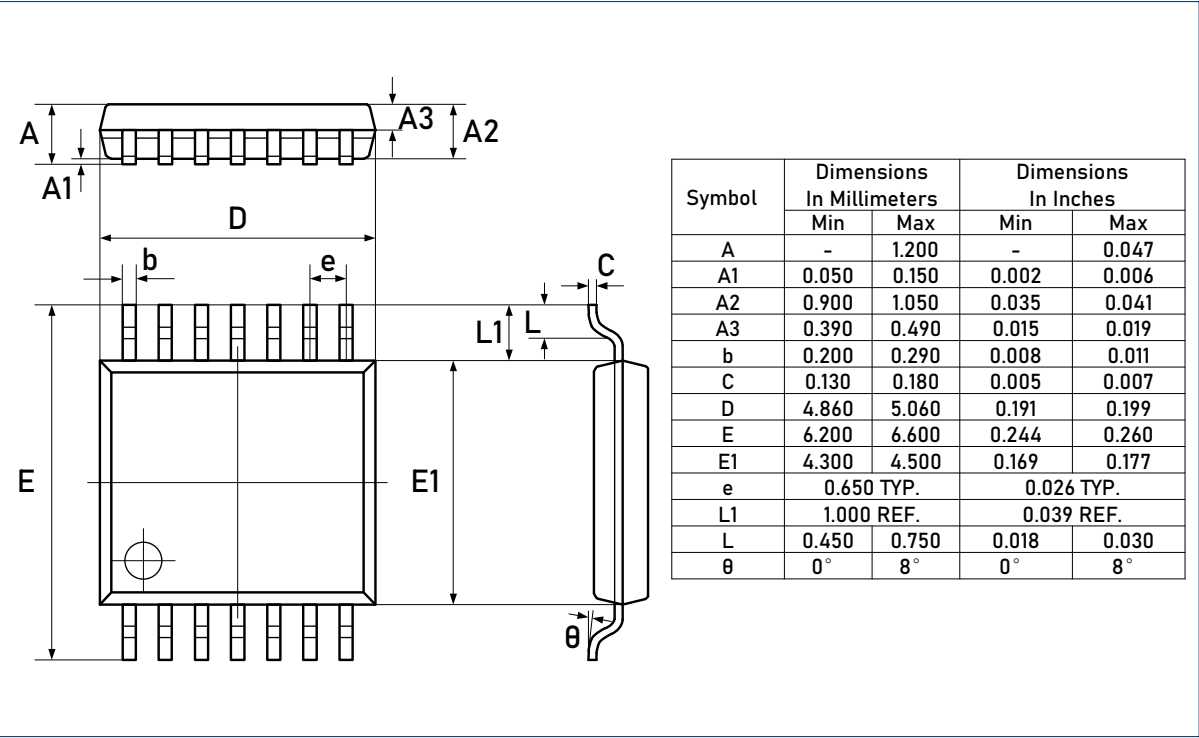


RECOMMENDED SOLDERING FOOTPRINT, SOIC-14L

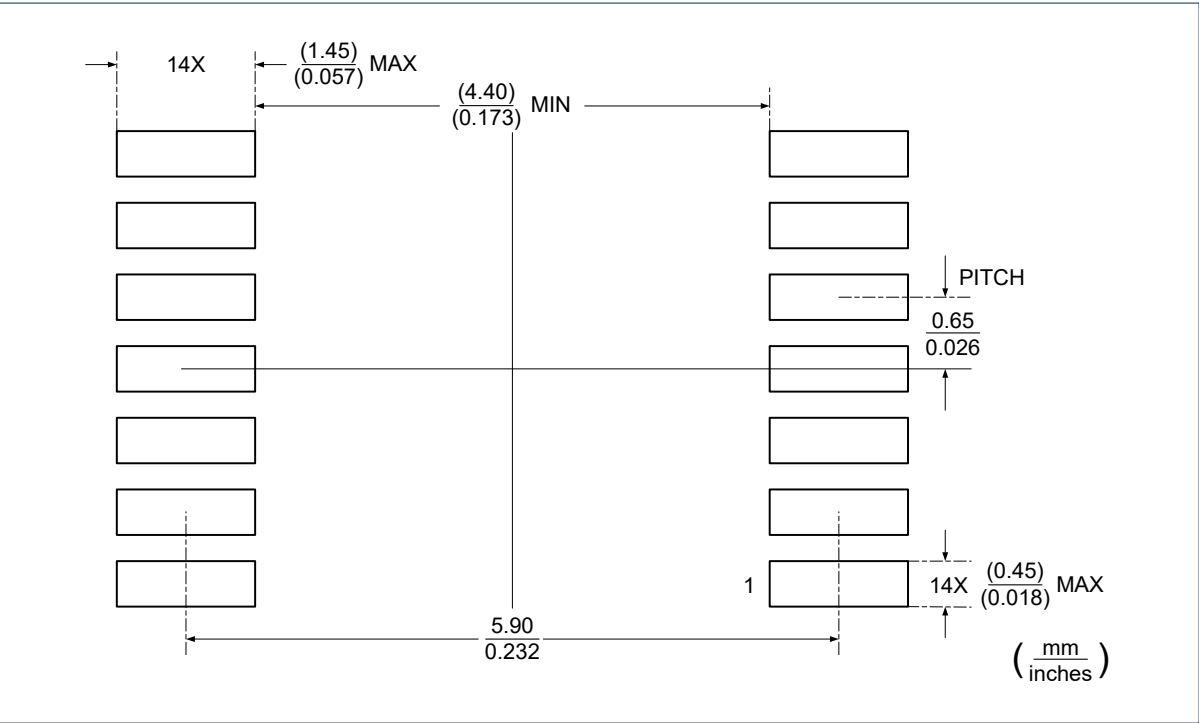


Package Outlines (continued)

DIMENSIONS, TSSOP-14L



RECOMMENDED SOLDERING FOOTPRINT, SOIC-14L



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