ADPL40502

Low Noise, 200mA, CMOS Linear Regulator

FEATURES

- Low Noise: 20μV_{RMS}
- No Noise Bypass Capacitor Required
- Stable with 1μF Ceramic Input and Output Capacitors
- Maximum Output Current: 200mA
- Input Voltage Range: 2.2V to 5.5V
- Low Quiescent Current
  - I_{GND} = 20μA with I_{OUT} = 0μA
  - I_{GND} = 290μA with I_{OUT} = 200mA
- Low Shutdown Current: <1μA
- Low Dropout Voltage: 150mV at I_{OUT} = 200mA
- Initial Accuracy: ±1%
- Accuracy Over Line, Load, and Temperature: ±2.5%
- 7 Fixed Output Voltage Options: 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 3.0V, and 3.3V
- PSRR Performance of 70dB at 10kHz
- Current-Limit and Thermal Overload Protection
- Logic Controlled Enable
- Internal Pull-Down Resistor on EN Input
- *5-Lead, Thin Small Outline Transistor Package*
- *6-Lead, Lead Frame Chip Scale Package*

APPLICATIONS

- RF, Voltage-Controlled Oscillator (VCO), and Phase Locked Loop (PLL) Power Supplies
- Mobile Phones
- Digital Camera and Audio Devices
- Portable and Battery-Powered Equipment
- Post DC-to-DC Regulation
- Portable Medical Devices

GENERAL DESCRIPTION

The ADPL40502 is a low noise, low dropout (LDO) linear regulator that operates from 2.2V to 5.5V and provides up to 200mA of output current. The low 150mV dropout voltage at 200mA load improves efficiency and allows operation over a wide input voltage range.

Using an innovative circuit topology, the ADPL40502 achieves low noise performance without the necessity of a bypass capacitor, making the device ideal for noise sensitive analog and RF applications. The ADPL40502 also achieves low noise performance without compromising the power supply rejection ratio (PSRR) or transient line and load performance. The low 290μA of operating supply current at 200mA load makes the ADPL40502 suitable for battery-operated portable equipment.

The ADPL40502 includes an internal pull-down resistor on the EN input.

The ADPL40502 is specifically designed for stable operation with tiny 1μF, ±30% ceramic input and output capacitors to meet the requirements of high performance, space constrained applications.

The ADPL40502 is capable of 7 fixed output voltage options, ranging from 1.2V to 3.3V.

Short-circuit and thermal overload protection circuits prevent damage in adverse conditions. The ADPL40502 is available in tiny 5-Lead, TSOT and 6-Lead, 2mm x 2mm LFCSP for the smallest footprint solution to meet a variety of portable power application requirements.

TYPICAL APPLICATION CIRCUITS

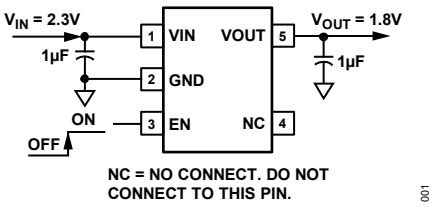

Figure 1. TSOT ADPL40502 with Fixed Output Voltage, 1.8V

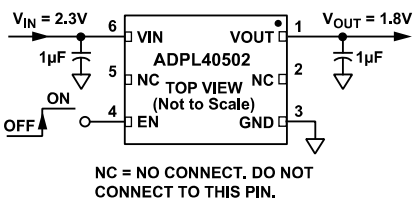

Figure 2. LFCSP ADPL40502 with Fixed Output Voltage, 1.8V

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REVSION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	12/24	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(V_{IN} = (V_{OUT} + 0.4 V) or 2.2 V, whichever is greater, V_{EN} = V_{IN}, I_{OUT} = 10mA, C_{IN} = C_{OUT} = 1µF, and T_A = -40°C to +125°C (Typ values at 25°C), unless otherwise noted. Note that V_{IN} is the input voltage, V_{OUT} is the output voltage, I_{OUT} is the output current, C_{IN} is the input capacitance, and C_{OUT} is the output capacitance.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		2.2		5.5	V
Operating Supply Current	I_{GND}	I_{OUT} = 0µA		20	40	µA
		I_{OUT} = 10mA		75	105	µA
		I_{OUT} = 200mA		290	390	µA
Shutdown Current	I_{GND-SD}	EN = GND		0.2	1.0	µA
Output Voltage Accuracy	V_{OUT}	I_{OUT} = 10mA	−1		+1	%
		100µA < I_{OUT} < 200mA, V_{IN} = (V_{OUT} + 0.4V) to 5.5V	−3		+2	%
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.4V) to 5.5V, T_J = −40°C to +125°C	−0.05		+0.05	%/V
Load Regulation[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 100µA to 200mA		0.006	0.012	%/mA
Dropout Voltage[2]	$V_{DROPOUT}$	I_{OUT} = 10mA		10	30	mV
		I_{OUT} = 200mA		150	230	mV
Start-up Time[3]	$t_{START-UP}$	V_{OUT} = 3.3V		180		µs
Current-Limit Threshold[4]	I_{LIMIT}	T_J = 0°C to +125°C	220	300	400	mA
Undervoltage Lockout						
Input Voltage Rising	$UVLO_{RISE}$				1.96	V
Input Voltage Falling	$UVLO_{FALL}$		1.28			V
Hysteresis	$UVLO_{HYS}$			120		mV
Thermal Shutdown						
Threshold	TS_{SD}	T_J rising		150		°C
Hysteresis	TS_{SD-HYS}			15		°C
EN Input						
Logic High	V_{IH}	2.2V ≤ V_{IN} ≤ 5.5V	1.2			V
Logic Low	V_{IL}	2.2V ≤ V_{IN} ≤ 5.5V			0.4	V
Pull-Down Resistance	R_{EN}	V_{IN} = EN voltage (V_{EN}) = 5.5V		2.6		MΩ
Output Noise						

(V_{IN} = (V_{OUT} + 0.4 V) or 2.2 V, whichever is greater, V_{EN} = V_{IN}, I_{OUT} = 10mA, C_{IN} = C_{OUT} = 1µF, and T_A = -40°C to +125°C (Typ values at 25°C), unless otherwise noted. Note that V_{IN} is the input voltage, V_{OUT} is the output voltage, I_{OUT} is the output current, C_{IN} is the input capacitance, and C_{OUT} is the output capacitance.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Noise	OUT_{NOISE}	10Hz to 100kHz, V_{IN} = 5V, V_{OUT} = 3.3V		20		μV_{RMS}
		10Hz to 100kHz, V_{IN} = 5V, V_{OUT} = 2.5V		20		μV_{RMS}
Power Supply Rejection Ratio						
Power Supply Rejection Ratio	PSRR	10kHz, V_{IN} = 3.8V to 4.3V, V_{OUT} = 3.3V, I_{OUT} = 10mA		70		dB
		100kHz, V_{IN} = 3.8V to 4.3V, V_{OUT} = 3.3V, I_{OUT} = 10mA		55		dB

1 Based on an end-point calculation using 0.1mA and 200mA loads. See *Figure 6* for typical load regulation performance for loads less than 1mA

2 Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This voltage applies only for output voltages above 2.2V.

3 Start-up time is defined as the time between the rising edge of EN and V_{OUT} being at 90% of its nominal value.

4 Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0V (i.e., 2.7V).

Table 2. Input and Output Capacitor, Recommended Specifications

(**INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS**)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Minimum Input and Output Capacitance[1]	C_{MIN}	T_A = −40°C to +125°C		0.7			µF
Capacitor ESR	R_{ESR}	T_A = −40°C to +125°C		0.001		0.2	Ω

1 The minimum input and output capacitance must be greater than 0.7µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended, and Y5V and Z5U capacitors are not recommended for use with any low dropout (LDO) regulator.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 3. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN} to GND	−0.3V to +6.5V
V_{OUT} to GND	−0.3 V to V_{IN}
EN to GND	−0.3V to +6.5V
Temperature Range	
Storage	−65°C to +150°C
Operating Junction	−40°C to +125°C
Operating Ambient	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Data

Absolute maximum ratings apply individually only, not in combination. The ADPL40502 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. T_J of the device is dependent on T_A, the power dissipation of the device (P_D), and the junction to ambient thermal resistance of the package (θ_{JA}).

To calculate the maximum T_J from T_A and P_D use the following equation:

$$T_J = T_A + (P_D \times \theta_{JA})$$

The θ_{JA} of the package is based on modeling and calculation using a 4-layer board. θ_{JA} is highly dependent on the application and board layout. In applications where high maximum P_D exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 inches × 3 inches circuit board. See JESD51-7 and JESD51-9 for detailed information on the board construction.

Ψ_{JB} is the junction to board, thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, Guidelines for Reporting and Using Electronic Package Thermal Information, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in θ_{JB}.

Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. To calculate the maximum T_J from the board temperature (T_B) and P_D, use the following equation:

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

Thermal Resistance

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
5-Lead TSOT (UJ-5)	170	43	°C/W
6-Lead LFCSP (CP-6-3)	63.6	28.3	°C/W

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

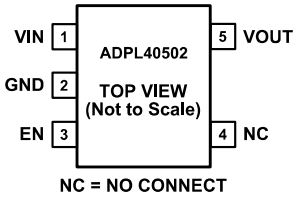

Figure 3. 5-Lead TSOT Pin Configuration

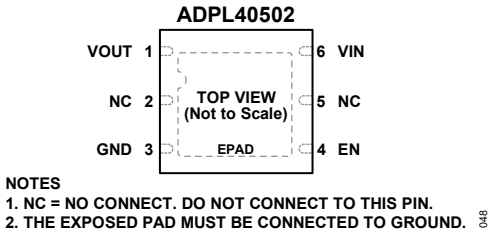

Figure 4. 6-Lead LFCSP Pin Configuration

Pin Descriptions

Table 5. Pin Descriptions

PIN		Mnemonic	DESCRIPTION
TSOT	LFCSP		
1	6	V_{IN}	Regulator Input Supply. Bypass V_{IN} to GND with a 1µF or greater capacitor.
2	3	GND	Ground.
3	4	EN	Enable Input. Drive EN high to turn on the regulator and drive EN low to turn off the regulator. For automatic startup, connect EN to V_{IN}.
4	2	NC	No Connect. Not connected internally.
5	1	V_{OUT}	Regulated Output Voltage. Bypass V_{OUT} to GND with a 1µF or greater capacitor.
Not applicable	5	NC	No Connect. Not connected internally.
Not applicable		EPAD	Exposed Pad. The exposed pad must be connected to ground. The exposed pad enhances the thermal performance of the package.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1µF, and T_A = 25°C, unless otherwise noted.

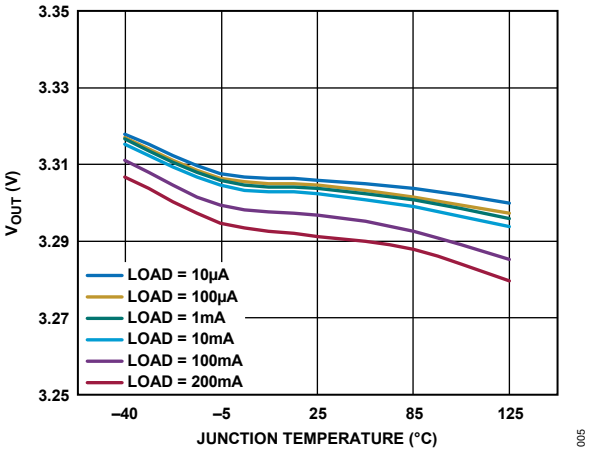

Figure 5. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J)

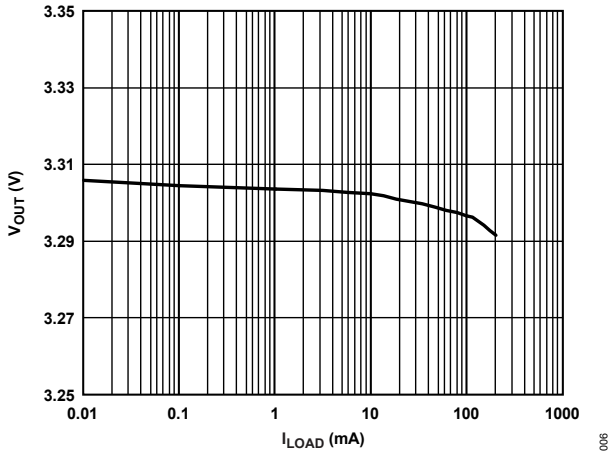

Figure 6. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD})

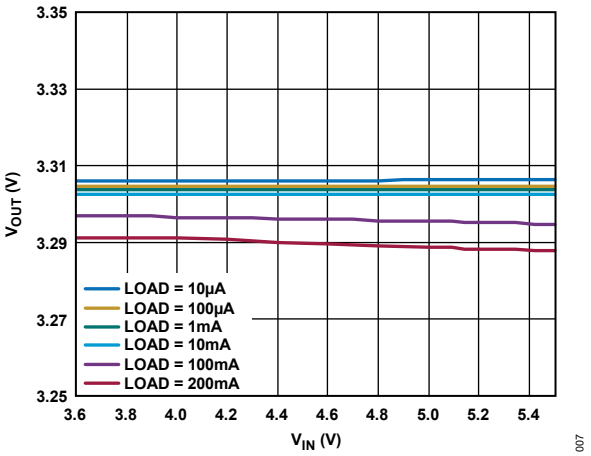

Figure 7. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN})

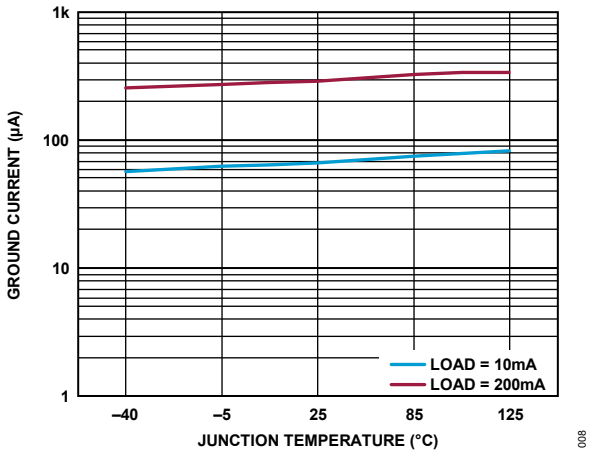

Figure 8. Ground Current (I_{GND}) vs. Junction Temperature (T_J)

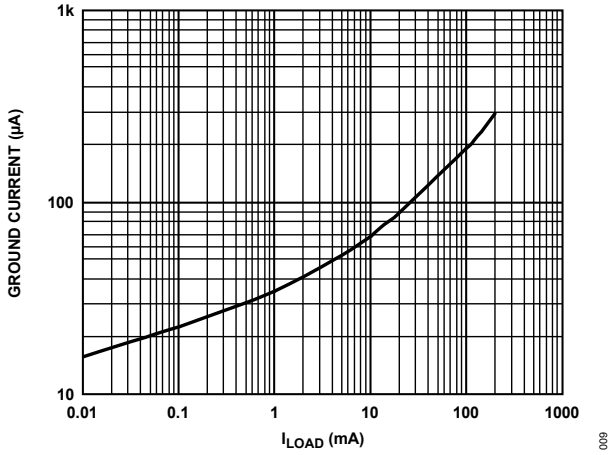

Figure 9. Ground Current (I_{GND}) vs. Load Current (I_{LOAD})

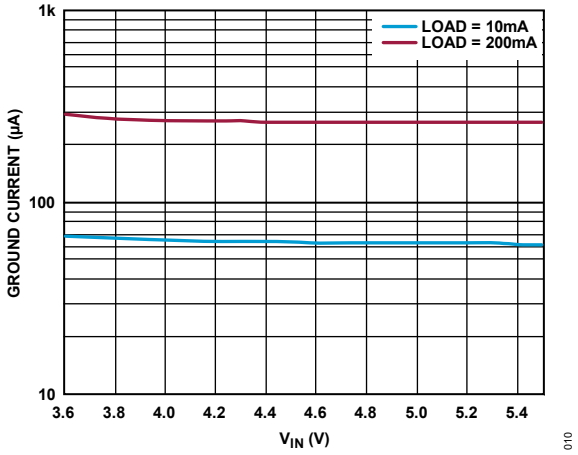

Figure 10. Ground Current (I_{GND}) vs. Input Voltage (V_{IN})

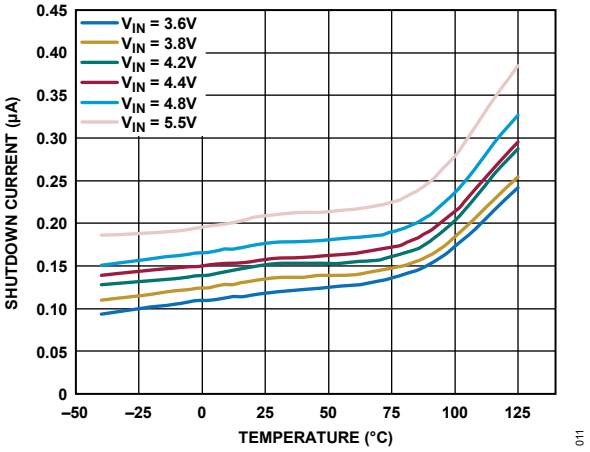

Figure 11. Shutdown Current (I_{GND-SD}) vs. Temperature (T_J) at Various Input Voltages

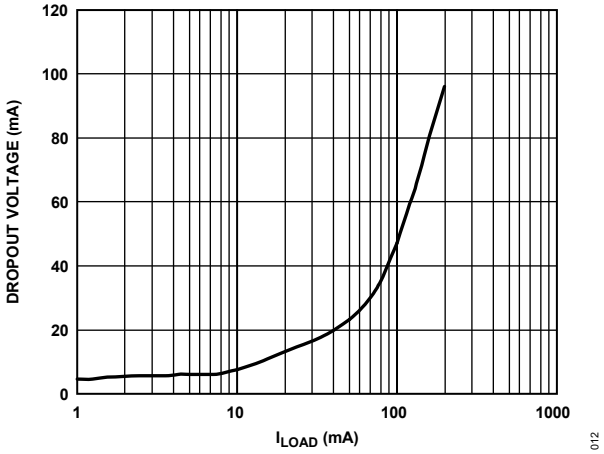

Figure 12. Dropout Voltage ($V_{DROPOUT}$) vs. Load Current (I_{LOAD})

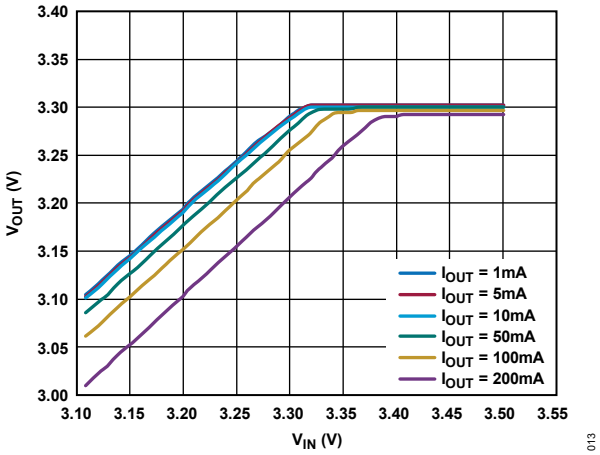

Figure 13. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) (in Dropout)

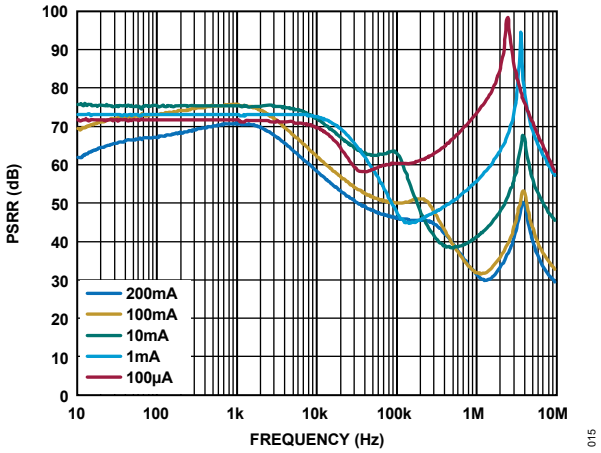

Figure 14. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = 1.2V, V_{IN} = 2.2V

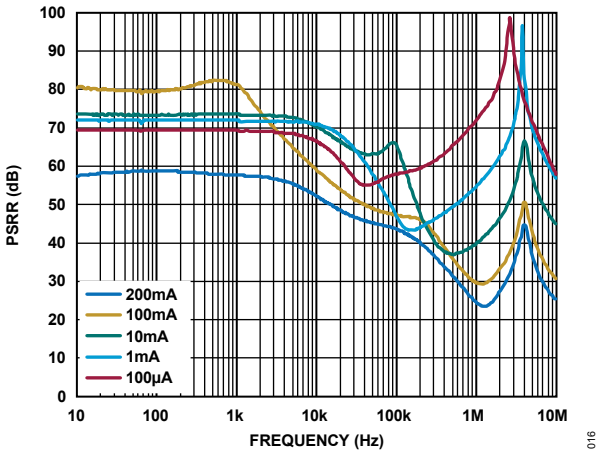

Figure 15. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = 2.8V, V_{IN} = 3.3V

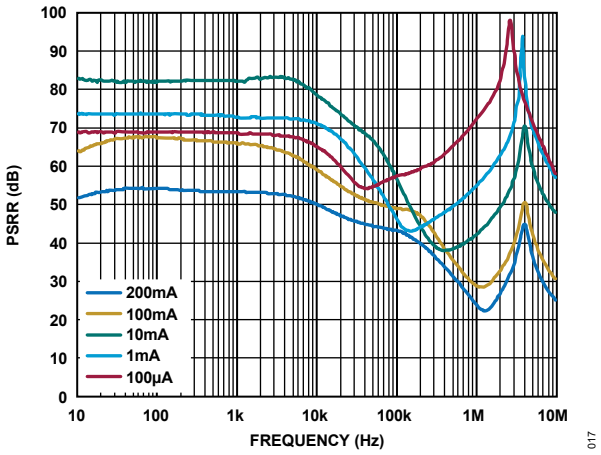

Figure 16. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = 3.3V, V_{IN} = 3.8V

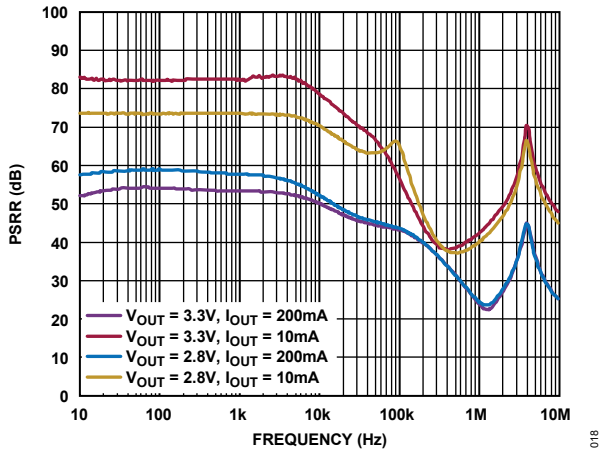

Figure 17. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Output Voltages and Load Currents, $V_{OUT} - V_{IN} = 0.5V$

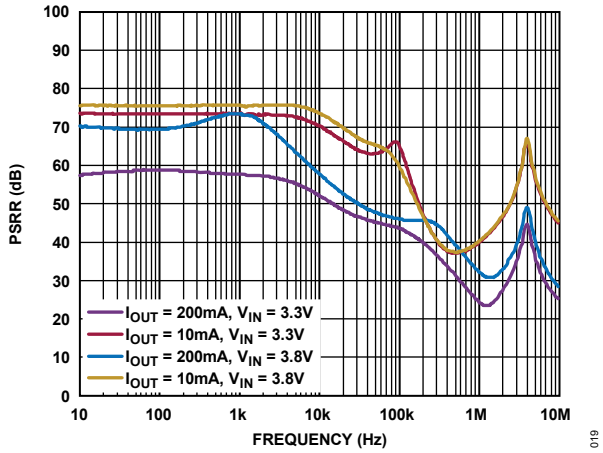

Figure 19. Power Supply Rejection Ratio (PSRR) vs. Frequency at Various Voltages and Load Currents, $V_{OUT} = 2.8V$

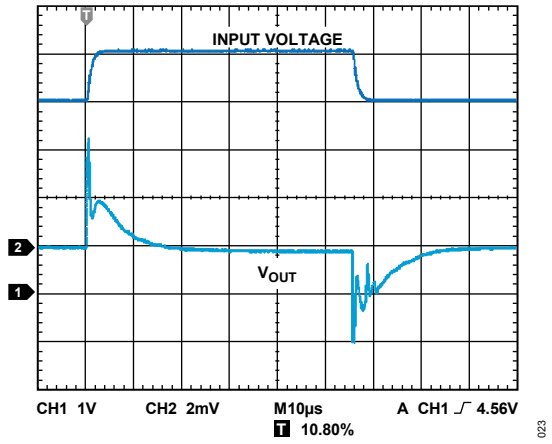

Figure 21. Line Transient Response, $C_{IN} = C_{OUT} = 1\mu F$, $I_{LOAD} = 200mA$

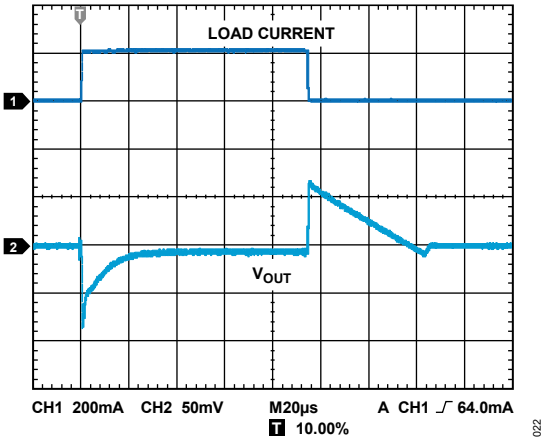

Figure 18. Load Transient Response, $C_{IN} = C_{OUT} = 1\mu F$, $I_{LOAD} = 1mA$ to $200mA$

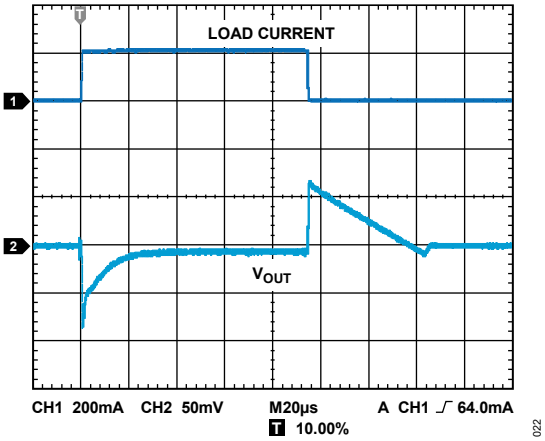

Figure 20. Load Transient Response, $C_{IN} = C_{OUT} = 1\mu F$, $I_{LOAD} = 1mA$ to $200mA$

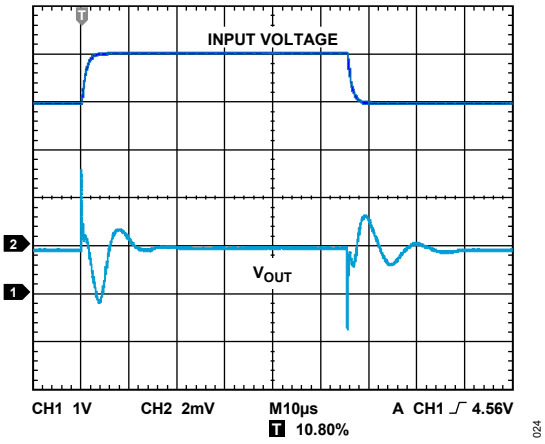

Figure 22. Line Transient Response, $C_{IN} = C_{OUT} = 1\mu F$, $I_{LOAD} = 1mA$

THEORY OF OPERATION

The ADPL40502 is a low noise, low quiescent current, LDO linear regulator that operates from 2.2V to 5.5V and can provide up to 200mA of output current. Drawing a low 290µA of operating supply current (typical) at full load makes the ADPL40502 ideal for battery operated, portable equipment. Shutdown current consumption is typically 0.2µA.

Internally, the ADPL40502 consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device pulls lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device pulls higher, allowing less current to pass and decreasing the output voltage.

An internal pull-down resistor on the EN input holds the input low when the pin is left open.

The ADPL40502 is available in seven output voltage options, ranging from 1.2V to 3.3V. The ADPL40502 uses the EN pin to enable and disable the V_{OUT} pin under normal operating conditions. When EN is high, V_{OUT} turns on, and when EN is low, V_{OUT} turns off. For automatic startup, tie EN to V_{IN}.

APPLICATIONS INFORMATION

Capacitor Selection

Output Capacitor

The ADPL40502 is designed for operation with small, space-saving ceramic capacitors but can function with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 1µF capacitance with an ESR of 1Ω or less is recommended to ensure the stability of the ADPL40502. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADPL40502 to large changes in load current. *Figure 23* shows the transient responses for an output capacitance value of 1µF. Derating of ceramic capacitors with DC voltage, temperature, and AC signal must be considered while selecting the output capacitor. Effective capacitance can be 80% lower than the nominal capacitor value. Derating curves are available from all major ceramic capacitor vendors.

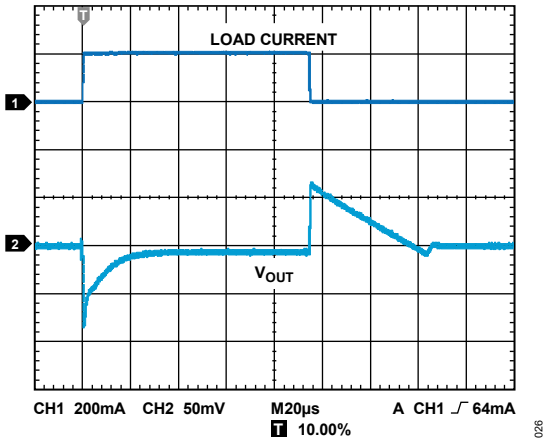

Figure 23. Output Transient Response, C_{OUT} = 1µF

Input Bypass Capacitor

Connecting a 1µF capacitor from V_{IN} to GND reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance are encountered. If greater than 1µF of output capacitance is required, the input capacitor must be increased to match it. Derating of ceramic capacitors with DC voltage, temperature, and AC signal must be considered while selecting the output capacitor. Effective capacitance can be 80% lower than the nominal capacitor value. Derating curves are available from all major ceramic capacitor vendors.

Enable Feature

The ADPL40502 uses the EN pin to enable and disable the V_{OUT} pin under normal operating conditions. As shown in *Figure 24*, when a rising voltage on EN crosses the active threshold, V_{OUT} turns on. When a falling voltage on EN crosses the inactive threshold, V_{OUT} turns off.

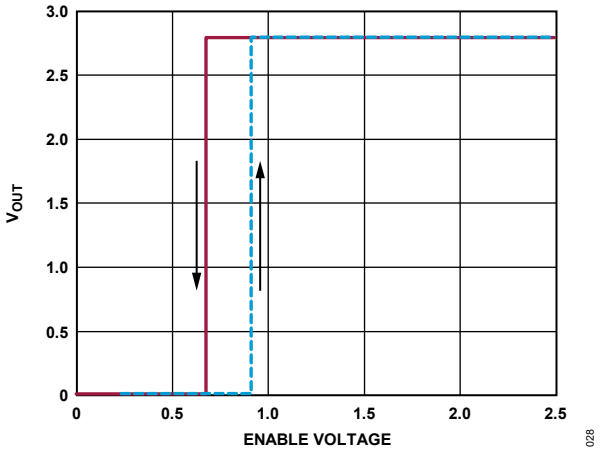

Figure 24. ADPL40502 Typical EN Pin Operation

As shown in *Figure 24*, the EN pin has hysteresis built in to prevent on and off oscillations that can occur due to noise on the EN pin as this pin passes through the threshold points.

The EN pin active and inactive thresholds are derived from the V_{IN} voltage. Therefore, these thresholds vary with changing input voltage. *Figure 25* shows typical EN active and inactive thresholds when the input voltage varies from 2.2V to 5.5V.

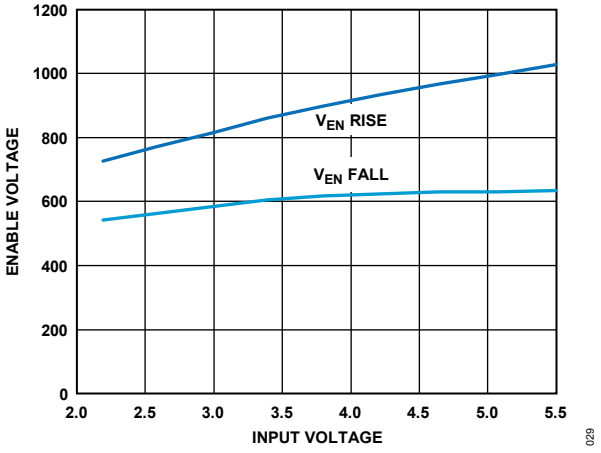

Figure 25. Typical EN Pin Thresholds vs. Input Voltage

The ADPL40502 uses an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 3.3V option is approximately 180µs from the time the EN active threshold is crossed to when the output reaches 90% of its final value. *Figure 26* shows typical EN active and inactive thresholds when the input voltage varies from 2.2V to 5.5V.

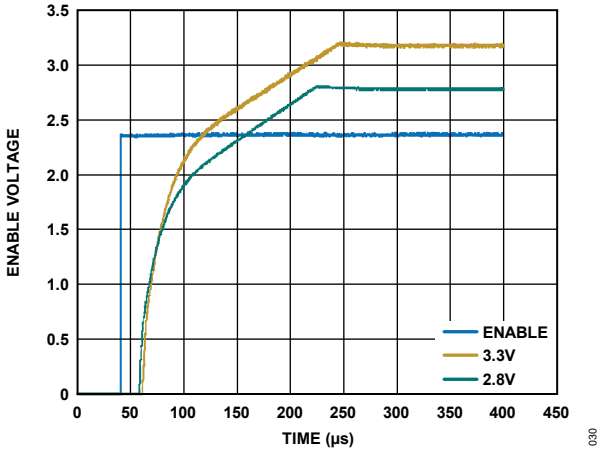

Figure 26. Typical Start-Up Behavior

Current-Limit and Thermal Overload Protection

The ADP40502 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADPL40502 is designed to current limit when the output load reaches 300mA (typical). When the output load exceeds 300mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (i.e., high ambient temperature and power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to 0. When the junction temperature drops below 135°C, the output is turned on again, and the output current is restored to its nominal value.

Consider the case where a hard short from V_{OUT} to ground occurs. At first, the ADPL40502 current limits, so that only 300mA is conducted into the short. If self heating of the junction causes its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to 0. As the junction temperature cools and drops below 135°C, the output turns on and conducts 300mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 300mA and 0mA that continues as long as the short remains at the output.

Current-limit and thermal limit protections protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that junction temperatures do not exceed 125°C.

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADPL40502.

Place the input capacitor as close as possible to the V_{IN} and the GND pins. Place the output capacitor as close as possible to the V_{OUT} and the GND pins. Use of 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

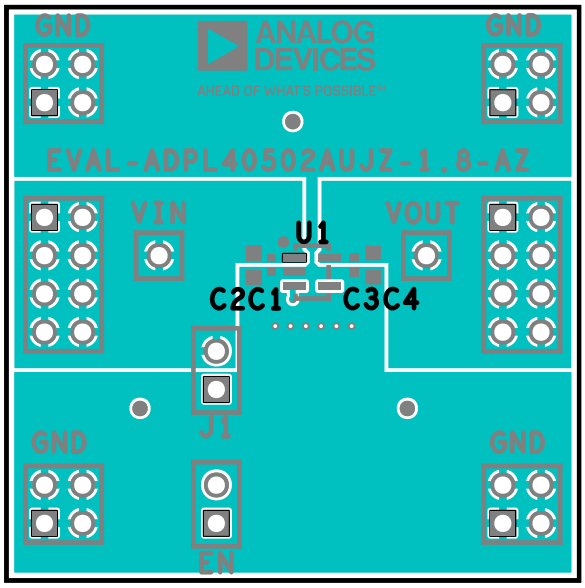

Figure 27. Example TSOT PCB Layout

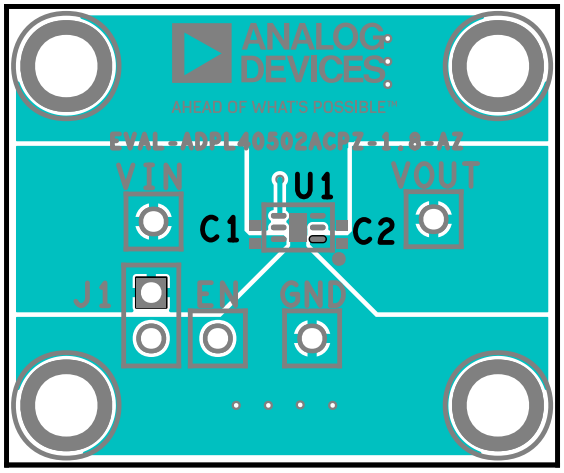

Figure 28. Example LFCSP PCB Layout

OUTLINE DIMENSIONS

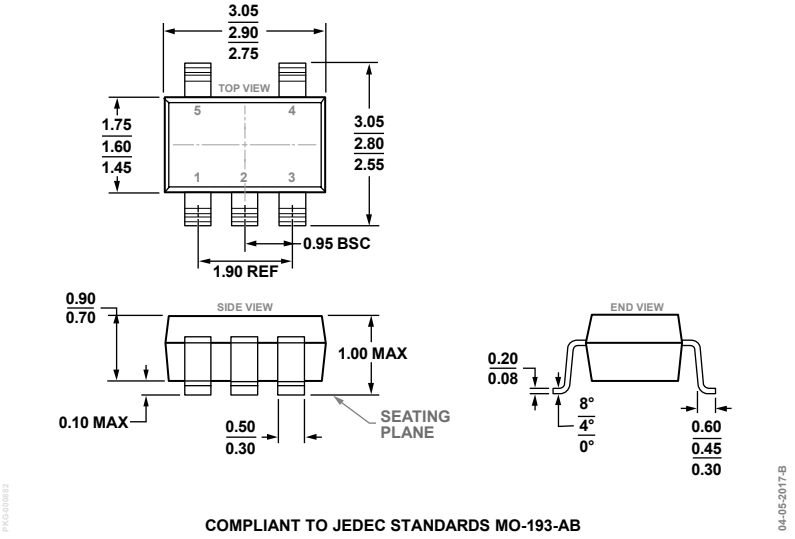

Figure 29. 5-Lead, Thin Small Outline Transistor Package [TSOT] (UJ-5) Dimensions shown in millimeters

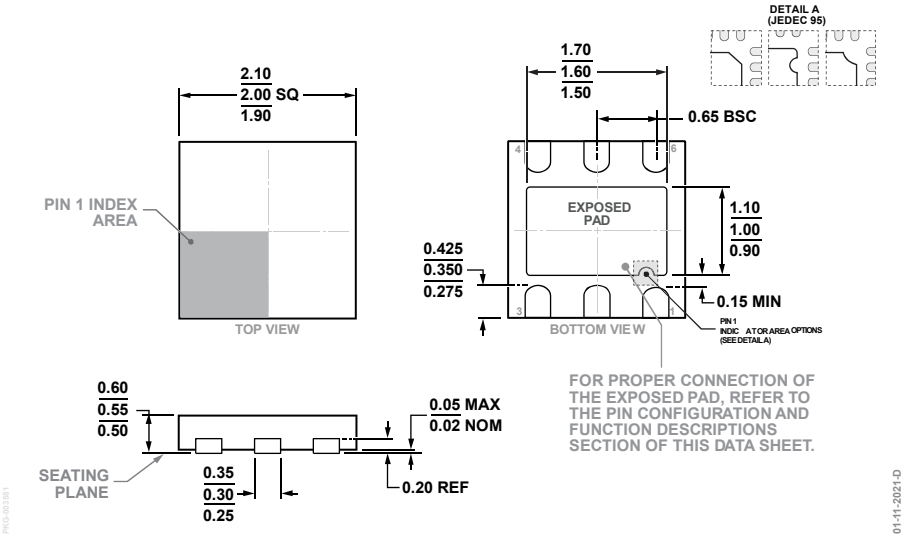

Figure 30. 6-Lead, Lead Frame Chip Scale Package [LFCSP] 2mm × 2mm Body and 0.55mm Package Height (CP-6-3) Dimensions shown in millimeters

ORDERING GUIDE

Table 6. Ordering Guide

MODEL[1]	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKING QUANTITY
ADPL40502ACPZ-1.2-R7	-40°C to +125°C	6-Lead LFCSP (2mm x 2mm w/ EP)	Reel, 3000
ADPL40502ACPZ-1.8-R7	-40°C to +125°C	6-Lead LFCSP (2mm x 2mm w/ EP)	Reel, 3000
ADPL40502ACPZ-2.5-R7	-40°C to +125°C	6-Lead LFCSP (2mm x 2mm w/ EP)	Reel, 3000
ADPL40502ACPZ-3.0-R7	-40°C to +125°C	6-Lead LFCSP (2mm x 2mm w/ EP)	Reel, 3000
ADPL40502ACPZ-3.3-R7	-40°C to +125°C	6-Lead LFCSP (2mm x 2mm w/ EP)	Reel, 3000
ADPL40502AUJZ-1.2-R7	-40°C to +125°C	5-Lead TSOT	Reel, 3000
ADPL40502AUJZ-1.5-R7	-40°C to +125°C	5-Lead TSOT	Reel, 3000
ADPL40502AUJZ-1.8-R7	-40°C to +125°C	5-Lead TSOT	Reel, 3000
ADPL40502AUJZ-2.5-R7	-40°C to +125°C	5-Lead TSOT	Reel, 3000
ADPL40502AUJZ-2.8-R7	-40°C to +125°C	5-Lead TSOT	Reel, 3000
ADPL40502AUJZ-3.0-R7	-40°C to +125°C	5-Lead TSOT	Reel, 3000
ADPL40502AUJZ-3.3-R7	-40°C to +125°C	5-Lead TSOT	Reel, 3000

Output Voltage Options

Table 7. Output Voltage Options

MODEL[1]	OUTPUT VOLTAGE (V)[2]
ADPL40502ACPZ-1.2-R7, ADPL40502AUJZ-1.2-R7	1.2
ADPL40502AUJZ-1.5-R7	1.5
ADPL40502ACPZ-1.8-R7, ADPL40502AUJZ-1.8-R7	1.8
ADPL40502ACPZ-2.5-R7, ADPL40502AUJZ-2.5-R7	2.5
ADPL40502AUJZ-2.8-R7	2.8
ADPL40502ACPZ-3.0-R7, ADPL40502AUJZ-3.0-R7	3.0
ADPL40502ACPZ-3.3-R7, ADPL40502AUJZ-3.3-R7	3.3

[1] Z = RoHS Compliant Part.

[2] For additional voltage options, contact a local Analog Devices, Inc., sales or distribution representative.