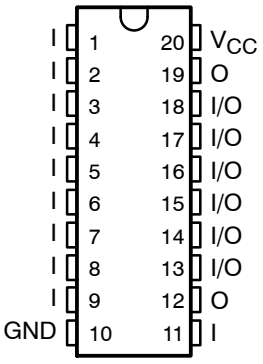
# TIBPAL16L8-15M, TIBPAL16R4-15M
# HIGH-PERFORMANCE *IMPACT* ™ *PAL*® CIRCUITS

SRPS018B – D3338, JANUARY 1986 – REVISED NOVEMBER 2011

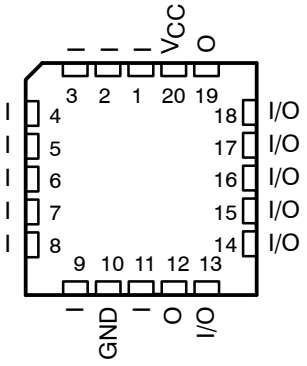
- **High-Performance Operation:**
  **Propagation Delay . . . 15 ns Max**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set High, but Voltage Levels at the Output Pins Go Low)**
- **Package Options Include Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

| DEVICE | I INPUTS | 3-STATE O OUTPUTS | REGISTERED Q OUTPUTS | I/O PORTS |
|---|---|---|---|---|
| PAL16L8 | 10 | 2 | 0 | 6 |
| PAL16R4 | 8 | 0 | 4 (3-state buffers) | 4 |
| PAL16R6 | 8 | 0 | 6 (3-state buffers) | 2 |
| PAL16R8 | 8 | 0 | 8 (3-state buffers) | 0 |

**TIBPAL16L8'**
**J OR W PACKAGE**
**(TOP VIEW)**




**TIBPAL16L8'**
**FK PACKAGE**
**(TOP VIEW)**




Pin assignments in operating mode

## description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

The TIBPAL16' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

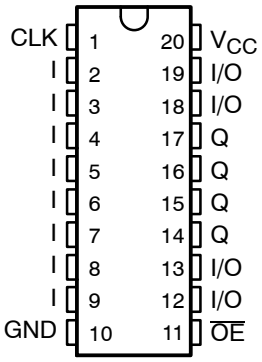
**IMPORTANT PROGAMMING NOTE:** For TIBPAL16L8–15M devices in J, W, or FK packages – For date code 9903A or later device programming, select from either **TI Military/16L8–12** or TI commercial **TI/16L8–10** on the Manufacturer/Device menu listing in your programming system.

**IMPORTANT PROGAMMING NOTE:** For TIBPAL16R4–15M devices in J, W, or FK packages – For date code 9616A or later device programming, select from either **TI Military/16R4–12** or TI commercial **TI /16R4–10** on the Manufacturer/Device menu listing in your programming system.

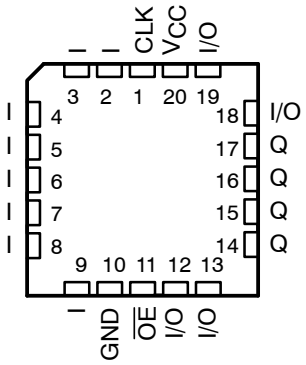
# TIBPAL16L8-15M, TIBPAL16R4-15M
# HIGH-PERFORMANCE *IMPACT* ™ *PAL*® CIRCUITS

SRPS018B – D3338, JANUARY 1986 – REVISED NOVEMBER 2011

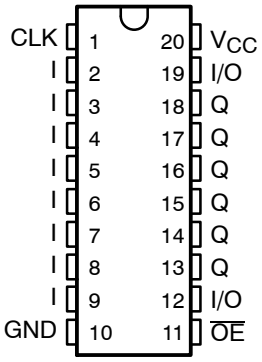
**TIBPAL16R4'**
**J OR W PACKAGE**
**(TOP VIEW)**



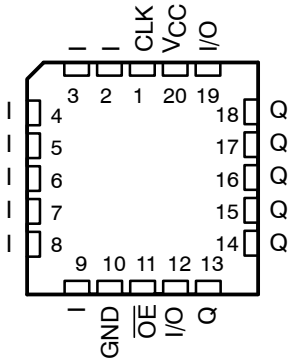

**TIBPAL16R4'**
**FK PACKAGE**
**(TOP VIEW)**



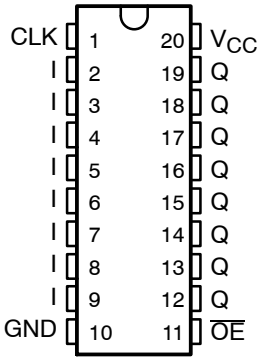

**TIBPAL16R6'**
**J OR W PACKAGE**
**(TOP VIEW)**



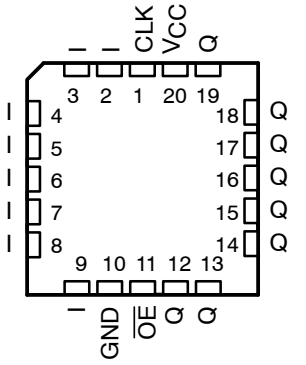

**TIBPAL16R6'**
**FK PACKAGE**
**(TOP VIEW)**




**TIBPAL16R8'**
**J OR W PACKAGE**
**(TOP VIEW)**



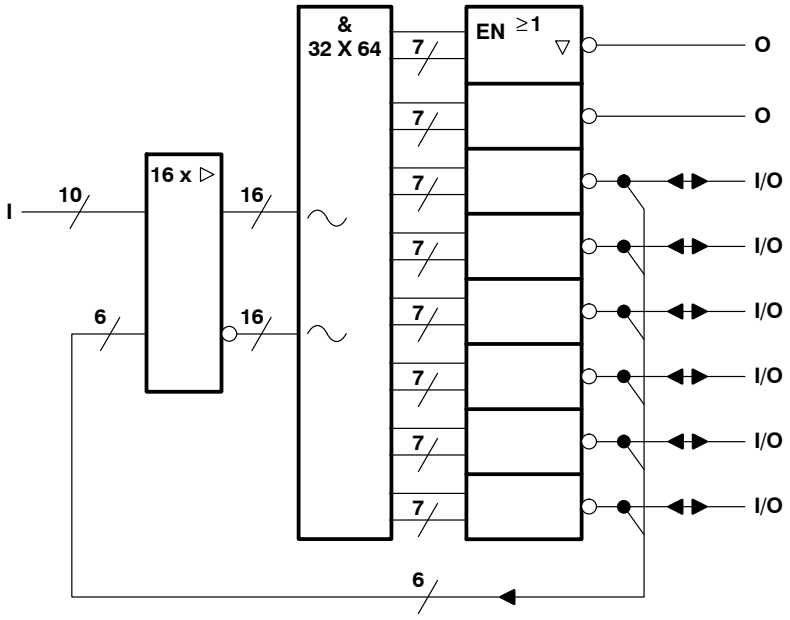

**TIBPAL16R8'**
**FK PACKAGE**
**(TOP VIEW)**



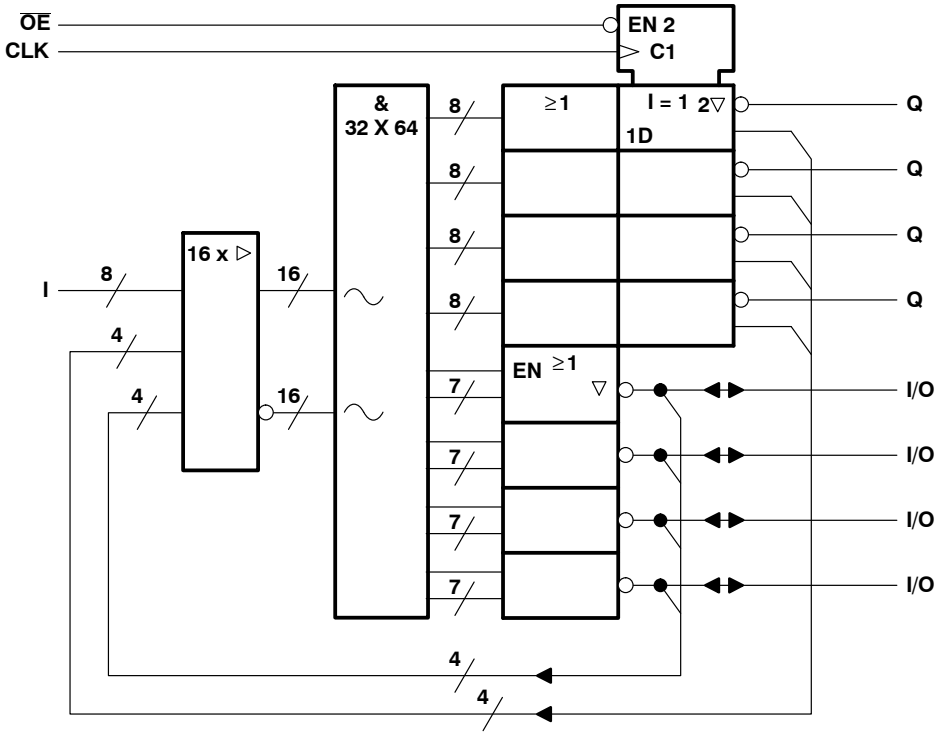

Pin assignments in operating mode

## functional block diagrams (positive logic)

TIBPAL16L8'



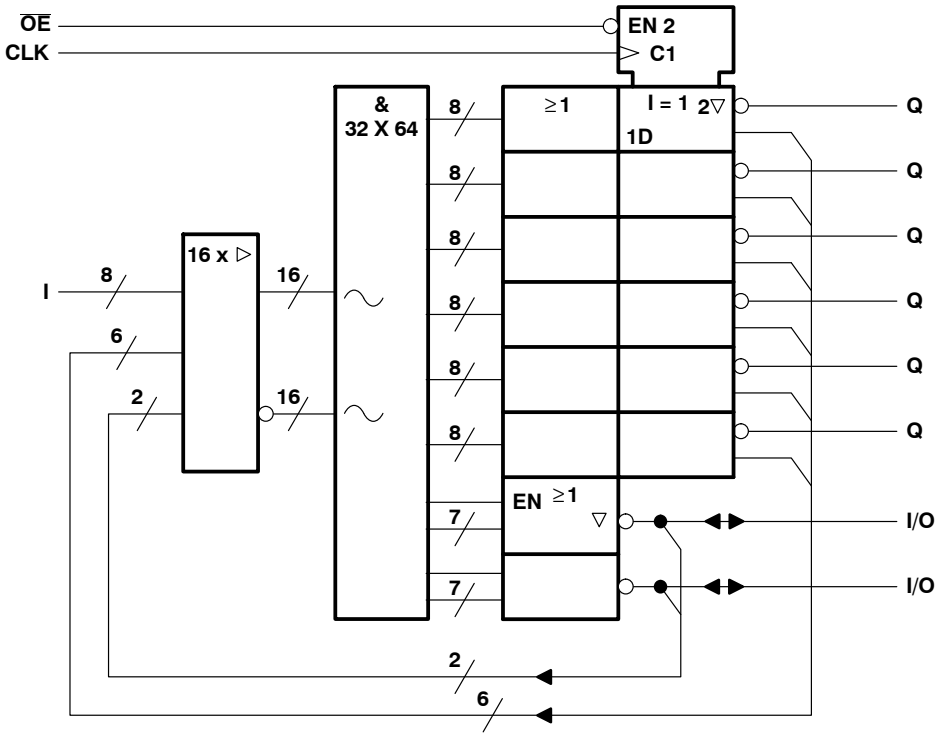

TIBPAL16R4'



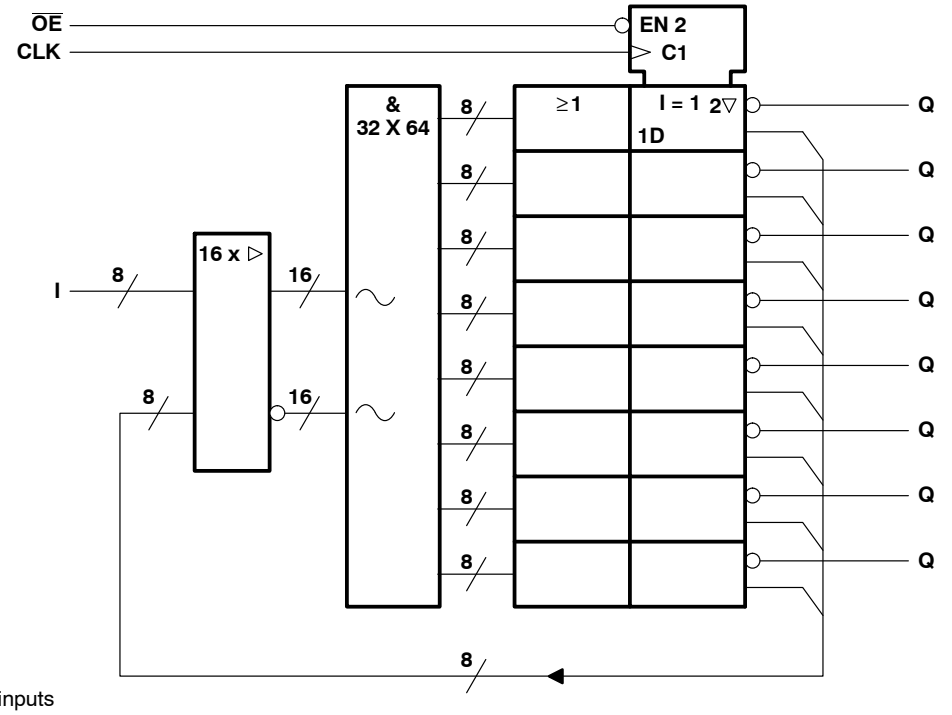

denotes fused inputs

## functional block diagrams (positive logic)

**TIBPAL16R6'**

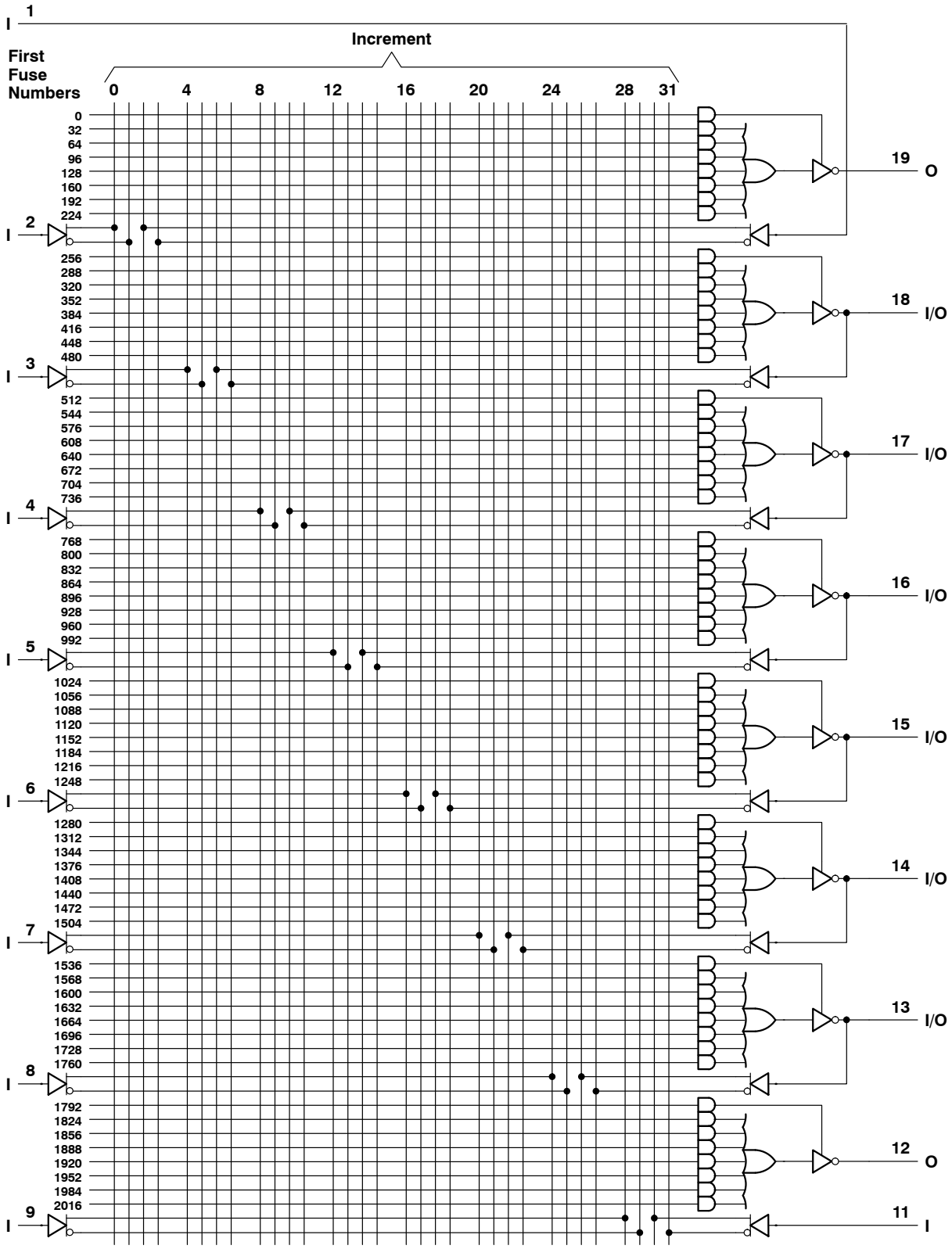



**TIBPAL16R8'**



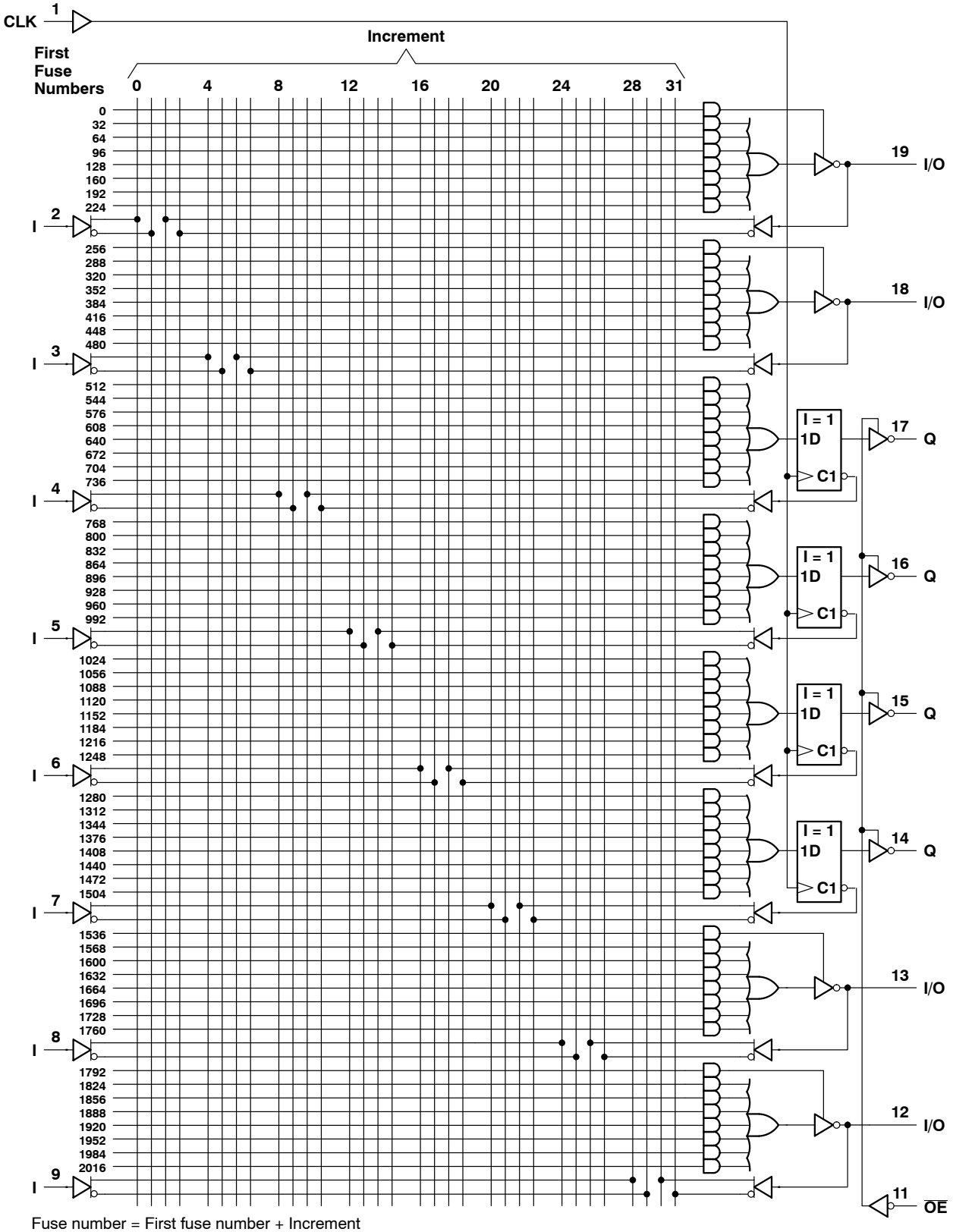

denotes fused inputs

## TIBPAL16L8-15M logic diagram (positive logic)



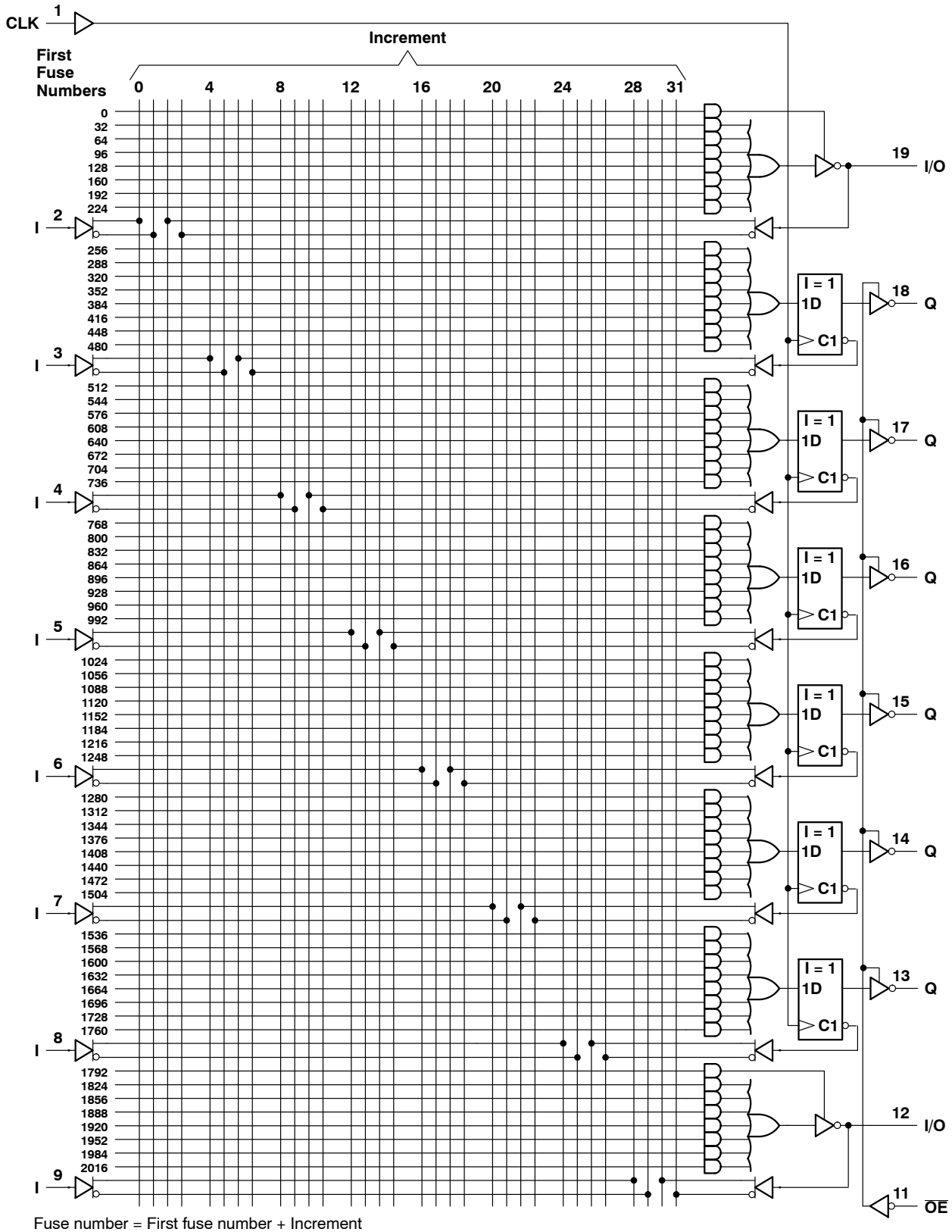

Fuse number = First fuse number + Increment

## TIBPAL16R4-15M logic diagram (positive logic)



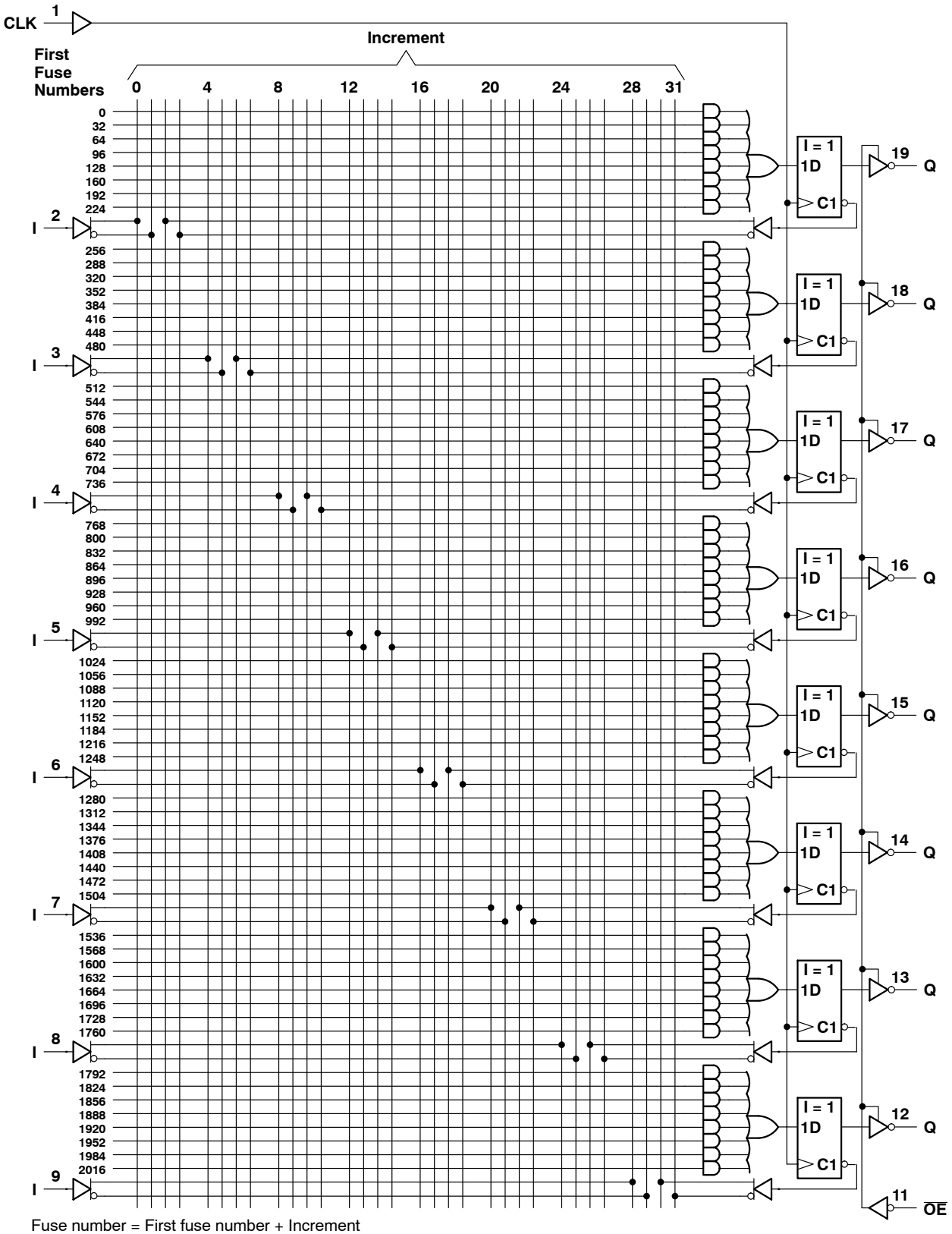

Fuse number = First fuse number + Increment

## TIBPAL16R6-15M logic diagram (positive logic)




Fuse number = First fuse number + Increment

## TIBPAL16R8-15M logic diagram (positive logic)




Fuse number = First fuse number + Increment

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: These ratings apply except for programming pins during a programming cycle.

## recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 5.5 | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | –2 | mA |
| $I_{OL}$ | Low-level output current | | | | 12 | mA |
| $f_{clock}$ | Clock frequency | | 0 | | 50 | MHz |
| $t_w$ | Pulse duration, clock (see Note 2) | High | 9 | | | ns |
| | | Low | 10 | | | |
| $t_{su}$ | Setup time, input or feedback before clock↑ | | 15 | | | ns |
| $t_h$ | Hold time, input or feedback after clock↑ | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | –55 | 25 | 125 | °C |

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, $f_{clock}$. The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

## electrical characteristics over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | | TIBPAL16R4-15M | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | | –1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –2 mA | | 2.4 | 3.3 | | V |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 12 mA | | | 0.35 | 0.5 | V |
| $I_{OZH}$ | Outputs | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | | 20 | µA |
| | I/O ports | | | | | | 100 | |
| $I_{OZL}$ | Outputs | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | | –20 | µA |
| | I/O ports | | | | | | –250 | |
| $I_I$ | Pin 1, 11 | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V | | | | 0.2 | mA |
| | All others | | | | | | 0.1 | |
| $I_{IH}$ | Pin 1, 11 | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | | 50 | µA |
| | I/O ports | | | | | | 100 | |
| | All others | | | | | | 25 | |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | | –0.25 | mA |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | –30 | | –250 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0, | Outputs open | | 170 | 220 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set $V_O$ at 0.5 V to avoid test equipment degradation.

## electrical characteristics over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | | TIBPAL16L8-15M TIBPAL16R6-15M TIBPAL16R8-15M | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | | –1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –2 mA | | 2.4 | 3.3 | | V |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 12 mA | | | 0.35 | 0.5 | V |
| $I_{OZH}$ | Outputs | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | | 20 | μA |
| | I/O ports | | | | | | 100 | |
| $I_{OZL}$ | Outputs | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | | –20 | μA |
| | I/O ports | | | | | | –250 | |
| $I_I$ | Pin 1, 11 | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V | | | | 0.2 | mA |
| | All others | | | | | | 0.1 | |
| $I_{IH}$ | Pin 1, 11 | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | | 50 | μA |
| | I/O ports | | | | | | 100 | |
| | All others | | | | | | 20 | |
| $I_{IL}$ | I/O ports | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | | –0.25 | mA |
| | All others | | | | | | –0.2 | |
| $I_{OS}$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.5 V | | –30 | | –250 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0, | Outputs open | | 170 | 220 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set $V_O$ at 0.5 V to avoid test equipment degradation.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$§ | | | | 50 | | | MHz |
| $t_{pd}$ | I, I/O | O, I/O | | | 8 | 15 | ns |
| $t_{pd}$ | CLK↑ | Q | R1 = 390 Ω, | | 7 | 12 | ns |
| $t_{en}$ | OE↓ | Q | R2 = 750 Ω, | | 8 | 12 | ns |
| $t_{dis}$ | OE↑ | Q | See Figure 1 | | 7 | 12 | ns |
| $t_{en}$ | I, I/O | O, I/O | | | 8 | 15 | ns |
| $t_{dis}$ | I, I/O | O, I/O | | | 8 | 15 | ns |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Maximum operating frequency and propagation delay are specified for the basic building block. When using feedback, limits must be calculated accordingly.

## programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

The TIBPAL16R4-15M with date codes prior to 9616A must be programmed according to programming algorithms/specifications corresponding to the TIBPAL16R4-12C. The TIBPAL16R4-15M with date code 9616A or newer must be programmed according to programming algorithms/specifications corresponding to the TIBPAL16R4-10C.

Regardless of date code, the TIBPAL16L8-15M, TIBPAL16R6-15M, and TIBPAL16R8-15M must be programmed according to programming algorithms/specifications corresponding to the TIBPAL16L8-12C, TIBPAL16R6-12C, and TIBPAL16R8-12C, respectively. Failure to do so may damage the devices.

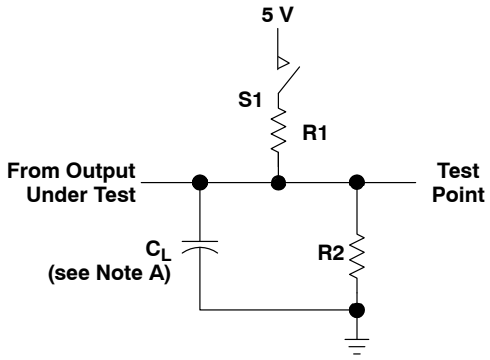
Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

**Table 1. Programming Reference Table**
**(see Note 3)**

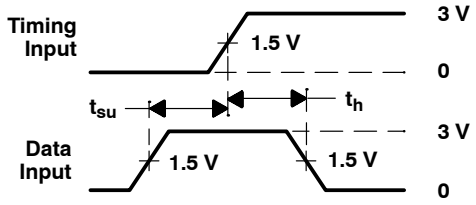
| DEVICE | DESC SMD NUMBER | FAMILY/PINOUT CODE |
|---|---|---|
| TIBPAL16L8-15MJB | 5962-8515509RA | 9A/17 |
| TIBPAL16L8-15MFKB | 5962-85155092A | 9A/717 |
| TIBPAL16L8-15MWB | 5962-8515509SA | 9A/17 |
| TIBPAL16R4-15MJB | 5962-8515512RA | A1/24 |
| TIBPAL16R4-15MFKB | 5962-85155122A | 0A1/724 |
| TIBPAL16R4-15MWB | 5962-8515512SA | A1/24 |
| TIBPAL16R6-15MJB | 5962-8515511RA | 9A/24 |
| TIBPAL16R6-15MFKB | 5962-85155112A | 9A/724 |
| TIBPAL16R6-15MWB | 5962-8515511SA | 9A/24 |
| TIBPAL16R8-15MJB | 5962-8515510RA | 9A/24 |
| TIBPAL16R8-15MFKB | 5962-85155102A | 9A/724 |
| TIBPAL16R8-15MWB | 5962-8515510SA | 9A/24 |

NOTE 3: Programming information for TIBPAL16R4-15M with date codes 9616A or newer. Programming information for TIBPAL16L8-15M, TIBPAL16R6-15M, and TIBPAL16R8-15M regardless of date code.

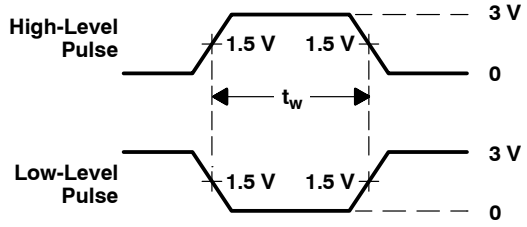
## PARAMETER MEASUREMENT INFORMATION



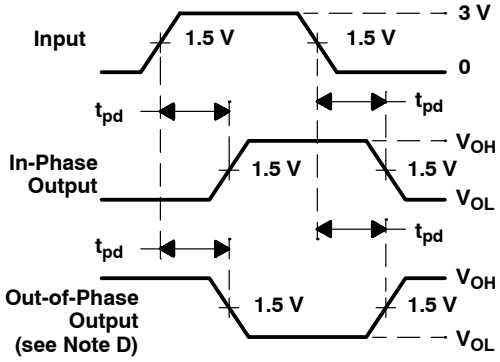

LOAD CIRCUIT FOR 3-STATE OUTPUTS



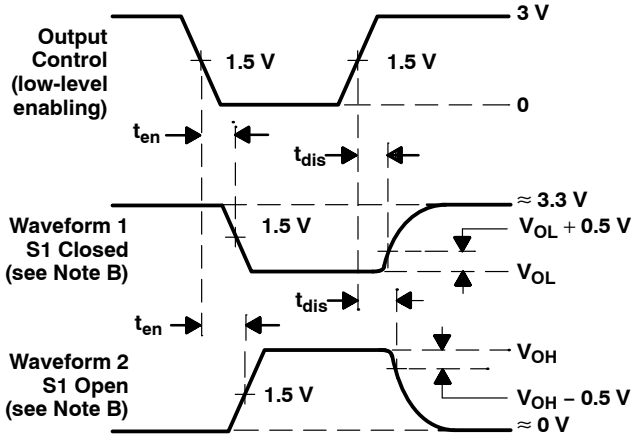

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS PULSE DURATIONS




VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. $C_L$ includes probe and jig capacitance and is 50 pF for $t_{pd}$ and $t_{en}$, 5 pF for $t_{dis}$.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 10 MHz, $t_r$ and $t_f$ ≤ 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-85155122A | NRND | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-85155122A TIBPAL16R4-15MFKB |
| 5962-8515512RA | NRND | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515512RA TIBPAL16R4-15MJB |
| 5962-8515512SA | NRND | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515512SA TIBPAL16R4-15MWB |
| TIBPAL16L8-15MJ | NRND | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | TIBPAL16L8-15MJ |
| TIBPAL16L8-15MJ.A | NRND | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | TIBPAL16L8-15MJ |
| TIBPAL16R4-15MFKB | NRND | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-85155122A TIBPAL16R4-15MFKB |
| TIBPAL16R4-15MFKB.A | NRND | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-85155122A TIBPAL16R4-15MFKB |
| TIBPAL16R4-15MJB | NRND | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515512RA TIBPAL16R4-15MJB |
| TIBPAL16R4-15MJB.A | NRND | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515512RA TIBPAL16R4-15MJB |
| TIBPAL16R4-15MWB | NRND | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515512SA TIBPAL16R4-15MWB |
| TIBPAL16R4-15MWB.A | NRND | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515512SA TIBPAL16R4-15MWB |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

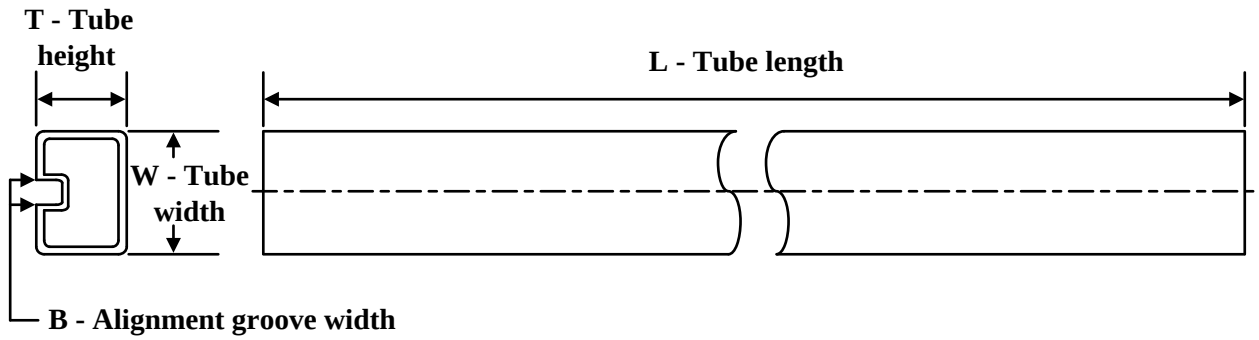
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

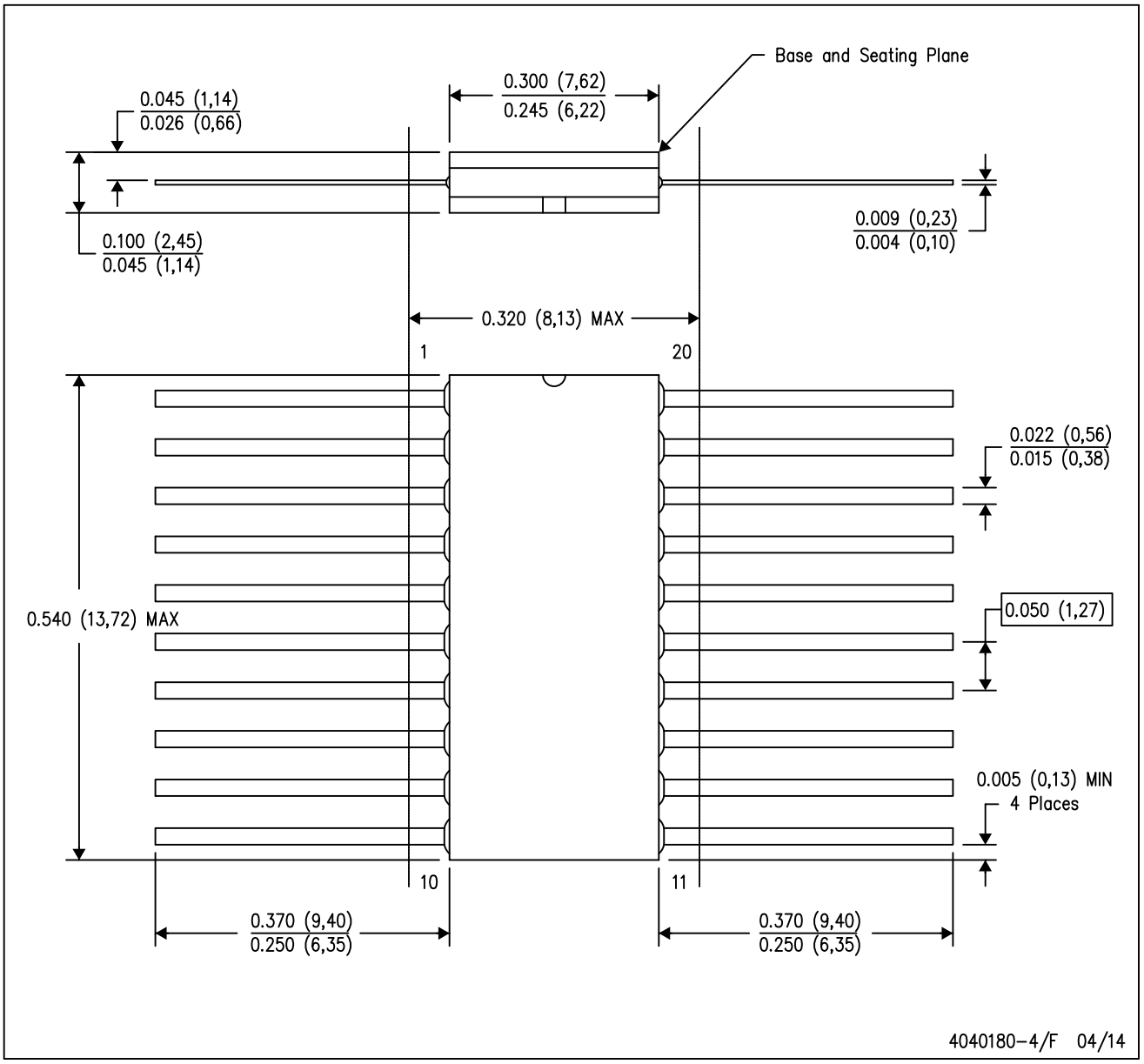
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-85155122A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-8515512SA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| TIBPAL16R4-15MFKB | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TIBPAL16R4-15MFKB.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TIBPAL16R4-15MWB | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| TIBPAL16R4-15MWB.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

W (R–GDFP–F20) CERAMIC DUAL FLATPACK

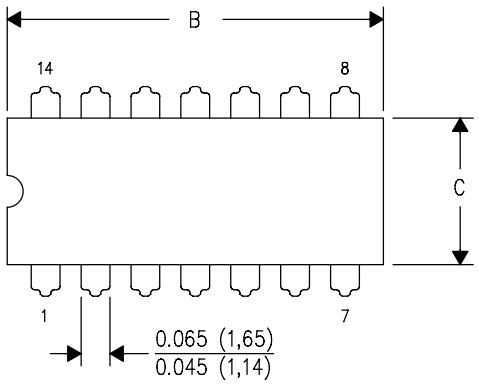



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

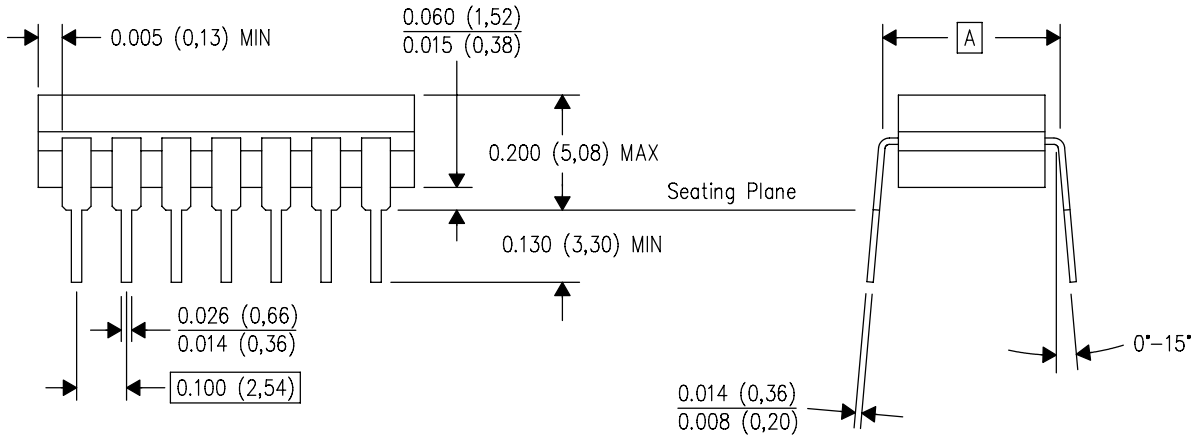
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

# GENERIC PACKAGE VIEW

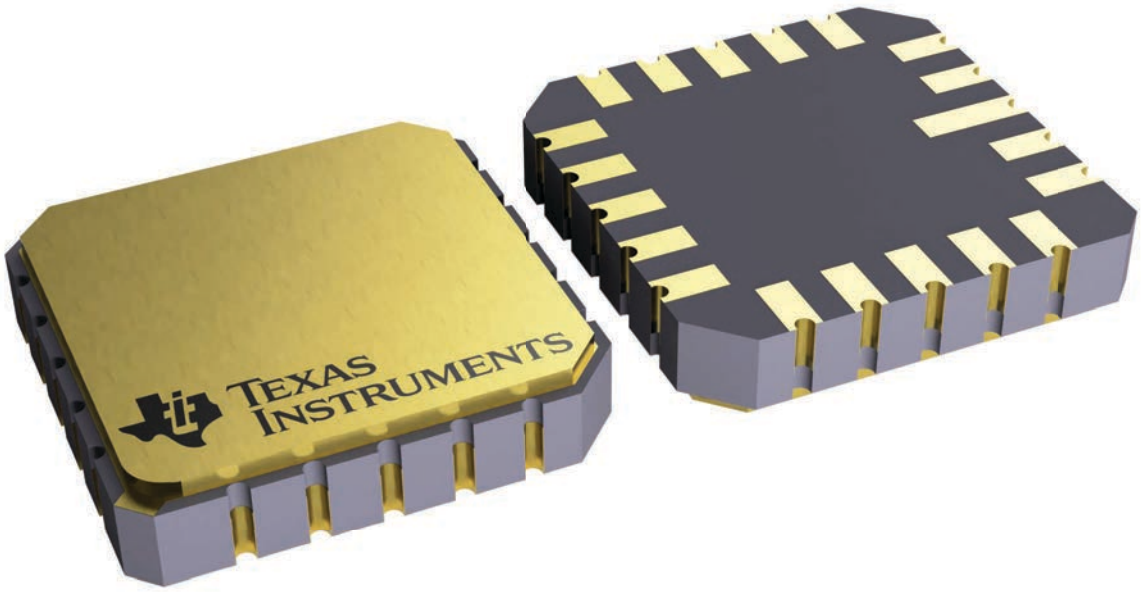
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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