



Le79252

Dual Intelligent Subscriber Line Interface Circuit
VE790 Series

APPLICATIONS

- Enables a cost effective voice solution for long or short loop applications providing POTS and integrated test capabilities
 - CO
 - DLC
 - IVD
 - Voice-enabled DSLAM
 - PBX/KTS
 - Pair gain

FEATURES

- Monitor of two-wire interface voltages and currents supports
 - Voice transmission
 - Internal ringing generation
 - Programmable DC feed characteristics
 - Independent of battery
 - Current limited
 - Selectable off-hook and ground-key thresholds
 - Subscriber line diagnostics
 - Leakage resistance
 - Loop resistance
 - Line capacitance
 - Bell capacitance
 - Foreign voltage sensing
 - Power cross and fault detection
- Supports 85 Vrms internal ringing
- 3.3 V and battery supplies
- Dual battery operation for system power saving
 - Automatic battery switching
 - Intelligent thermal management
- Compatible with inexpensive protection networks
 - Accommodates low tolerance fuse resistors or PTC thermistors
- Metering capable
 - 12 kHz and 16 kHz
 - Smooth polarity reversal
- Tip-open state supports ground start signaling
- Integrated test load switch/relay drivers
- 5 REN with DC offset

OPTIONAL FEATURES (VCP LE79112)

- DTMF detection
- Integrated test software routine
- Call aggregation
- Meets GR-844 requirements

ORDERING INFORMATION

An Le79228x ISLAC™ device must be used with this part.

Device	Package Type (Green) ¹	Packing ²
Le79252BTC	44-Pin eTQFP	Tray

1. The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.
2. For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.

DESCRIPTION

The Le79252 Dual Intelligent Subscriber Line Interface Circuit (ISLIC™) device, in combination with an Le79228x ISLAC™ device, implements the telephone line interface function. This enables the design of a low cost, high performance, fully software programmable line interface for multiple country applications worldwide. All AC, DC, and signaling parameters are fully programmable via microprocessor or GCI interfaces on the Le79228x ISLAC devices. Additionally, the Le79252 device has integrated self-test and line-test capabilities to resolve faults to the line or line circuit. The integrated test capability is crucial for remote applications where dedicated test hardware is not cost effective. When combined with Legerity's Le79112 VCP device, an optimized chip set with additional performance features can be realized.

RELATED LITERATURE

- 081256 Le79228 Quad ISLAC™ Device Data Sheet
- 080923 Le792x2/Le79228 Chip Set User's Guide
- 081152 Le79242 Dual ISLIC™ Device Data Sheet
- 081130 Le79232 Dual ISLIC™ Device Data Sheet
- 081191 Le75282 Dual LCAS Device Data Sheet

BLOCK DIAGRAM

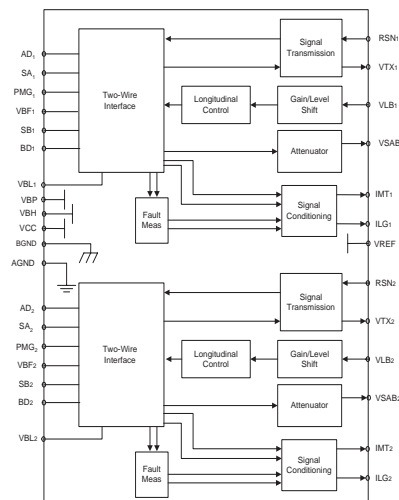


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PRODUCT DESCRIPTION

Legerity's VoiceEdge™ VE790 series chip set integrates all functions required to interface to a subscriber line. Two chip types are used to implement the line card — the Le79252 device and an Le79228x ISLAC device. These provide the following basic functions:

1. The Le79252 Dual ISLIC™ device: A high voltage, bipolar device that drives the subscriber line, maintains longitudinal balance and senses line conditions.
2. The Le79228x Quad ISLAC™ devices: Low voltage CMOS ICs that provide conversion, control and DSP functions for the Le79252 device.

A complete schematic of the line card is shown in [Application Circuit, on page 21](#).

The Le79252 device uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be controlled by the Le79228x ISLAC device to operate in different modes that control power consumption and signaling. This enables it to have full control over the subscriber loop. The Le79252 device is designed to be used exclusively with the Le79228x ISLAC devices. The Le79252 device requires only VCC and the battery supplies for its operation.

The Le79252 device implements a linear loop-current feeding method with the enhancement of intelligent thermal management. This limits the amount of power dissipated on the Le79252 device by dissipating power in external resistors in a controlled manner.

The Le79252 is designed to provide balanced ringing, with or without dc offset, to the subscriber loop.

Each ISLAC device contains high-performance circuits that provide A/D and D/A conversion for the voice, DC-feed and supervision signals. The Le79228x ISLAC devices contain a DSP core that handles signaling, DC-feed, supervision and line diagnostics for all channels.

The DSP core selectively interfaces with three types of backplanes:

- Standard PCM/MPI
- Standard GCI
- Modified GCI with a single analog line per GCI channel

The VE790 series chip set provides a complete software configurable solution to the BORSCHT functions as well as complete programmable control over subscriber line DC-feed characteristics, such as current limit and feed resistance. In addition, these chip sets provide system level solutions for the loop supervisory functions and metering. In total, they provide a programmable solution that can satisfy worldwide line card requirements by software configuration.

Software programmed filter coefficients, DC-feed data and supervision data are easily calculated with WinSLAC™ software. This PC software is provided free of charge. It allows the designer to enter a description of system requirements. WinSLAC then computes the necessary coefficients and plots the predicted system results.

The Le79252 device interface unit inside the Le79228x ISLAC device processes information regarding the line voltages, loop currents and battery voltage levels. These inputs allow the Le79228x ISLAC device to place several key Le79252 device performance parameters under software control.

The main functions that can be observed and/or controlled through the Le79228x ISLAC device backplane interface are:

- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- Metering signal
- Longitudinal operating point
- Subscriber line voltage and currents
- Ring trip detection
- Abrupt and smooth battery reversal
- Subscriber line impedance matching
- Transmit and receive paths frequency response
- 4-wire to 2-wire hybrid impedance balance, or transhybrid loss
- Ringing generation
- Sophisticated line and circuit tests

To accomplish these functions, the Le79252 device collects the following information and feeds it, in analog form, to the Le79228x ISLAC device:

- The metallic (IMTi) and longitudinal (ILGi) loop currents
- The AC (VTXi) and DC (VSABi) loop voltage

The outputs supplied by the Le79228x ISLAC devices to the Le79252 device are then:

- A voltage (VHL_i^*) that provides control for the following high-level Le79252 device outputs:
 - DC loop current
 - Internal ringing signal
 - 12 or 16 kHz metering signal
- A low-level voltage proportional to the voice signal ($VOUT_i$)
- A voltage that controls longitudinal offset for test purposes (VLB_i)

The Le79228x ISLAC devices perform the conversion and filtering functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance and provide frequency attenuation adjustment (equalization) of the receive and transmit paths. Adaptive transhybrid balancing is also included. All programmable digital filter coefficients can be calculated using WinSLAC software. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or μ -law.

Besides the ISLAC device functions, the VE790 series chip set provides all the sensing, feedback, and clocking necessary to completely control Le79252 device functions with programmable parameters. System-level parameters under programmable control include active loop current limits, feed resistance, and feed mode voltages.

The Le79228x ISLAC devices supply complete mode control to the Le79252 device using the control bus (P1-P3) and tri-level load signal (LD_i).

The VE790 series chip set provides extensive loop supervision capability including off-hook, ring trip and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce.

For subscriber line diagnostics, AC and DC line conditions can be monitored using built-in test tools. Measured parameters can be compared to programmed threshold levels to set a pass/fail bit. The user can choose to send the actual measurement data directly to a higher level processor by way of the PCM voice channel. Both longitudinal and metallic resistance and capacitance can be measured, which allows leakage resistance, line capacitance, and telephones to be identified.

***Note:**

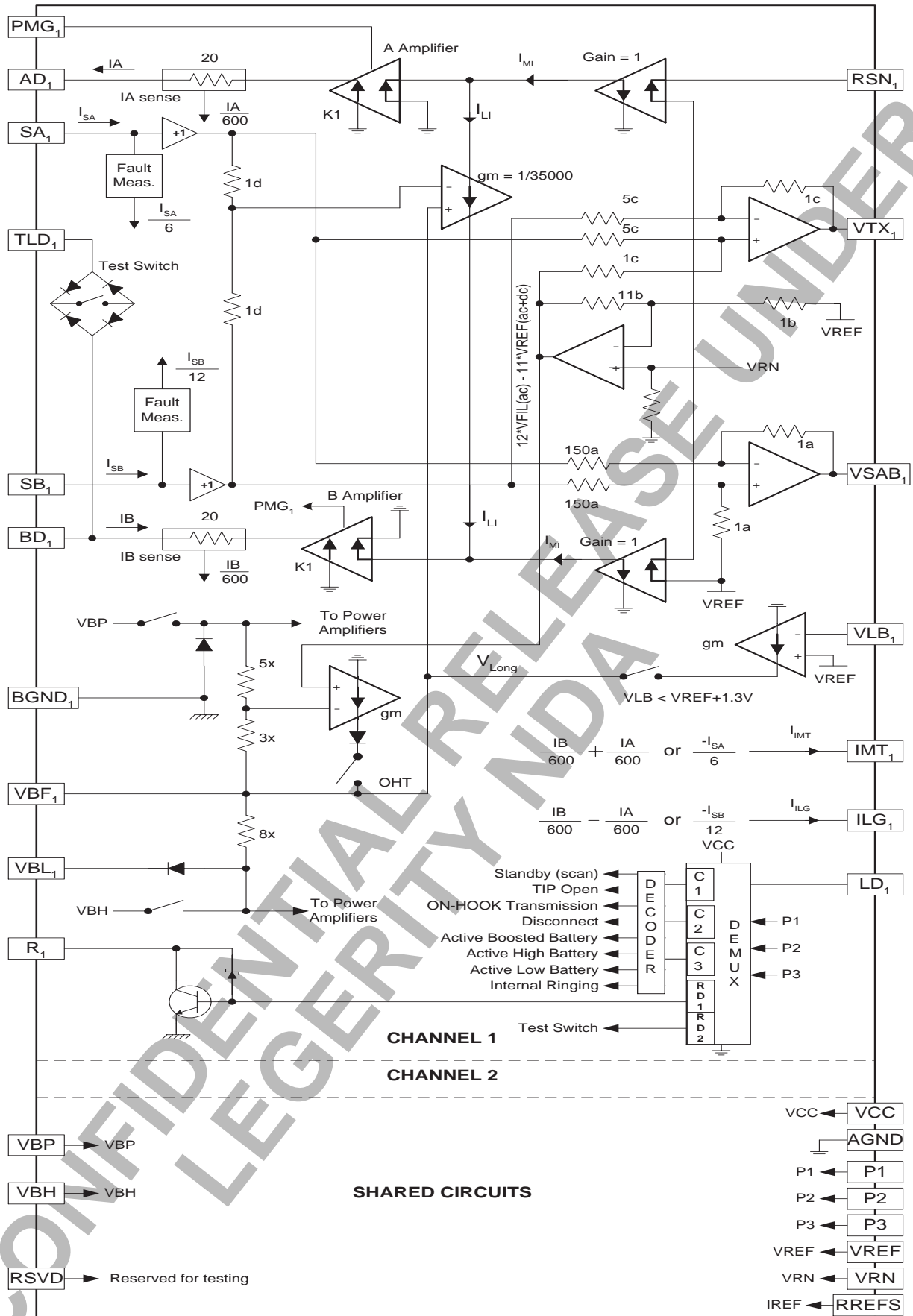
i = channel number

OPTIONAL VCP FEATURES

Optional Voice Control Processor (VCP) features provide the following solutions to the VE790 series intelligent chip sets:

- Integrated test software routines
- DTMF detection
- Aggregated codec/filter control

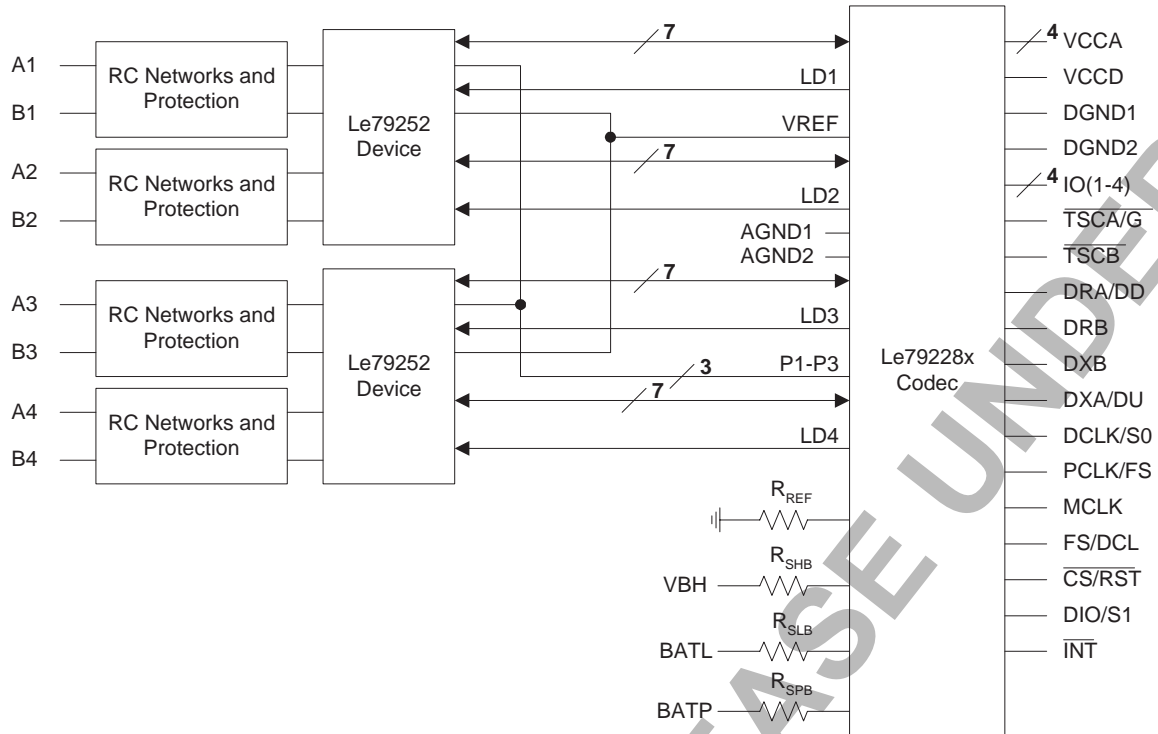
Figure 1. Le79252 Device Internal Block Diagram



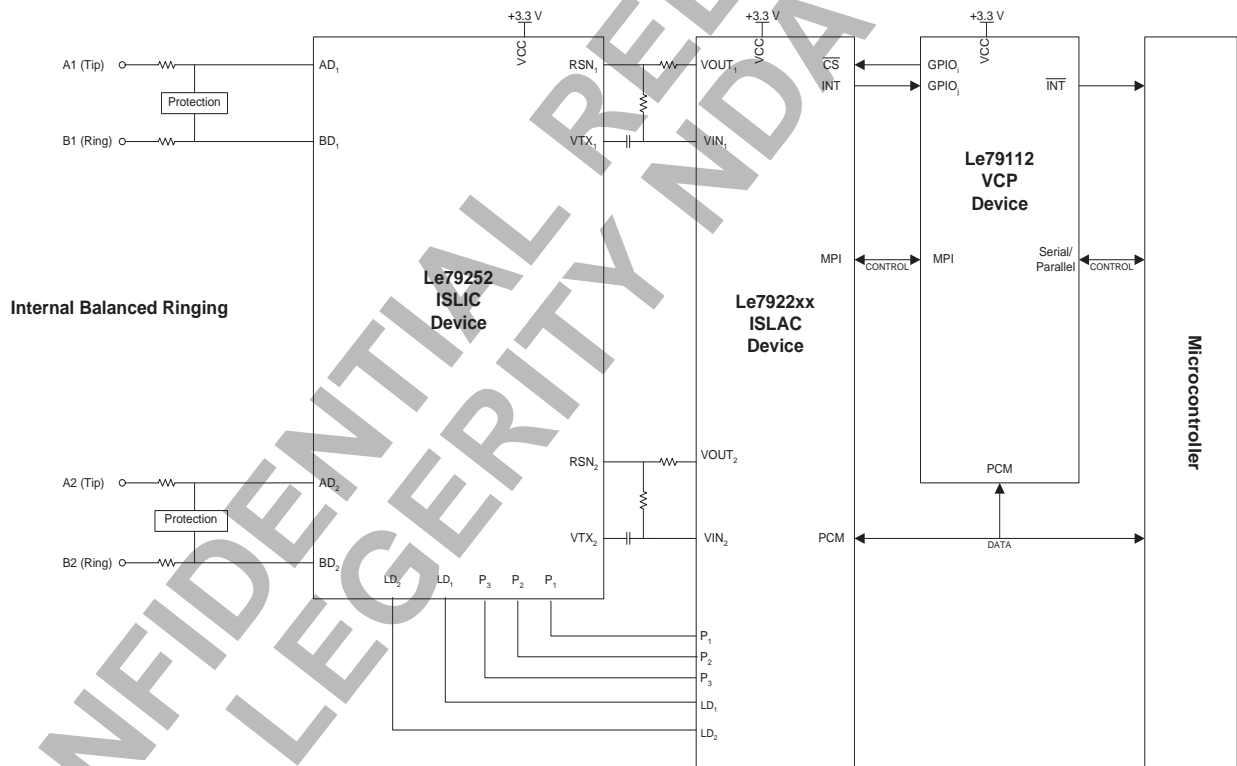
FEATURES OF THE VoiceEdge™ VE790 SERIES CHIP SET

- Performs all battery feed, ringing, signaling, hybrid and test (BORSCHT) functions
- Two chip solution supports high density, multi-channel architecture
- Single hardware design meets multiple country requirements through software programming of:
 - Ringing waveform and frequency
 - DC loop-feed characteristics and current-limit
 - Loop-supervision detection thresholds
 - Off-hook debounce circuit
 - Ground-key and ring trip filters
 - Off-hook detect de-bounce interval
 - Two-wire AC impedance
 - Transhybrid balance impedance
 - Transmit and receive gains
 - Equalization
 - Digital I/O pins
 - A-law/ μ -law and linear selection
- Supports internal balanced ringing
 - Self-contained ringing generation and control
 - Integrated ring trip filter and software enabled manual or automatic ring trip mode
- Supports DTMF generation with Le79228x ISLAC and DTMF detection with Le79112 VCP
- Supports metering generation with envelope shaping
- Smooth or abrupt polarity reversal
- Adaptive transhybrid balance
 - Continuous or adapt and freeze
- Supports both loop-start and ground-start signaling
- Exceeds LSSGR and CCITT central office requirements
- Selectable PCM or GCI interface
 - Supports most available master clock frequencies from 512 kHz to 8.192 MHz
- On-hook transmission
- Power/service denial mode
- Line-feed characteristics independent of battery voltage
- Only 3.3-V and battery supplies needed
- Low idle-power per line
- Linear power-feed with intelligent power-management feature
- Compatible with inexpensive protection networks; Accommodates low-tolerance fuse resistors while maintaining longitudinal balance
- Monitors two-wire interface voltages and currents for subscriber line diagnostics
- Built-in voice path test modes
- Power-cross, fault, and foreign voltage detection
- Integrated line-test features
 - Leakage
 - Line and ringer capacitance
 - Loop resistance
- Integrated self-test features
 - Echo gain, distortion, and noise
- Guaranteed performance over commercial and industrial temperature ranges.
- One relay driver per channel
- Built-in per channel test load switch

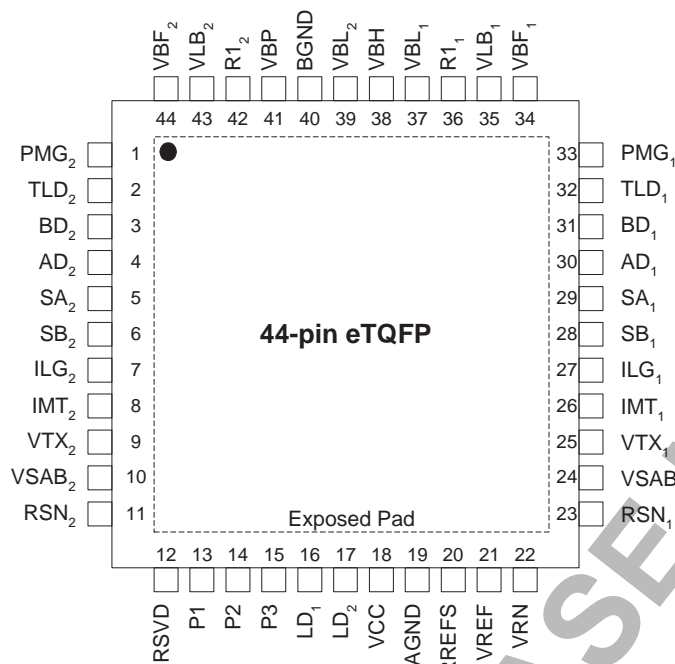
CHIP SET BLOCK DIAGRAM - FOUR CHANNEL LINE CARD EXAMPLE



VE790 SERIES CHIP SET WITH OPTIONAL VCP DEVICE



CONNECTION DIAGRAM



TOP VIEW

PIN DESCRIPTIONS

Pin Name	Type	Description
AD, BD [1,2]	Output	Provide the currents to the A and B leads of the subscriber loop.
AGND	Ground	Analog ground return for VCC.
BGND	Ground	Ground return for high, low, and positive battery supplies.
ILG [1,2]	Output	ILG is proportional to the common-mode line current ($I_A - I_B$), except in disconnect mode, where ILG is proportional to the current into grounded SB.
IMT [1,2]	Output	IMT is proportional to the differential line current ($I_A + I_B$), except in disconnect mode, where IMT is proportional to the current into grounded SA. The Le79252 device indicates thermal overload by pulling IMT to VCC.
LD [1,2]	Input	The LD pin controls the input latch and responds to a 3-level input. When the LD pin is a logic 1 ($> (V_{CC} - 1)$), the logic levels on P1–P3 latch into the Le79252 control register bits that operate the mode-decoder. When the LD pin is a logic 0 (< 0.6), the logic levels on P1–P3 latch into the Le79252 control register bits that control the relay driver and the test load switch (RD1–RD2). When the LD pin level is at $\sim V_{REF} \pm 0.3$ V, the control register contents are locked.
P1–P3	Input	Inputs to the latch for the operating-mode decoder and the relay-drivers.
PMG [1,2]	Output	Power dump resistor. If the power dump resistor is not used, tie this pin to VBL and limit VBL to -100 V.
R1 [1,2]	Output	Collector connection for relay driver. Emitter internally connected to AGND.
RREFS	Input	External resistor connected from RREF to AGND sets bias on Le79252.
RSN [1,2]	Input	The metallic current between AD and BD is equal to 500 times the current into this pin. Networks that program receive gain and two-wire impedance connect to this node. This input is at a virtual potential of VREF.
RSVD		This pin is used during Legerity testing. In the application, it must be left floating or grounded.
SA, SB [1,2]	Input	Senses the voltages on the line side of the fuse resistors at the A and B leads. External sense resistors, RSA and RSB, protect these pins from lightning or power-cross.
TLD [1,2]	Output	Resistor connected from this pin to AD is connected from AD to BD when Testload is enabled and programmed on.
VBH [1,2]		VBH (or VBL) / 2 filters. A capacitor to BGND on these pins can be used to reject common mode battery noise.
VBH	Battery (Power)	Connection to high-battery supply used for ringing and long loops. When only a single battery is available, it connects to both VBH and VBLi.
VBL [1,2]	Battery (Power)	Connection to low-battery supply used for short loops. When only a single battery is available, these pins can be connected to VBH.
VBP	Battery (Power)	Positive battery.
VCC	+3.3 Power Supply	Positive supply for low voltage analog and digital circuits in the Le79252 device.
VLB [1,2]	Input	Sets the DC longitudinal voltage of the Le79252 device. It is the reference for the longitudinal control loop. When the VLB pin is greater than $VREF + 1.3$ V, the Le79252 device sets the longitudinal voltage to a voltage approximately half-way between the positive and negative power supply battery rails. When the VLB pin is driven to levels between 0V and $VREF + 1.3$ V, the longitudinal voltage moves away from the half-way point in proportion to the difference between VREF and VLB.
VREF	Input	The ISLAC device provides this voltage, which is used by the Le79252 device for internal reference purposes. All analog input and output signals interfacing to the ISLAC device are referenced to this pin.
VRN		VREF noise. Connect a 0.1 μ F from this pin to VREF.
VSAB [1,2]	Output	A scaled-down version of the voltage between the sense points SA and SB is present on this pin.
VTX [1,2]	Output	The voltage between this pin and VREF is a scaled down version of the voltage sensed between the SA and SB pins. An external capacitor is required to remove the dc bias before connecting that signal to the two-wire input impedance programming network going to the RSN pin. The voltage on the impedance programming network swings positive and negative with respect to VREF.
Exposed Pad	Ground	This must be electrically tied to BGND.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(T_A = 23°C)

Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage temperature	–55 to +150°C
Ambient temperature under bias; Humidity	–40 to +85°C; 5% to 95%
V _{BP} with respect to AGND	–0.4 to +110 V
V _{BP} with respect to V _{BH}	–0.4 to +160 V
V _{CC} with respect to AGND	–0.4 to +4 V
V _{BH} , V _{BL} with respect to AGND	+0.4 to –150 V
V _{BL} with respect to V _{BH}	V _{BL} ≤ V _{BH} + 1 V
BGND with respect to AGND	–3 to +3 V
Voltage on relay outputs	+6 V
Test Switch On-state current	45 mA
AD or BD: Continuous 10 ms (F = 0.1 Hz) 1 μs (F = 0.1 Hz) 250 ns (F = 0.1 Hz)	V _{BH} – 1 to V _{BP} + 1 V _{BH} – 5 to V _{BP} + 5 V _{BH} – 10 to V _{BP} + 10 V _{BH} – 15 to V _{BP} + 15
Current into SA or SB: 10 μs rise to I _{peak} 1000 μs fall to 0.5 I _{peak} ; 10000 μs fall to I = 0	I _{peak} = ±5 mA
Current into SA or SB: 2 μs rise to I _{peak} 10 μs fall to 0.5 I _{peak} ; 100 μs fall to I = 0	I _{peak} = ±12.5 mA
SA SB continuous	5 mA
Current through AD or BD	± 150 mA
P1, P2, P3, LD to AGND	–0.4 to V _{CC} + 0.4 V
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant

Thermal Resistance

The junction to air thermal resistance of the 44-pin eTQFP package is discussed in the *Thermal Management of Dual SLIC Devices* application note. This parameter is measured under free air convection conditions, with a four-layer JEDEC test board.

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane.

Package Assembly

Green package devices are assembled with enhanced, environmental, compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

Electrical Operating Ranges

Legerity guarantees the performance of this device over commercial (0°C to 70°C) and industrial (-40°C to 85°C) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Environmental Ranges

Ambient Temperature	0 to 70°C Commercial
	-40 to +85 °C extended temperature
Thermal Protection Shutdown	Min. 150°C, Typ. 165°C
Ambient Relative Humidity	15 to 85%

Electrical Ranges

V_{CC}^*	+3.3 V \pm 5%
V_{BL}^*	-15 V to VBH
V_{BH}^*	-42.5 to -145 V
VBP*	+100 V to AGND
Maximum supply voltage across device, VBP - VBH	150 V
Differential Tip to Ring loop voltage (including AC)	80 V maximum
BGND with respect to AGND	-300 to +300 mV
Load resistance on V_{TX} to V_{REF} or RSN	20 k Ω minimum

* No power-up sequencing required, except for applying ground first.

SPECIFICATIONS

Power Dissipation

Loop resistance = ∞ , V_{BL} = -36 V, V_{BH} = -60 V, V_{CC} = +3.3 V, VBP = +60 V.

Power dissipation values are per channel.

Description	Test Conditions	Min	Typ	Max	Unit
Power Dissipation Normal Polarity	On-Hook Disconnect		21	32	mW
	On-Hook Standby		45	50	
	On-Hook Transmission Fixed Longitudinal Voltage		145	170	
	On-Hook Active High Battery		165	186	
	On-Hook Active Low Battery		86	135	
	On-Hook Tip Open Supervision		45	55	
	Internal Ringing, No load		300	372	
	On-Hook Active Boosted Battery		300	372	

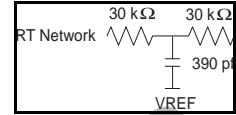
Supply Currents

Supply current values are per channel

Parameter	Min	Typ	Max	Unit
$V_{BH} = -60\text{ V}$, $V_{BL} = -36\text{ V}$, $V_{BP} = +60\text{ V}$ $V_{CC} = 3.3\text{ V}$, On-hook, no loop current, no load				
Disconnect mode:				
I_{VCC}		2.2	3.3	mA
I_{VBH}		150	250	μA
I_{VBL}		14	17	μA
I_{VBP}			100	μA
Standby state				
I_{VCC}		2.9	3.5	mA
I_{VBH}		0.59	0.63	mA
I_{VBL}		14	17	μA
I_{VBP}		1	25	μA
On-hook transmission mode, V_{BH} applied:				
I_{VCC}		3.8	5.0	mA
I_{VBH}		2.2	2.5	mA
I_{VBL}		14	17	μA
I_{VBP}		1	25	μA
Active High Battery:				
I_{VCC}		4.2	5.0	mA
I_{VBH}		2.5	2.8	mA
I_{VBL}		14	17	μA
I_{VBP}		1	25	μA
Active Low Battery:				
I_{VCC}		4.3	5.0	mA
I_{VBH}		0.5	0.65	mA
I_{VBL}		1.9	2.15	mA
I_{VBP}		1	25	μA
Tip Open Supervision:				
I_{VCC}		2.6	3.8	mA
I_{VBH}		0.6	0.68	mA
I_{VBL}		14	17	μA
I_{VBP}		1	25	μA
Internal Ringing mode:				
I_{VCC}		2.2	3.5	mA
I_{VBH}		2.6	3.0	mA
I_{VBL}		14	17	μA
I_{VBP}		2.35	3.0	mA
Active Boosted Battery:				
I_{VCC}		2.2	3.5	mA
I_{VBH}		2.6	3.0	mA
I_{VBL}		14	17	μA
I_{VBP}		2.35	3.0	mA

DC Specifications

Unless otherwise specified, test conditions are: $V_{CC} = 3.3\text{ V}$, $V_{BH} = -60\text{ V}$, $V_{BL} = -36\text{ V}$, $V_{BP} = 60\text{ V}$, $R_{RX} = 150\text{ k}\Omega$, $R_L = 600\text{ }\Omega$, $R_{SA} = R_{SB} = 200\text{ k}\Omega$, $R_{FA} = R_{FB} = 50\text{ }\Omega$, $R_T = 60\text{ k}\Omega$, $C_{AD} = C_{BD} = 22\text{ nF}$, capacitance at SA, SB, and RREFS $\leq 20\text{ pF}$, Active Low battery. For this document, currents flowing into a ISLIC pin are defined as positive and currents flowing out of a ISLIC pin are defined as negative. The currents known as I_A and I_B are currents flowing into the external protection resistors and are such that $I_A = -I_{AD}$ and $I_B = I_{BD}$. DC-feed conditions are normally set by the VE790 series ISLAC device. When the Le79252 device is tested by itself, its operating conditions must be simulated as if it were connected to an ideal VE790 series ISLAC device.



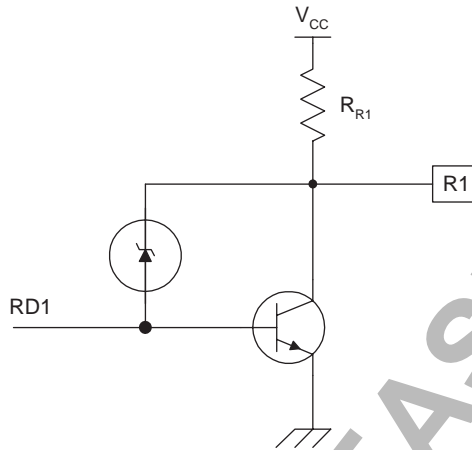
No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Two-wire Loop Voltage	Standby and OHT modes, open circuit, $-145\text{ V} < V_{BH} < -50\text{ V}$ A to GND (OHT polarity reversal) B to GND A to B	42.75		56.5 56.5 54.00	V	
		Tip Open mode, open circuit, $-145\text{ V} < V_{BH} < -50\text{ V}$ B to GND			56.5	V	
2	Common Mode Voltage	OHT mode		-24		V	
3	K1 Gain (RSN to A/B)	Incremental DC current gain K1 AD pin	490	500	510	A/A	
		BD pin	-490	-500	-510	A/A	
		Current Offset	-750		750	μA	
	Gain from A/B to VTX	VTX / (VA - VB)	0.196	0.200	0.204	V/V	
4	AD & BD pins, Feed resistance per leg	Standby mode			300	Ω	
	AD & BD pins, Leakage current per leg	Disconnect mode			5	μA	
5	Feed current limit	Feed current Active modes, $R_L = 600\text{ }\Omega$	0		75	mA	
	DC feed current limit accuracy	Feed Current = 15 to 75 mA			± 2	%	
6	DC loop range	3.17 dBm into $900\text{ }\Omega$, Active High Battery mode, -51 V battery, $I_{LOOP} = 20\text{ mA}$, plus $2 \times 50\text{ }\Omega$ protection resistors, No PPM	1930			Ω	1,6
7	Ternary input voltage boundaries for LD pin. Mid-level input source must be Vref.	Low boundary	VREF-0.3	VREF	0.6	V	
		Mid boundary	2.2		VREF+0.3	V	
		High boundary				V	
		Input high current	-20		20	μA	
		Input low current	-20		20	μA	
		Mid-level current	-20		20	μA	
8	Logic Inputs P1, P2, P3	Input high voltage	2.0			V	
		Input low voltage			0.8	V	
		Input high current	-20	0	20	μA	
		Input low current	-35	0	5	μA	
9	VREF input current	VREF = 1.4 V	-150		150	μA	
10	β , DC Ratio of VSAB to loop voltage: $\beta = \frac{V_{SAB}}{V_{SA} - V_{SB}}$	VSA - VSB = 22 V	-0.00653 (1/153)	-0.00667 (1/150)	-0.00680 (1/147)	V/V	

No.	Item	Condition	Min	Typ	Max	Unit	Note
11	VSAB output offset VSAB – VREF	VSA = VSB	–5		5	mV	
	VSAB Common Mode Rejection	VLB = VREF ± 0.5 V -20 log [(ΔVSAB output offset) / (ΔVA / 150)]	40			dB	
12	Fault Indicator Threshold	Voltage Output on IMT	2.8		VCC	V	
13	Gain from VLB pin to A or B pin, KLG	VLB = VREF ±1 V, (VLB – VREF) / [(VA + VB) / 2 - VMID]	–44.1	–45	–45.9	V/V	2, 10
	VLB Disable Threshold		VREF+1.02		VREF+1.30	V	
14	VLB pin input current	VLB = VREF ± 1 V		0	±100	μA	
15	I _{LOOP} /IMT	I _{LOOP} = (IA + IB) / 2 I _{LOOP} = 0 to ±40 mA	–294	–300	–306	A/A	
	I _{LONG} /IMT	I _{LONG} = IA – IB I _{LONG} = 0 to ±40 mA	30000			A/A	
16	I _{LONG} /ILG	I _{LONG} = IA – IB I _{LONG} = 0 to ±40 mA	588	600	612	A/A	
	I _{LOOP} /ILG	I _{LOOP} = (IA + IB) / 2 I _{LOOP} = 0 to ±40 mA	30000			A/A	
17	ISA/IMT slope	Disconnect mode ISA = –2 to +2 mA	5.88	6.00	6.12	A/A	3
18	ISB/ILG slope	Disconnect mode ISB = –2 to +2 mA	11.76	12.00	12.24		3
19	IMT output offset	Active modes OHT Disconnect	–1 –3 –1	0	1 3 1	μA	
20	ILG output offset	Active modes OHT Disconnect	–1 –3 –1	0	1 3 1	μA	

Relay Driver Specifications

Item	Condition	Min	Typ	Max	Unit	Note
On Voltage	40 mA/relay sink			0.5	V	
Relay Driver Leakage	$R_1 = 6\text{ V}$			350	μA	
Relay Driver Clamp Voltage	$I_{R1} = 30\text{ mA}$	6		17	V	
RR1 Resistance		10	15	20	$\text{K}\Omega$	

Figure 2. Relay Driver Configuration



Test Switch Specifications

Item	Condition	Min	Typ	Max	Unit	Note
Test Switch	ON-Resistance, $(V_{(25\text{ mA})} - V_{(20\text{ mA})}) / 5\text{ mA}$	10	19	30	Ω	
	On-Voltage drop at $\pm 20\text{ mA}$	-3		3	V	
	Off-state Leakage			5	μA	

Transmission Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	RSN input impedance	$\pm 200\text{ }\mu\text{A}$			12	Ω	
2	VTX output impedance	$\pm 250\text{ }\mu\text{A}$		8	32		
3	Max, AC + DC loop current	Active modes	80			mA	
4	Longitudinal AC current per wire	Active modes, $f = 15\text{ to }60\text{ Hz}$	20			mArms	6
		OHT mode	8.5				
5	A or B drive current = DC + longitudinal + signal currents		100			mAp	
	A or B drive current = ringing + longitudinal		100			mAp	
6	Longitudinal impedance, A or B to GND	Active modes	45		95	Ω	

No.	Item	Condition	Min	Typ	Max	Unit	Note
7	2-4 wire gain	V_{TX} / V_{AB} , 0 dBm, 1 kHz	-14.18	-14	-13.78	dB	
8	2-4 wire gain variation with frequency	$f = 300$ to 3400 Hz, relative to 1 kHz	-0.12	0	+0.1		
9	2-4 wire gain tracking	+3 dBm to -55 dBm Reference: -10 dBm, 1 kHz	-0.1	0	+0.1		7
10	4-2 wire gain	V_{AB} / V_{OUT} , 0 dBm, 1 kHz	-0.15	0	+0.15		
11	4-2 wire gain variation with frequency	$f = 300$ to 3400 Hz, relative to 1 kHz	-0.1	0	+0.1		
12	4-2 wire gain tracking	+3 dBm to -55 dBm Reference: -10 dBm	-0.1	0	+0.1		7
13	Total harmonic distortion level 2-wire 4-wire (VTX — VREF)	0 dBm, 1 kHz, 600 Ω	50 50			dB	
14	Idle channel noise C-message Weighted	Active modes, $R_L = 600 \Omega$ 2-wire		+7 -8	+13	dBrnC	
	Psophometric Weighted	4-wire		-83	-77	dBrnC	6
		2-wire		-98		dBmp	6
	Psophometric Weighted with metering	4-wire 2-wire, metering 2.5 Vrms			-65	dBmp	7
15	Longitudinal balance (IEEE method)	Longitudinal to metallic, Active modes, $I_{LOOP} = 40$ mA $T_A = -40^\circ\text{C}$ to 85°C $f = 200$ to 1000 Hz $f = 3000$ Hz	58 56	66		dB	4,8
		Metallic to longitudinal (HARM) $f = 200$ to 3000 Hz	40				
16	PSRR (VBH, VBL, VBP)	$f = 50$ to 3400 Hz $f = 3.4$ to 50 kHz	40	25		dB	7
	PSRR (VCC)	$f = 50$ to 3400 Hz $f = 3.4$ to 50 kHz	40 25				
17	BGND Rejection	$f = 50$ to 3400 Hz $f = 3.4$ to 50 kHz	45 25			dB	7
18	Metering Total Harmonic Distortion	$f = 12$ kHz or 16 kHz, 2.8 Vrms at A/B, metering load = 200 Ω , $I_{LOOP} = 20$ mA	40			dB	7
19	Crosstalk between channels	$f = 1$ kHz, 0dBm			-80	dB	5, 7
		$f = 12$ kHz, 16 kHz			-60		7
20	EMC, per ETSI EN 300 386 V1.3.1 (2001-09) and EN 61000-4-6	3 Vrms, 80% modulated with 1 kHz, 150 kHz – 80 MHz, 150 Ω common mode source impedance (300 Ω per leg)			-40	dBm	7

Internal Ringing Specifications

Item	Condition	Min	Typ	Max	Unit	Note
Ringing Voltage	5 REN 1386 Ω + 40 μF load, 1440 Ω loop, 2 x 50 Ω protection resistors, -140 V battery potential with -21 V dc offset	40			Vrms	6
Distortion	75 Vrms ringing		0.1	2.0	%	7

Ring Trip Specifications

Item	Condition	Min	Typ	Max	Unit	Note
Ring Trip Time	$f = 20 \text{ Hz}$, 300Ω applied to a loop $\leq 1500 \Omega$			150	ms	7, 9

Current-Limit Behavior

ISLIC Mode	Condition	Min	Typ	Max	Unit	Note
Tip Open	B Short to GND	20		50		
Standby	Short A-to-VBH Short B-to-GND	20 20		50 50	mA	
Active Ringing	VE790 series SLAC generating internal ringing	100				

Thermal Shutdown Fault Indications

Fault	Indication
No Fault	IMT operates normally ($V_{REF} \pm 1 \text{ V}$)
Thermal Shutdown	IMT above 2.8 V ; ILG operates normally, Device enters disconnect like mode (loop current denied), R1 and TLD outputs operate normally

Notes:

1. An overhead calibrate procedure will be instituted at call set-up.
2. Compliance is $V_{REF} = \pm 1 \text{ V}$. If $V_{LB} > +2.7 \text{ V}$, then this pin is disabled. If $V_{LB} = V_{REF} \pm 1 \text{ V}$, then offset is $\pm 5 \text{ mV}$.
3. Offset to be calibrated within 0.5 V .
4. Feed resistors are inside ISLIC device voltage sense feedback.
5. Both channels Active, or one channel Active off-hook and one channel in Standby on-hook. No impulse noise is recorded on adjacent channels using a 35 dBmC threshold. Also, in presence of dial pulse, no impulse noise is recorded on adjacent channels using a 35 dBmC threshold.
6. Guaranteed by correlation to other production tests.
7. Guaranteed by design or characterization.
8. Tested at 1 kHz only.
9. Shall not trip ringing ($f = 17$ to 23 Hz) when an alerting signal is applied to a termination of $10 \text{ k}\Omega$ in parallel with $8 \mu\text{F}$ or 100Ω in series with $2 \mu\text{F}$, either termination applied on A-to-B directly at the output of the line unit: (0Ω loop).
10. VMID is the common-mode output voltage $(V_A + V_B) / 2$ obtained under the condition of $V_{LB} = V_{CC}$.

OPERATING MODES

The Le79252 device receives multiplexed control data on the P1, P2 and P3 pins. The LD pin then controls the loading of P1, P2, and P3 values into the proper bits in the Le79252 device control register. When the LD pin is less than 0.3 V below V_{REF} ($< (V_{REF} - 0.3 \text{ V})$), P1–P2 must contain data for the relay and test load switch control bits RD1 and RD2. These are latched into the first two bits in the Le79252 device control register. When the LD pin is more than 0.3 V above V_{REF} , P1–P3 must contain Le79252 device control data C1, C2, and C3, which are latched into the last three bits of the Le79252 device control register. Connecting the LD pin to V_{REF} locks the contents of the Le79252 device control register.

The operating mode of the Le79252 device is determined by the C1, C2, and C3 bits in the control register of the Le79252 device. [Table 1](#) defines the Le79252 device operating modes set by these signals.

Under normal operating conditions, the Le79252 device does not have active relays. The Le79252 device to Le79228x ISLAC device interface is designed to allow continuous real-time control of the relay drivers to avoid incorrect data loads to the relay bit latches of the Le79252 devices.

Table 1. Operating Modes

C3	C2	C1	Operating Mode
0	0	0	Standby (Scan)
0	0	1	TIP Open
0	1	0	ON-HOOK Transmission
0	1	1	Disconnect
1	0	0	Active Boosted Battery
1	0	1	Active High Battery
1	1	0	Active Low Battery
1	1	1	Internal Ringing

Operating Mode Descriptions

Operating Mode	Battery Voltage Selection	Description
Standby (Scan)	VBH and BGND	<ul style="list-style-type: none"> AD and BD amplifiers are turned OFF. AD output is connected to a voltage near BGND through a resistor. BD output is connected to a voltage clamp circuit through a resistor. The clamp circuit voltage is defined in item 1 of the DC specification table. The clamp circuit is powered from VBH. Line supervision is active. The currents out of IMT and ILG are proportional to currents from the A and B amplifiers. VSAB is not active. Current limit of 30 mA is provided on both A and B lines.
TIP Open	VBH and BGND	<ul style="list-style-type: none"> A (TIP) lead is open ($> 150 \text{ k}\Omega$) in the voltage range of VBH and BGND. BD output is connected to a voltage clamp circuit through a resistor. The clamp circuit voltage is defined in item 1 of the DC specification table. The clamp circuit is powered from VBH. Current limit of 30 mA typical is provided on B (RING) line. ILG current sense circuit is active.
ON-HOOK Transmission	VBH and BGND	<ul style="list-style-type: none"> In this mode the ISLIC provides a fixed longitudinal voltage as defined in item 2 of the DC specification table. The A and B amplifiers are fully active and powered from VBH and BGND. This active mode should be used if loop voltage is to be derived from a battery voltage between -56.5 V and -145 V
Disconnect	VBH and VBP	<ul style="list-style-type: none"> The A and B amplifiers are turned OFF and are high impedance to any external voltage between VBH and BGND. The remaining active circuits are powered from VBH. SA and SB pins are low impedance and clamped at approximately AGND. The currents out of IMT and ILG are proportional to voltages on the A and B leads.
Active Boosted Battery	VBH and VBP	<ul style="list-style-type: none"> The A and B amplifiers are fully active and powered from VBH and VBP. This mode can be used for extended loop range applications.
Active High Battery	VBH and BGND	<ul style="list-style-type: none"> The A and B amplifiers are fully active and powered from VBH and BGND. This mode can be used for long loop applications.
Active Low Battery	VBL and BGND	<ul style="list-style-type: none"> In this mode the A and B amplifiers are powered from VBL and BGND supply to save power.
Internal Ringing	VBH and VBP	<ul style="list-style-type: none"> In this mode the A and B amplifiers are powered from VBH and VBP. Balanced ringing signal is generated at AD and BD pins and controlled by the SLAC device. The VTX output is disabled.

Driver Descriptions

Driver	Description
R1	A logic 1 on RD1 (from the P1 pin of the Le79228x ISLAC device) turns the R1 driver on and operates a relay connected between the R1 pin and a positive voltage. RD1 is gated off during thermal shutdown.
TLD	A logic 1 on RD2 (from the P2 pin of the Le79228x ISLAC device) turns the Testload driver on and routes current from the Testload pin to the BD pin. RD2 is gated off during thermal shutdown. Connect a test load between TLD and the AD (Tip) lead. This technique avoids the use of a relay to connect a test load. However, it does not isolate the subscriber line from the line card. The test load must be connected to the Le79252 device side of the protection resistor to avoid damage to the TLD driver.

Control bits RD1 and RD2 do not affect the operating mode of the Le79252 device.

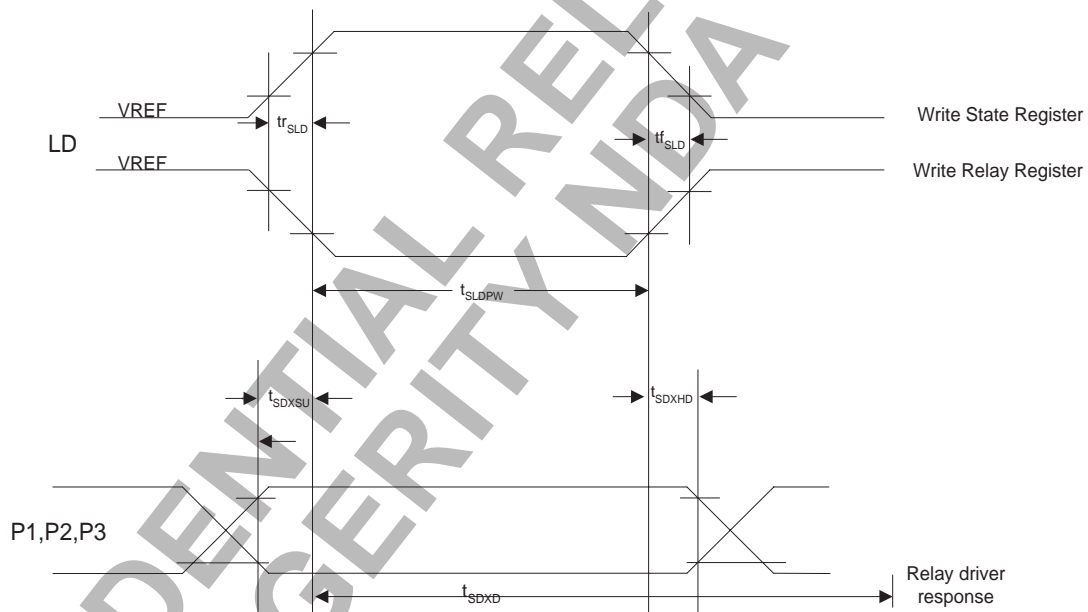
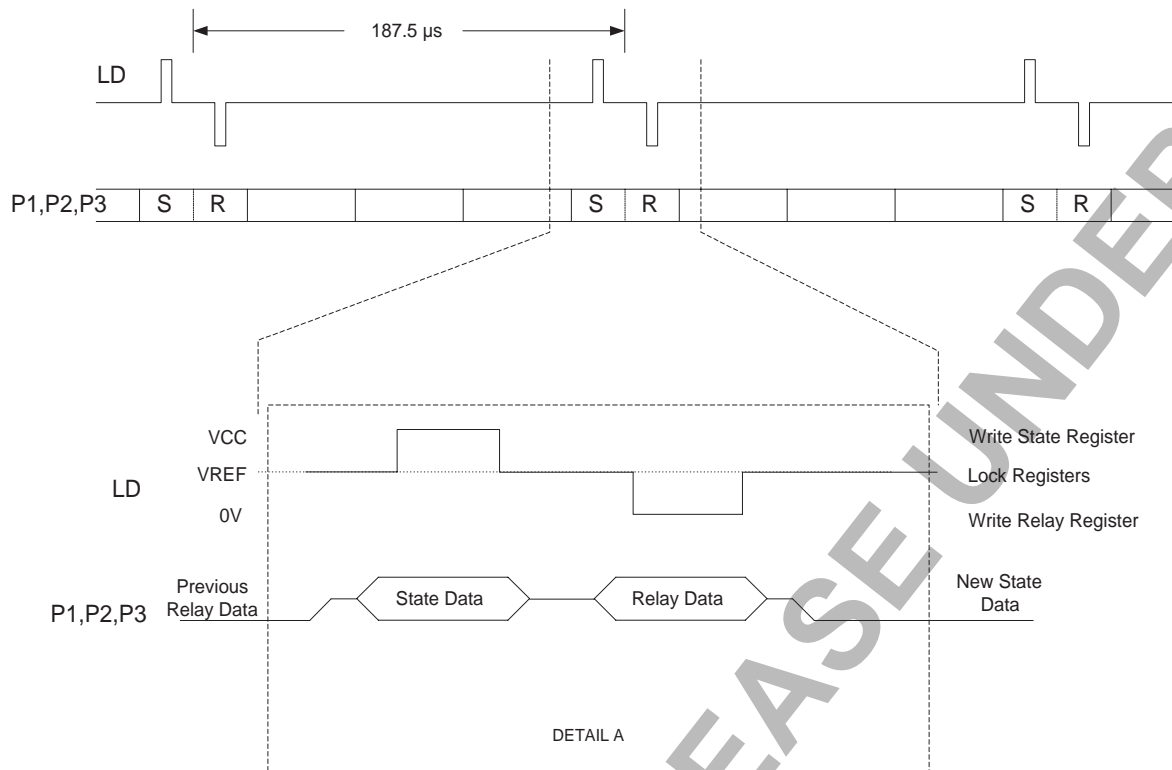
TIMING SPECIFICATIONS

Symbol	Signal	Parameter	Min	Typ	Max	Unit
trSLD	LD	Rise time Le79252 device LD pin			2	μ s
tfSLD	LD	Fall time Le79252 device LD pin			2	
tSLDPW	LD	LD minimum pulse width	3			
tSDXSU	P1,P2,P3	P1–3 data Setup time	4.5			
tSDXHD	P1,P2,P3	P1–3 data hold time	4.5			
tSDXD	P1,P2,P3	Max P1–3 data delay			5	

Notes:

- The P1–3 pins are updated continuously during operation by the LD signal.
- When writing to the Le79252 device registers, the sequence is:
 - Set LD pin to mid-state.
 - Place appropriate data on the P1–3 pins.
 - Assert the LD pin to High or Low to write the proper data.
 - Return LD pin to mid-state.
- Le79252 device registers are refreshed at 5.33 kHz when used with a VE790 series ISLAC device.

WAVEFORMS



APPLICATION CIRCUIT

Figure 3. Internal Ringing Line Card Schematic

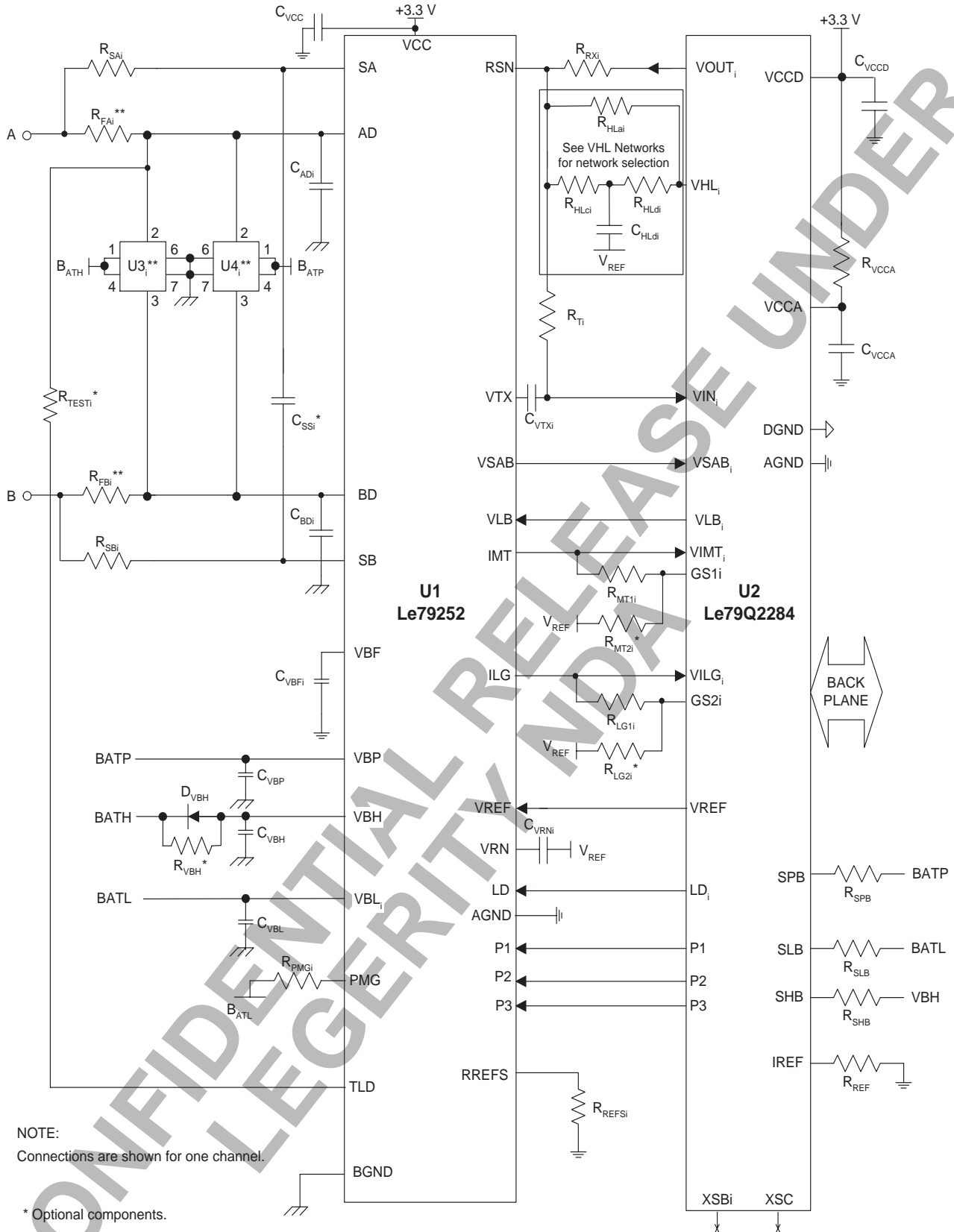
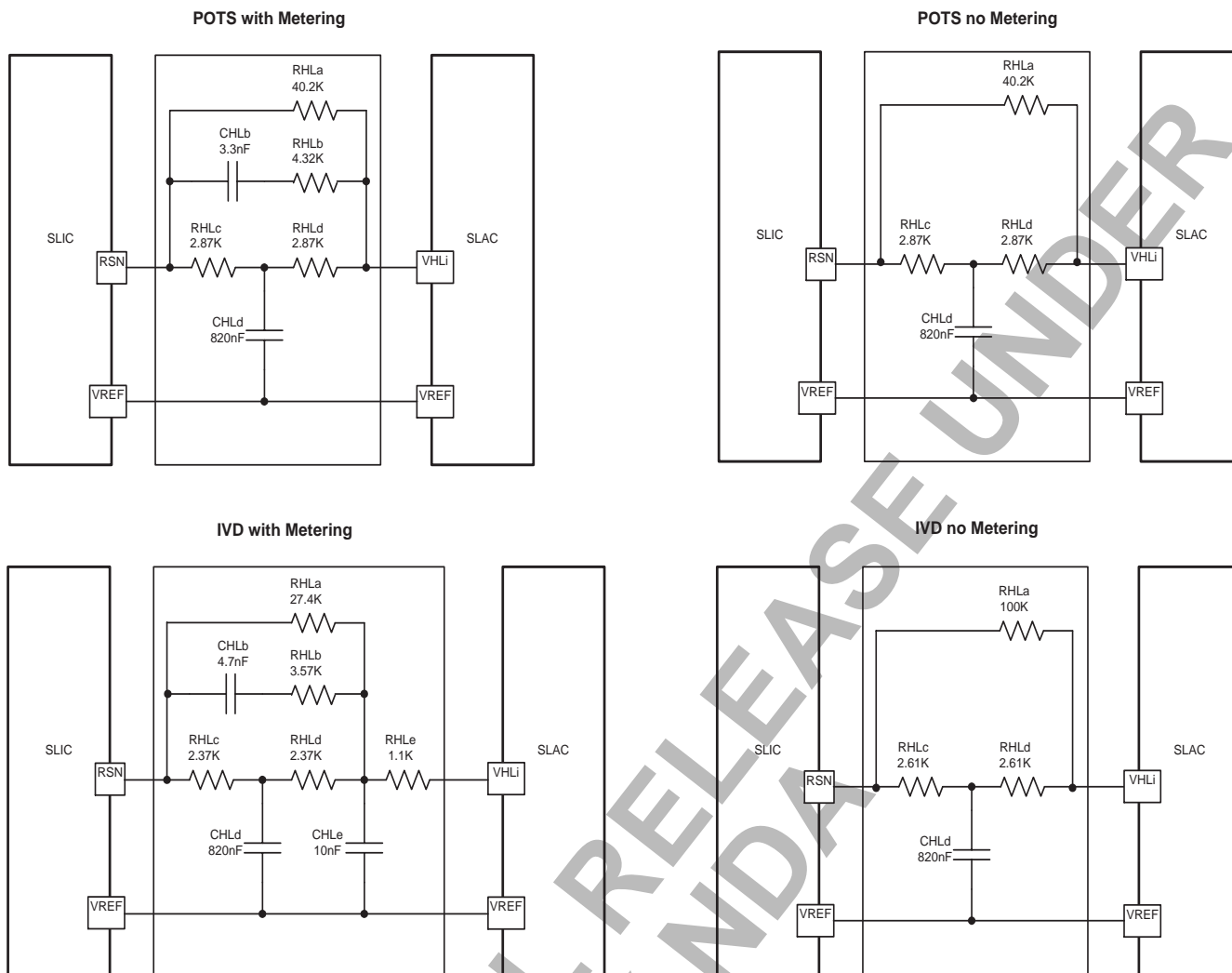


Figure 4. VHL networks for POTS and IVD Applications With and Without Metering



LINE CARD PARTS LIST

The following list defines the parts and part values required to meet target specification limits for channel i of the line card ($i = 1, 2, 3, 4$ or $i = 1, 2$).

Item	Type	Value	Tol.	Rating	Comments	Optional Components
U1 _i	Le79252 device				Dual ISLIC device	
U2	Le79228x				ISLAC device	
U3 _i	TISP8200M				Bourns® Negative Overvoltage Protector	
U4 _i	TISP8201M				Bourns® Positive Overvoltage Protector	
D _{VBH}	Diode	100 mA		100 V		
R _{VBH}	Resistor	1 k Ω	5%	1/16 W		Required if R _{FAi} , R _{FBi} are PTC components and R _{SAi} , R _{SBi} sense resistors are wired as shown in Figure 3
R _{FAi} , R _{FBi}	Resistor	50 Ω	2%	2 W	Fusible resistors or PTC protection resistors	
R _{SAi} , R _{SBi}	Resistor	200 k Ω	1%	3/4 W	Sense resistors, pulse withstanding component	
R _{Ti}	Resistor	80.6 k Ω	1%	1/16 W	Impedance control resistor	
R _{RXi}	Resistor	90.9 k Ω	1%	1/16 W	Receive path gain resistor	
C _{VTXi}	Capacitor	100 nF	10%	50 V		
R _{REF}	Resistor	69.8 k Ω	1%	1/16 W	Current reference setting resistor	
R _{SHB} , R _{SLB} , R _{SPB}	Resistor	750 k Ω	1%	1/16 W	Battery sense resistors	
R _{HLa_i}	Resistor	40.2 k Ω	1%	1/16 W	Feed resistor, see VHL networks for IVD value	
R _{H_Lbi}	Resistor	4.32 k Ω	1%	1/16 W	Metering resistor	Required for metering
R _{H_Lci} , R _{H_Ldi}	Resistor	2.87 k Ω	1%	1/16 W	Feed resistors, see VHL networks for IVD values	
C _{H_Lbi}	Capacitor	3.3 nF	10%	10 V	Metering capacitor - Not Polarized	Required for metering
C _{H_Ldi}	Capacitor	0.82 μ F	10%	10 V	Feed capacitor -Ceramic	
C _{SSi}	Capacitor	33 or 56 pF	5%	100 V	Metering capacitor -Ceramic, use 33 pF for 3.2 Vrms max. or 56 pF for 5.0 Vrms max. metering.	Only required for metering > 2.2 Vrms, otherwise omit
R _{MT1i}	Resistor	3.01 k Ω	1%	1/16 W	Metallic loop current gain resistor	
R _{MT2i}	Resistor	75 k Ω	1%	1/16 W	Metallic loop current resistor for high gain selection	Required for testing, tie RMT1i to VREF if not used
R _{LG1i}	Resistor	6.04 k Ω	1%	1/16 W	Longitudinal loop current gain resistor	
R _{LG2i}	Resistor	150 k Ω	1%	1/16 W	Longitudinal loop current resistor for high gain selection	Required for testing, tie RLG1i to VREF if not used
R _{REFSi}	Resistor	56.2 k Ω	1%	1/16 W		
R _{PMGi}	Resistor	510 Ω	5%	1 W	Value should be adjusted to suit application	
R _{TESTi}	Resistor	2 k Ω	1%	1 W	Test load	Optional for testing
C _{ADi} , C _{B_Di}	Capacitor	15 nF	10%	200 V	Ceramic, X7R dielectric	
C _{BATH} , C _{BATL} , C _{BATP}	Capacitor	100 nF	20%	100 V	Ceramic	
C _{VBFi}	Capacitor	1 nF	20%	100 V	Ceramic	
C _{VCC}	Capacitor	100 nF	20%	10 V		

C _{VCCD}	Capacitor	100 nF	20%	10 V		
C _{VCCA}	Capacitor	33 μ F	20%	6.3 V	Tantalum	
R _{VCCA}	Resistor	3.3 Ω	1%	1/16 W		
C _{VRNi}	Capacitor	100 nF	20%	10 V		

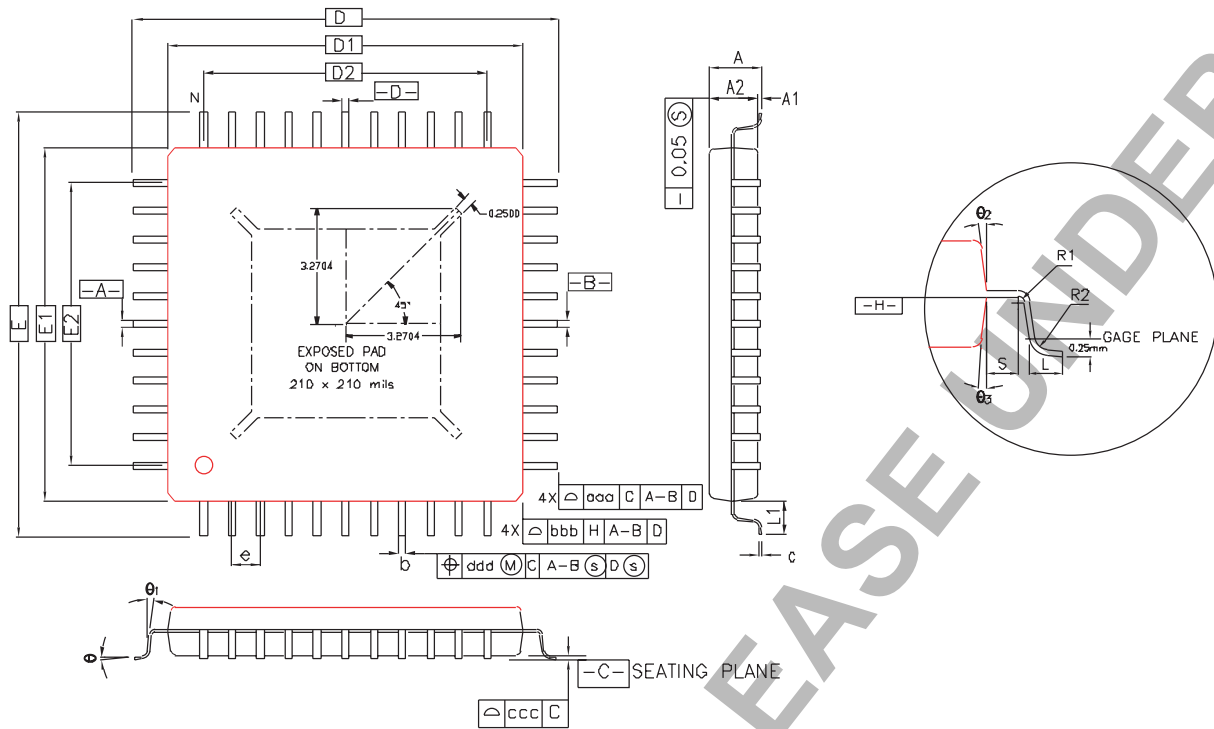
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PHYSICAL DIMENSIONS

44-Pin eTQFP



SYMBOL	MIN	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
D	—	12.00 BSC.	—
D1	—	10.00 BSC.	—
E	—	12.00 BSC.	—
E1	—	10.00 BSC.	—
R2	0.08	—	0.20
R1	0.08	—	—
θ	0°	3.5°	7°
θ_1	0°	—	—
θ_2	11°	12°	13°
θ_3	11°	12°	13°
c	0.09	—	0.20
L	0.45	0.60	0.75
L1	—	1.00 REF.	—
S	0.20	—	—
b	0.17	0.20	0.27
e	—	0.80 BSC.	—
D2	—	8.00	—
E2	—	8.00	—
aaa	—	0.20	—
bbb	—	0.20	—
ccc	—	0.10	—
ddd	—	0.20	—
N	—	44	—

1. CONTROLLING DIMENSION IN MILLIMETER UNLESS OTHERWISE SPECIFIED.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. "D1" AND "E1" ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM "b" DIMENSION BY MORE THAN 0.08 mm.
4. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm FOR 0.4 mm AND 0.5 mm PITCH PACKAGES.
5. SQUARE DOTTED LINE IS E-PAD OUTLINE.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

REVISION HISTORY

Revision D1 to E1

- Added green package OPN to [Ordering Information, on page 1](#).
- Added [Package Assembly, on page 10](#).
- Power Dissipation and Supply Currents updated to reflect product.
- In Electrical Ranges, on page 10, added differential dc loop voltage maximum of 85 V.
- In [DC Specifications, on page 13](#), No. 1, Standby and OHT modes A to B voltage increased from 53 to 54 V.
- In [DC Specifications, on page 13](#), No. 4, Leakage current for AD and BD leads modified.
- In DC Specifications, No. 11, VSAB Common Mode Rejection parameter added.
- In [DC Specifications, on page 13](#), No. 16, ILOOP/ILG min changed from 60000 to 30000.
- In [Test Switch Specifications, on page 15](#), changed ON-Resistance from 25 ohms Max to 30 ohms Max.
- In [Test Switch Specifications, on page 15](#), Max off-state leakage changed from 1 to 5 μ A.
- In [Transmission Specifications, on page 15](#), No. 1, max RSN impedance changed from 10 to 12 ohms.
- In [Transmission Specifications, on page 15](#), No. 8, 2-4 wire gain variation with frequency min -0.1 dB changed to -0.12 dB.
- In [Transmission Specifications, on page 15](#), No. 14, idle channel noise max changed from +11 to 13 dBnC and from -79 to -77 dBm.
- In [Transmission Specifications, on page 15](#), No. 15, longitudinal balance, active modes min changed from $f = 3400$ Hz, 53 dB to $f = 3000$ Hz, 56 dB, Typical values also changed. Standby mode longitudinal balance removed.
- In [Transmission Specifications, on page 15](#), No. 16, PSRR min for voice-band changed from 45 to 40 dB. PSRR 25 dB min for 3.4 to 50 kHz frequencies changed to 25 dB typ.
- In Transmission Specifications, No. 18, Metering Total Harmonic Distortion, $I_{\text{LOOP}} = 20$ mA added to conditions.
- In [Transmission Specifications, on page 15](#), No. 19, 1 kHz crosstalk changed to guaranteed by design.
- In Thermal Shutdown Fault Indications, R1 and TLD outputs changed from "outputs turned off" to "outputs operate normally".
- In Operating Mode Descriptions, Standby, Current limit increased to 36 mA.
- Line Card Parts List modified.
- VCP references added.
- In Thermal Shutdown Fault Indications, R1 and TLD outputs changed from "outputs turned off" to "outputs operate normally".
- In Operating Mode Descriptions, Standby, Current limit increased to 36 mA.
- Line Card Parts List modified.
- VCP references added.

Revision E1 to F1

- Added "Packing" column and Note 2 to [Ordering Information, on page 1](#).
- Power Dissipation, On-Hook Standby typical power increased from 38 mW to 45 mW, maximum power increased from 48 mW to 50 mW.
- Supply Currents, Standby State I_{VBH} current typical increased from 0.41 mA to 0.59 mA, maximum increased from 0.58 mA to 0.63 mA.
- Decoupling capacitors added to Application Circuit and Line Card Parts List.
- VHL Networks, IVD with metering resistor values changed to common values.
- Line Card Parts List, R_{SAi} , R_{SBi} resistors rating changed from 1/4 W to 3/4 W.
- In [Line card Parts List, on page 23](#), changed C_{VBF} from optional component to required component.
- Minor text edits.

Revision F1 to G1

- Chip Set Block Diagram on page 7 modified.
- Figure 3 Application Circuit on page 21 modified.
- Line Card Parts List on page 23 modified.
- Minor text and formatting edits.



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