Guaranteed Low Skew CMOS Clock Driver/Buffer

FEATURES/BENEFITS

- 10 CMOS outputs
- Monitor output
- Rail-to-rail output voltage swing
- 25Ω on-chip resistors available for low noise
- Input hysteresis for better noise margin
- Guaranteed low skew
  - 0.3ns same bank
  - 0.5ns opposite transition
  - 1.0ns different devices
- Industrial temperature range
- Available in QSOP (Q) and SOIC (SO)

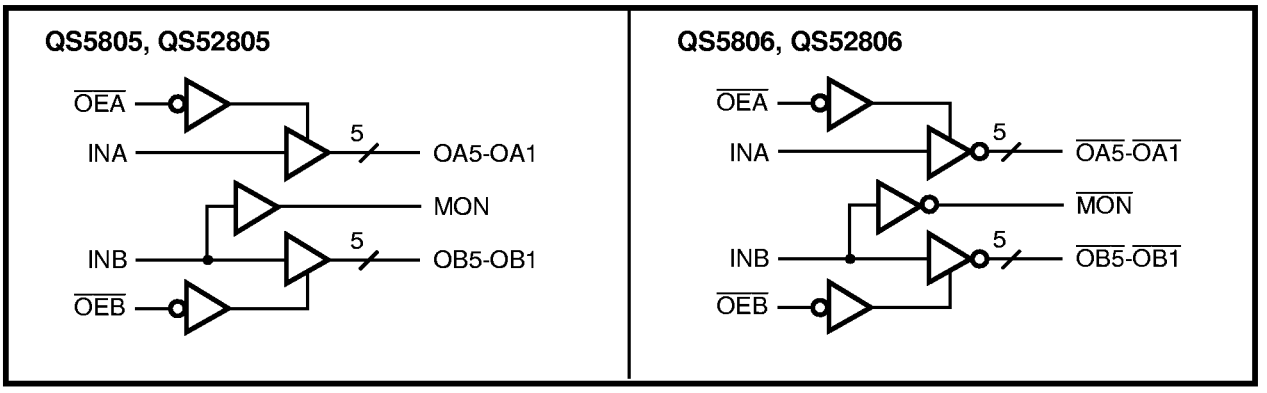
DESCRIPTION

The QS5805 and QS5806 clock driver/buffer circuits can be used for clock buffering schemes where low skew is a key parameter. The QS5805 offers two banks of five non-inverting outputs and the QS5806 provides inverting outputs. Designed in QSI's proprietary QCMOS process, these devices provide low propagation delay buffering with on-chip skew of 0.3ns for same-transition, same-bank signals. The QS52805 and QS52806 have on-chip series termination resistors for lower noise clock signals.

The QS52805 and QS52806 series resistor versions are recommended for driving unterminated lines with capacitive loading and other noise sensitive clock distribution circuits. These clock buffer products are designed for use in high-performance workstations, embedded and personal computing systems. Several devices can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks. Rail-to-rail output swing improves noise margin and allows easy interface with CMOS inputs.

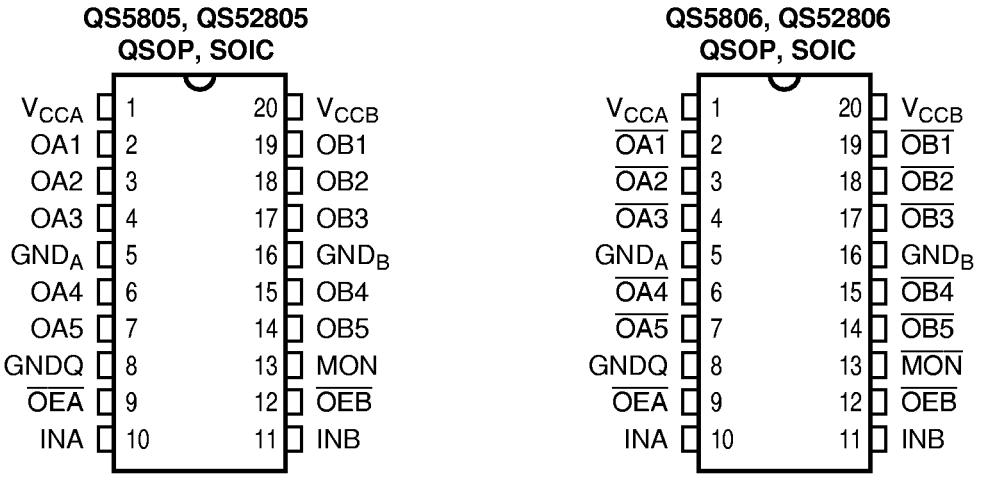
See Application Note AN-21A for more information on low-skew clock buffers.

Figure 1. Functional Block Diagram



Note: QS52805 and QS52806 devices have 25Ω series termination resistors on each clock output including monitor.

Figure 2. Pin Configurations (All Pins Top View)



2

Table 1. Pin Description

Name	I/O	Description
$\overline{OEA}$, $\overline{OEB}$	I	Output Enable Inputs
INA, INB	I	Clock Inputs
OAn, OBn, $\overline{OAn}$, $\overline{OBn}$	O	Clock Outputs
MON, $\overline{MON}$	O	Monitor Output (non-disable)

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to +7.0V
DC Output Voltage V_{OUT}	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation At T_A = 85°C, QSOP	0.82 watts
SOIC	0.75 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 3. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V

	QSOP		SOIC		
Pins	Typ	Max	Typ	Max	Unit
C_{IN}	4	6	4	6	pF
C_{OUT}	7	9	7	9	pF

Note: Capacitance is characterized but not tested.

Table 4. DC Electrical Characteristics Over Operating Range

Industrial: T_A = –40°C to 85°C, V_{CC} = 5.0V ± 10%, V_{HC} = V_{CC}-0.2V, V_{LC} = 0.2V

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for All Inputs	—	—	0.8	V
V_{IC}	Clamp Diode Voltage(3)	V_{CC} = Min., I_{IN} = –18mA	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage QS5805/5806	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OH} = –300µA	V_{HC}	V_{CC}	—	V
		I_{OH} = –15mA	3.6	4.3	—	
		I_{OH} = –24mA	2.4	3.8	—	
V_{OH}	Output HIGH Voltage QS52805/52806	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OH} = –12mA	3.6	4.3	—	V
		I_{OH} = –24mA	2.4	—	—	
V_{OL}	Output LOW Voltage QS5805/5806	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OL} = 300µA	—	GND	V_{LC}	V
		I_{OL} = 64mA	—	0.3	0.55	
V_{OL}	Output LOW Voltage QS52805/52806	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OL} = 12mA	—	—	0.50	V
$\lvert I_{IN} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = V_{CC}, V_{IN} = GND	—	—	1	µA
$\lvert I_{OZ} \rvert$	Output Leakage Current	V_{CC} = Max., V_{OUT} = V_{CC}, V_{OUT} = GND	—	—	1	µA
$\lvert I_{OFF} \rvert$	Input Power Off Leakage	V_{CC} = 0V, V_{IN} ≤ 4.5V	—	—	1	µA
I_{OS}	Short Circuit Current(2,3)	V_{CC} = Max., V_{OUT} = GND	–60	—	—	mA
ΔV_T	Input Hysteresis	V_{TLH} – V_{THL} for All Inputs	—	0.2	—	V
R_{OUT}	Output Resistance QS52805/52806	V_{CC} = Min., I_{OL} = 12mA	—	28	—	Ω

Notes:
1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be used to test this high power condition and the duration is ≤1 second.
3. Guaranteed by design but not tested.

Table 5. Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]		Typ[3]	Max	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		0.005	0.5	mA
ΔI_{CC}	Supply Current per Input HIGH	V_{CC} = Max., V_{IN} = 3.4V		1.0	2.5	mA
I_{CCD}	Dynamic Power Supply Current per Output[2]	V_{CC} = Max., $\overline{OEA}$ = $\overline{OEB}$ = GND Outputs enabled, 50% duty cycle		0.2	0.3	mA/ MHz
I_C	Total Power Supply Current Examples[2,4]	V_{CC} = Max., $\overline{OEA}$ = $\overline{OEB}$ = GND	V_{IN} = V_{CC} or V_{IN} = GND	10.0	15.5	mA
		50% duty cycle, f_I = 10MHz 5 outputs toggling Unused inputs = GND or Vcc	V_{IN} = 3.4V or V_{IN} = GND	10.5	16.8	
		V_{CC} = Max., $\overline{OEA}$ = $\overline{OEB}$ = GND	V_{IN} = V_{CC} or V_{IN} = GND	5.5	8.8	
		50% duty cycle, f_I = 2.5MHz All outputs toggling	V_{IN} = 3.4V or V_{IN} = GND	6.5	11.3	

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Guaranteed by design but not tested. C_L = 0pF
3. Typical values are for reference only. Conditions are V_{CC} = 5.0V and T_A = 25°C.
4. $I_C = I_{CC} + (\Delta I_{CC})(D_H)(N_T) + I_{CCD}(f_O)(N_O)$
   where:
   D_H = Input duty cycle
   N_T = Number of TTL HIGH inputs at D_H
   f_O = Output frequency
   N_O = Number of outputs at f_O

Table 6. Skew Characteristics Over Operating Range

Industrial: T_A = –40°C to 85°C, V_{CC} = 5.0V ± 10%
For QS5805, QS5806, C_{LOAD} = 50pF, R_{LOAD} = 500Ω.
For QS52805, QS52806, C_{LOAD} = 50pF (no resistor).

Symbol	Description[1]	—		A		B		C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{SK(O1)}$	Skew between all outputs same transition, same bank	—	0.5	—	0.35	—	0.3	—	0.3	ns
$t_{SK(O2)}$	Skew between outputs of all banks same transition,	—	0.7	—	0.5	—	0.4	—	0.4	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output (t_{PHL}-t_{PLH})	—	1.0	—	0.7	—	0.6	—	0.5	ns
$t_{SK(t)}$	Part to part skew[2]	—	1.5	—	1.0	—	1.0	—	1.0	ns

Notes:
1. Skew parameters are guaranteed across temperature range, but not production tested. Skew parameters are measured at 0.5V_{CC}. See Test Circuit and Waveforms.
2. $t_{SK(t)}$ only applies to devices of the same transition, same part type, same temperature, power supply voltage, loading, package and speed grade.

Table 7. Switching Characteristics Over Operating Range

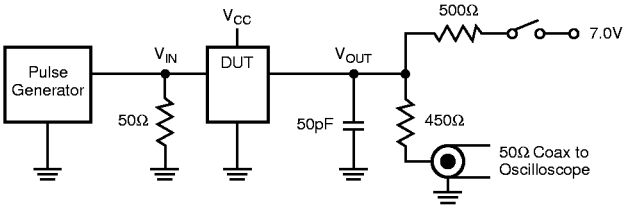
Industrial: T_A = –40°C to 85°C, V_{CC} = 5.0V ± 10%
For QS5805, QS5806, C_{LOAD} = 50pF, R_{LOAD} = 500Ω.
For QS52805, QS52806, C_{LOAD} = 50pF (no resistor).

Symbol	Description[1]	—		A		B		C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay[2] INA to OAn, INB to OBn	1.5	5.6	1.5	5.3	1.5	5.0	1.5	4.5	ns
t_{PZL} t_{PZH}	Output Enable Time	1.5	8.0	1.5	8.0	1.5	7.0	1.5	7.0	ns
t_{PLZ} t_{PZH}	Output Disable Time[3]	1.5	7.0	1.5	7.0	1.5	6.0	1.5	6.0	ns
t_R,t_F	Output Rise/Fall Time[3] 0.8V-2.0V	—	1.5	—	1.5	—	1.5	—	1.5	ns
	0.2V_{CC}-0.8V_{CC}	—	3.0	—	3.0	—	3.0	—	3.0	ns

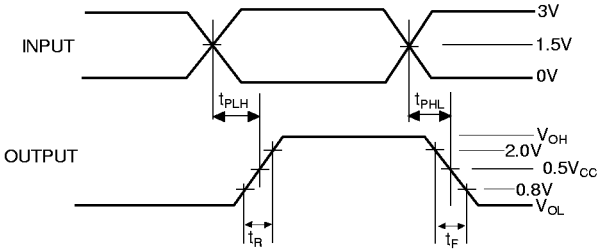
Notes:
1. See Test Circuit and Waveforms. Minimums guaranteed but not tested. Timing parameters are measured at 0.5V_{CC}.
2. The propagation delay range indicated by Min. and Max. specifications results from process and environmental variables. These propagation delay limits do not imply skew.
3. Guaranteed by design but not tested.

Figure 3. Test Circuits and Waveforms

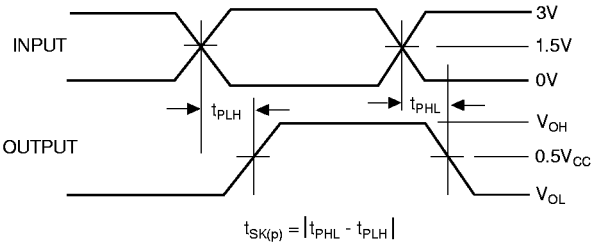
Parameter Tested	Switch Position
t_{PLZ}, t_{PZL}	Closed
All Others	Open



Pulse generator for all pulses: $f \leq 1.0MHz$; $t_F \leq 2.5ns$; $t_R \leq 2.5ns$

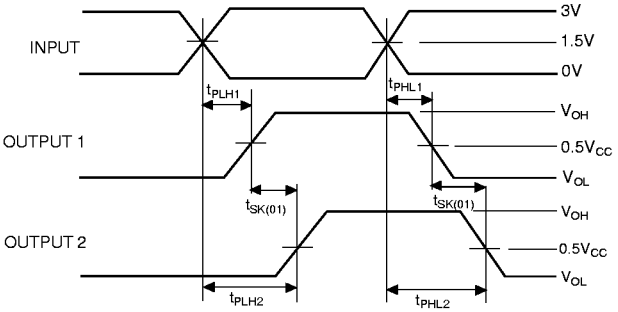


Propagation Delay



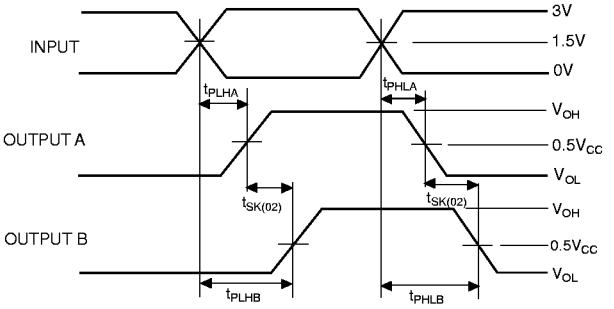
$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

Pulse Skew - $t_{SK(p)}$



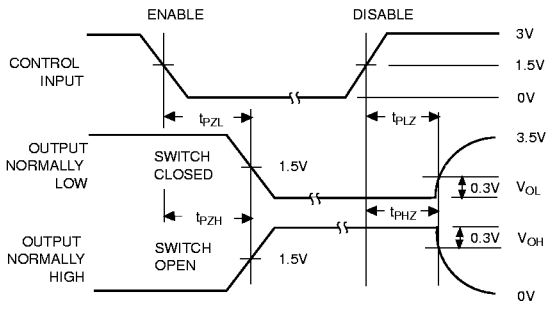
$t_{SK(O1)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Output Skew (Same Bank) - $t_{SK(O1)}$

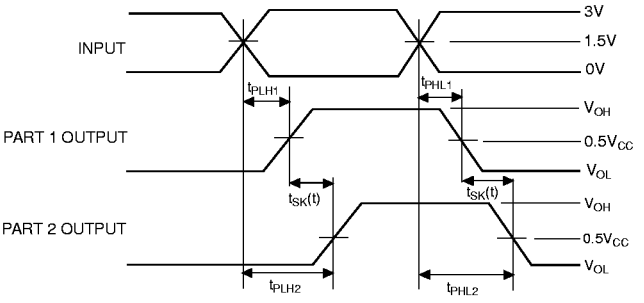


$t_{SK(O2)} = |t_{PLHB} - t_{PLHA}|$ or $|t_{PHLB} - t_{PHLA}|$

Ouput Skew (Different Banks) - $t_{SK(O2)}$



Enable and Disable Times



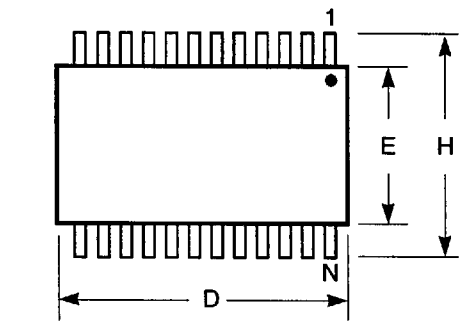
$t_{SK(t)} = |t_{PLH}2 - t_{PLH}1|$ or $|t_{PH}L2 - t_{PHL}1|$

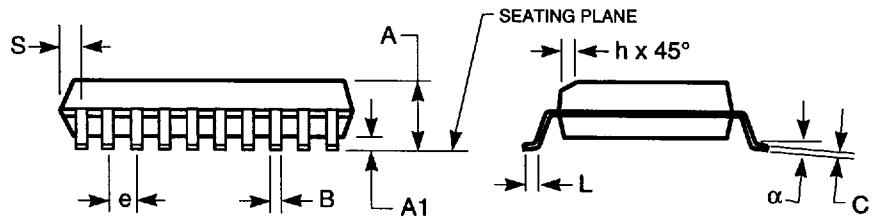
Part-to-Part Skew - $t_{SK(t)}$

150-MIL QSOP - Package Code Q

Quarter-Size Outline Package
Plastic Small Outline Gull-Wing

Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.



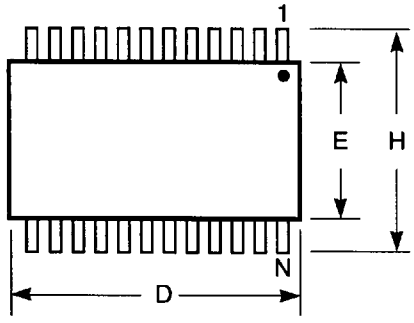


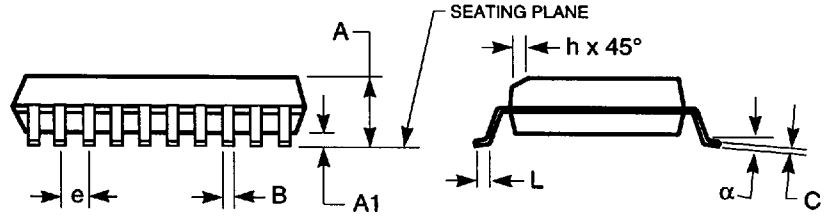
JEDEC#	MO-137AB			MO-137AD			MO-137AE			MO-137AF		
DWG#	PSS-16A			PSS-20A			PSS-24A			PSS-28A		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
B	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010
D	0.189	0.193	0.197	0.337	0.341	0.344	0.337	0.341	0.344	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157
e	0.025 BSC			0.025 BSC			0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035
N	16			20			24			28		
α	0°	5°	8°	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.006	0.009	0.010	0.056	0.058	0.060	0.031	0.033	0.035	0.031	0.033	0.035

300-MIL SOIC - Package Code SO

Plastic Small Outline Gull-Wing

Notes:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.





JEDEC#	MS-013AA		MS-013AC		MS-013AD		MS-013AE	
DWG#	PS16A		PS20A		PS24A		PS28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.096	0.104
A1	0.005	0.011	0.005	0.011	0.005	0.011	0.005	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.402	0.412	0.500	0.510	0.602	0.612	0.701	0.711
E	0.292	0.299	0.292	0.299	0.292	0.299	0.292	0.299
e	0.044	0.056	0.044	0.056	0.044	0.056	0.044	0.056
H	0.396	0.416	0.396	0.416	0.396	0.416	0.396	0.416
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
N	16		20		24		28	
α	0°	8°	0°	8°	0°	8°	0°	8°