极景微半导体

LVPECL Output Ultra-Low Additive Jitter/Differential Clock Buffer

US5D8905/8907/8925

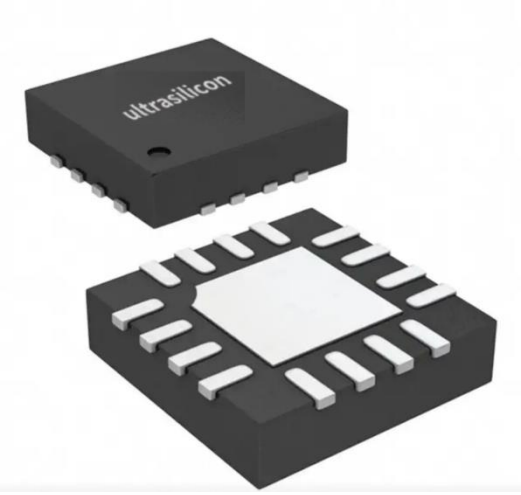
Datasheet

Description

The US5D8905(one input, one output), US5D8907(dual one input, one output),and US5D8925(one input, two outputs) are 2-GHz,differential high-performance clock fanout buffer.

The US5D8905/US5D8907/US5D8925 are highly versatile, low additive jitter buffer that can generate LVPECL clock outputs from LVPECL,and LVDS, or LVCMOS inputs for a variety of communication applications. It has a maximum clock frequency up to 2-GHz.

The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.



Features

- 1:1 Differential Buffer(US5D8905)
- Dual1:1 Differential Buffer(US5D8907)
- 1:2 Differential Buffer(US5D8925)
- Universal Input Accept LVPECL,LVDS and LVCMOS/LVTTL
- LVPECL output
- Maximum Output Frequency LVPECL - 2-GHz
- Maximum Propagation Delay:500 ps(typical)
- Output skew: 20 ps (typical)
- Part-to-part skew< 300ps
- Additive RMS phase jitter @ 156.25MHz: 38fs RMS (12kHz - 20MHz), typical @ 3.3V/ 3.3V
- Supply voltage : VDD= 3.3V or 2.5V
- Industrial Temperature Range:-40°C to 85°C
- Available in QFN-16 package

Applications

- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Elthernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH,CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express(PCIe 3.0,4.0,5.0)
- Remote Radio Units and Baseband Units

Block Diagram

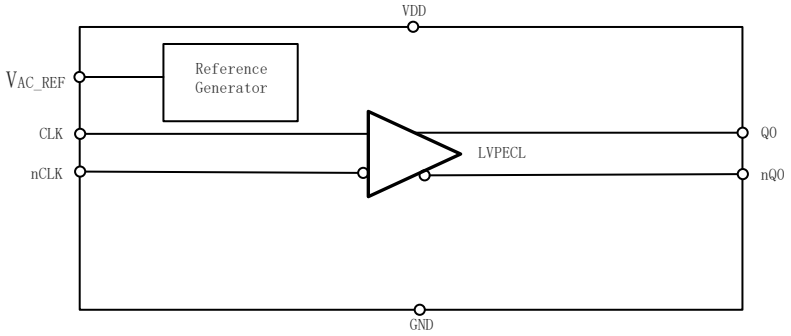


Figure1. US5D8905

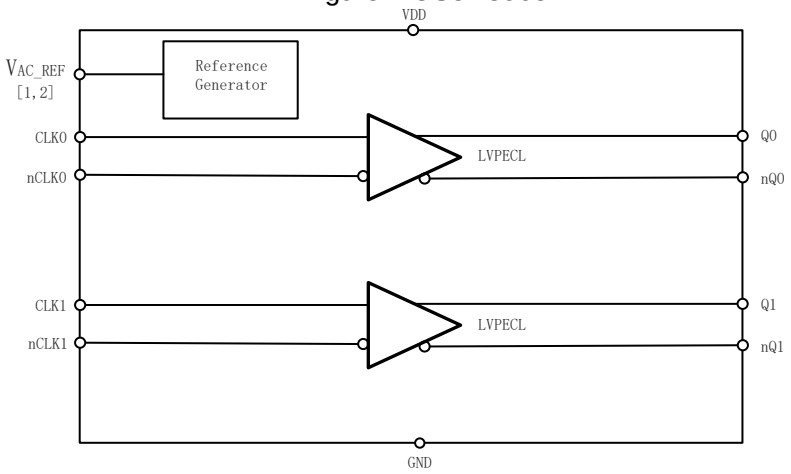


Figure2. US5D8907

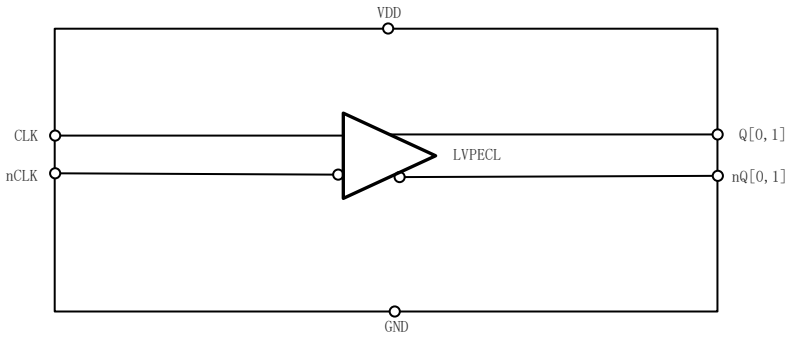
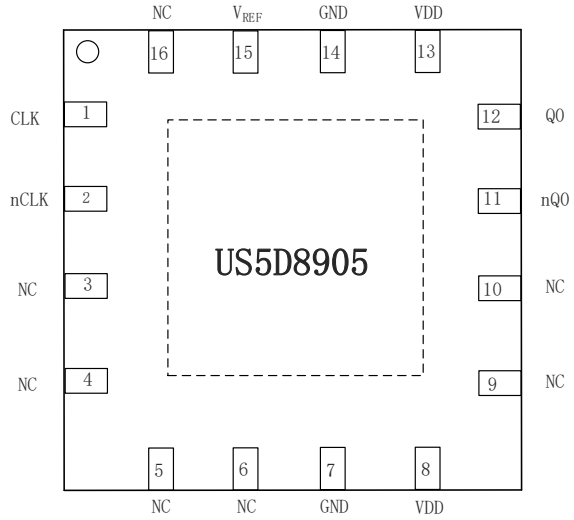
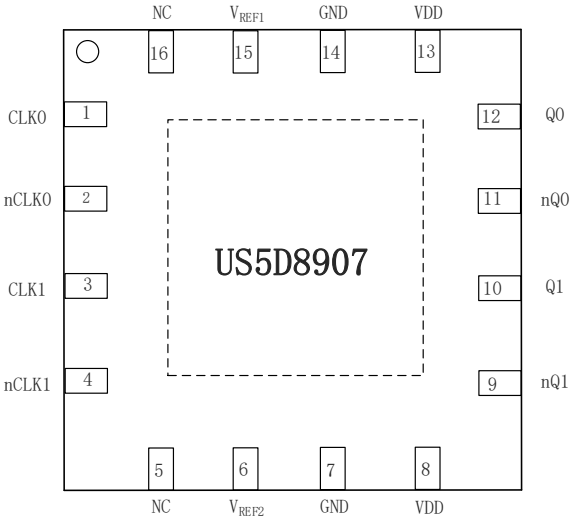
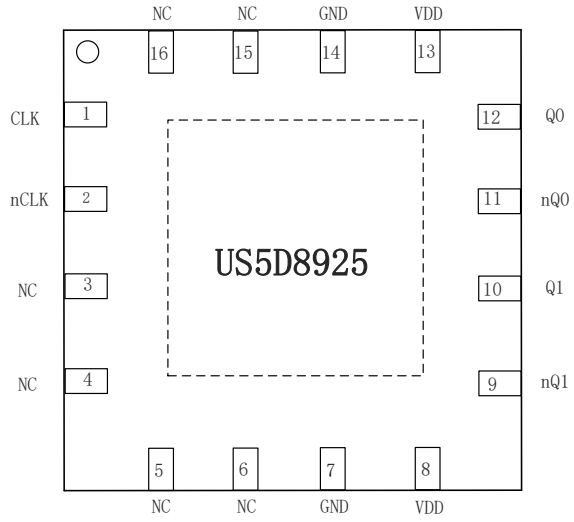


Figure3. US5D8925

Pin Assignment for QFN-16 Package







Pin Description and Pin Characteristic Tables

Table 1: US5D8905 Pin Descriptions

Number	Name	Type	Description
1	CLK	Input	Differential input pair or single-ended input. Unused input pair can be left floating.
2	nCLK	Input	Differential input pair.
3	NC	NC	Not connect.
4	NC	NC	Not connect.
5	NC	NC	Not connect.
6	NC	NC	Not connect.
7	GND	Power	Ground.
8	VDD	Power	Power supply voltage.
9	NC	NC	Not connect.
10	NC	NC	Not connect.
11	nQ0	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating.
12	Q0	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating.
13	VDD	Power	Power supply voltage.
14	GND	Power	Ground.
15	V_{REF}	Output	Reference Voltage.Reference voltage for biasing ac-coupled inputs.
16	NC	NC	Not connect.

Table 2: US5D8907 Pin Descriptions

Number	Name	Type	Description
1	CLK0	Input	Differential input pair or single-ended input. Unused input pair can be left floating.
2	nCLK0	Input	Differential input pair.
3	CLK1	Input	Differential input pair or single-ended input. Unused input pair can be left floating.
4	nCLK1	Input	Differential input pair.
5	NC	NC	Not connect.
6	V_{REF2}	Output	Reference Voltage 2.Reference voltage for biasing ac-coupled inputs.
7	GND	Power	Ground.
8	VDD	Power	Power supply voltage.
9	nQ0	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating.
10	Q0	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating.
11	nQ1	Output	Differential LVPECL output pair no. 1. Unused output pair can be left floating.
12	Q1	Output	Differential LVPECL output pair no. 1. Unused output pair can be left floating.
13	VDD	Power	Power supply voltage.
14	GND	Power	Ground.
15	V_{REF1}	Output	Reference Voltage 1.Reference voltage for biasing ac-coupled inputs.
16	NC	NC	Not connect.

Table 3: US5D8925 Pin Descriptions

Number	Name	Type	Description
1	CLK	Input	Differential input pair or single-ended input. Unused input pair can be left floating.
2	nCLK	Input	Differential input pair.
3	NC	NC	Not connect.
4	NC	NC	Not connect.
5	NC	NC	Not connect.
6	NC	NC	Not connect.
7	GND	Power	Ground.
8	VDD	Power	Power supply voltage.
9	nQ1	Output	Differential LVPECL output pair no. 1. Unused output pair can be left floating.
10	Q1	Output	Differential LVPECL output pair no. 1. Unused output pair can be left floating.
11	nQ0	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating.
12	Q0	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating.
13	VDD	Power	Power supply voltage.
14	GND	Power	Ground.
15	NC	NC	Not connect.
16	NC	NC	Not connect.

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD}	4.6V
V_{IN}	-0.5V to V_{DD} + 0.5V
T_J :Junction Temperature	125°C
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5% 2.5-5%	3.3 2.5	3.3+5% 2.5+5%	V

Electrical Characteristics(INPUT)

At VCC = 2.375 V to 3.6 V and TA = －40° C to +85° C and TPCB ≤ 105° C (unless otherwise noted).

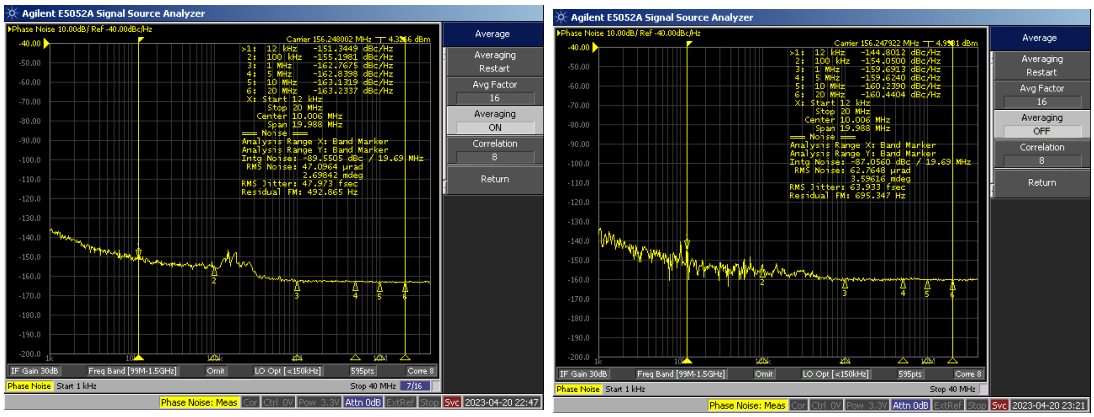
Parameter		Test Conditions	Min	Typ	Max	Unit
DC input characteristics						
F_{IN}	Input Frequency	VDD=3.3V	0.1		2000	MHz
V_{IH}	Input high voltage		1.6		VDD	V
V_{IL}	Input low voltage		GND		VDD-0.7	V
V_{ID}	Input differential range	-40° C to +85° C(±1.7V between input pins)	0.2		3.4	Vpp
C_{IN}	Input capacitance			0.4		pF

Electrical Characteristics(OUTPUT)

VDD = 3.125 V to 3.6 V; TA = －40° C to +85° C and TPCB ≤ 105° C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
LVPECL Output						
V_{OH}	Output high voltage		VDD-1.2		VDD-0.9	V
V_{OL}	Output low voltage		VDD-1.7		VDD-1.3	V
V_{OD}	Differential output voltage swing	F_{IN} ≤ 2 GHz	0.61		1040	mV
V_{REF}	Reference voltage		VDD-1.6		VDD-1.1	V
t_{PD}	Propagation delay			0.5	2	ns
$t_{SK,PP}$	Part-to-part skew				300	ps
$t_{SK,O}$	Output skew			20	50	ps
t_{RJIT}		Additive RMS phase jitter @ 156.25MHz: (12kHz - 20MHz)		TBD		fs
t_R/t_F	Output rise/fall time	20% to 80%		120	500	ps
I_{DD}	Operating current	VDD=3.3V, all outputs active(US5D905)		TBD		mA
		VDD=3.3V, all outputs active(US5D907)		TBD		
		VDD=3.3V, all outputs active(US5D925)		82		

PHASE JITTER



(a)Jitter_Source **(b)3V3_156M25_LVPECL**

Figure 4 .RMS_Jitter_3V3=Sqrt(64^2-48^2)=38fs

The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

Timing Diagrams

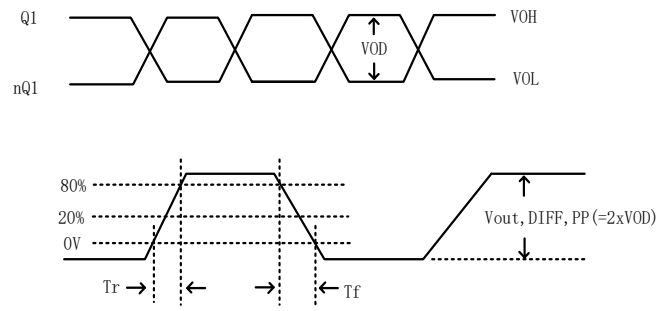
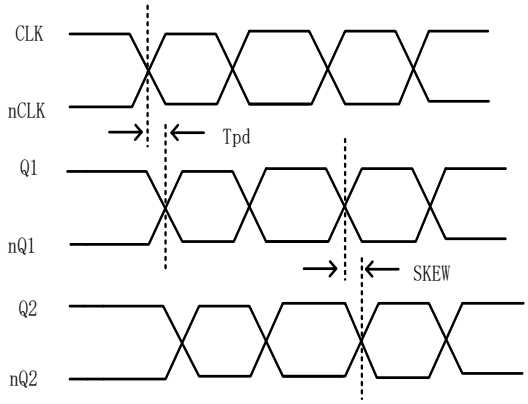


Figure 5.output voltage and rise/fall time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn(n = 0, 1, 2....7), or as the difference between the fastest and the slowest tPHLn (n = 0, 1, 2....7).
(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2....7) across multiple devices, or the difference between the fastest and the slowest tPHLn (n = 0, 1,2....7) across multiple devices

Figure 6.output and skew

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

For the single-ended input LVCMOS signal, Rs and R0 in the driver form a 50Ω impedance match, and the direct-isolated capacitor C3 avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to VDD/2.

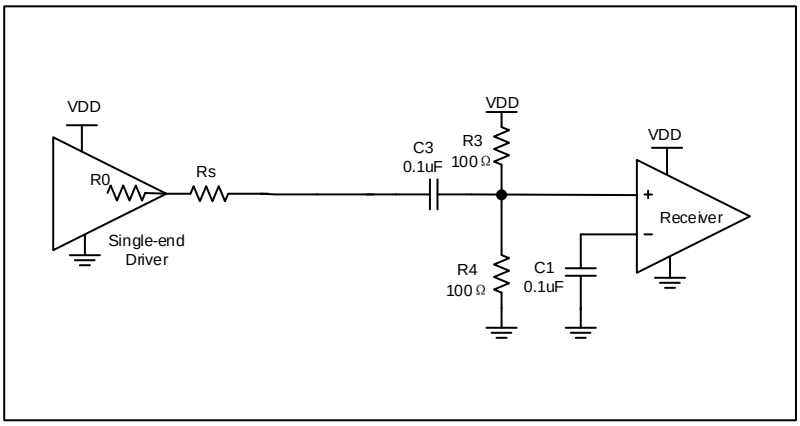
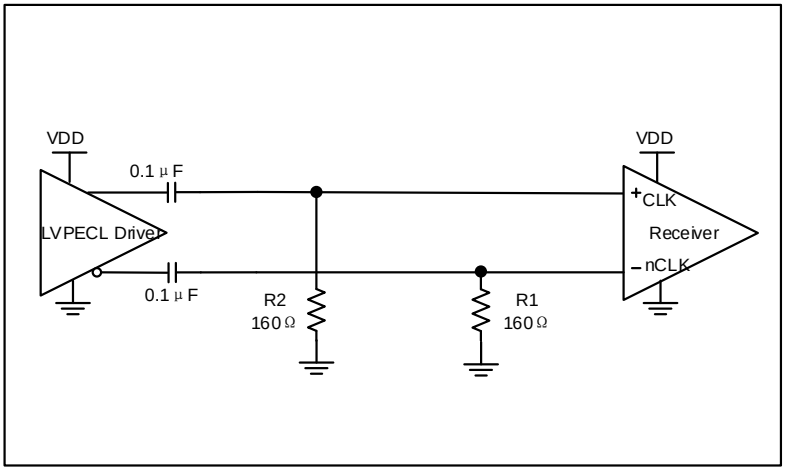
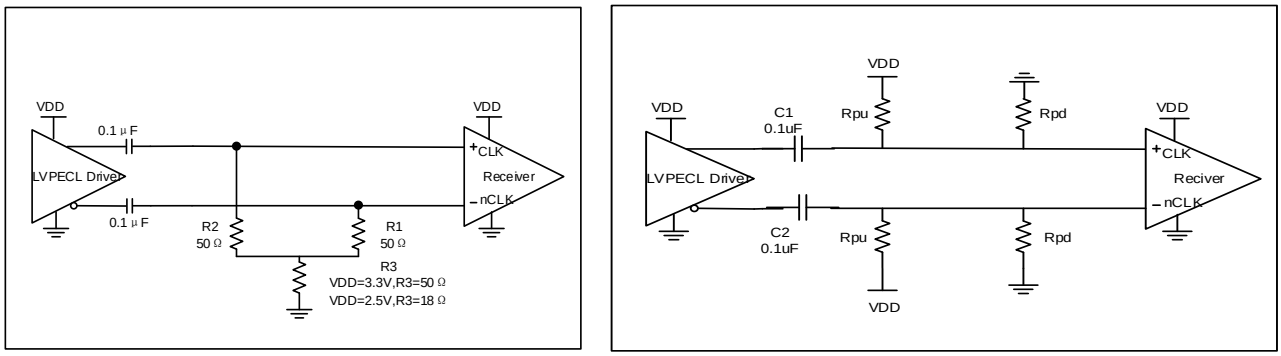


Figure7.Single-termination method of differential input

Input connection circuit

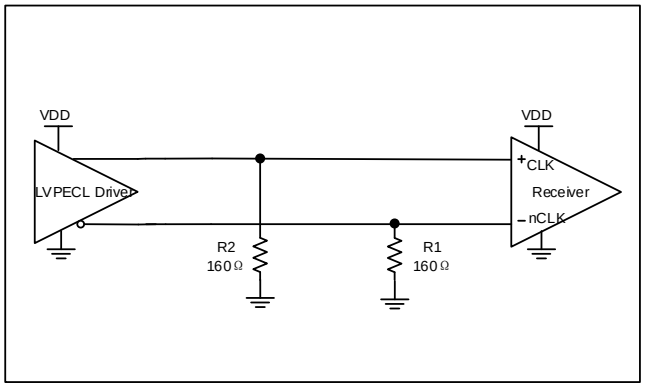
The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the VPP and VCMR input requirements. Figure8 to Figure12 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

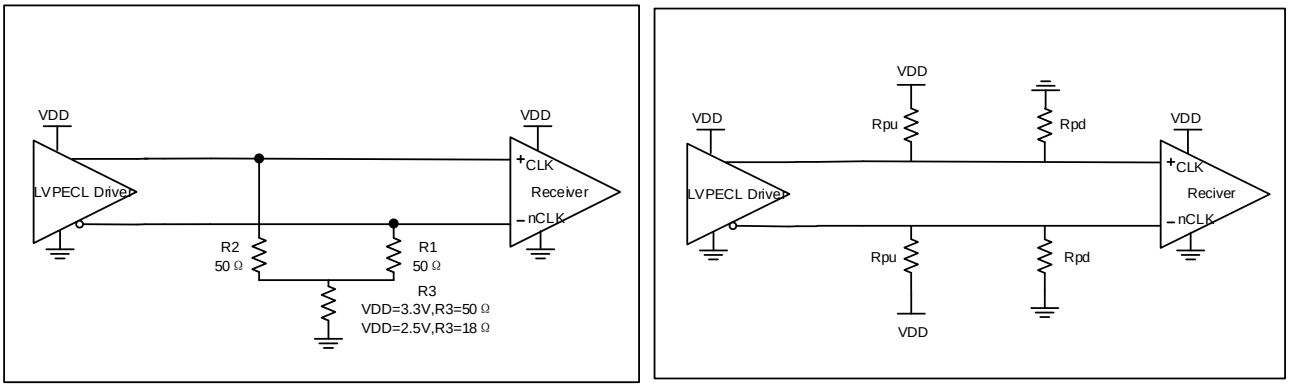




VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

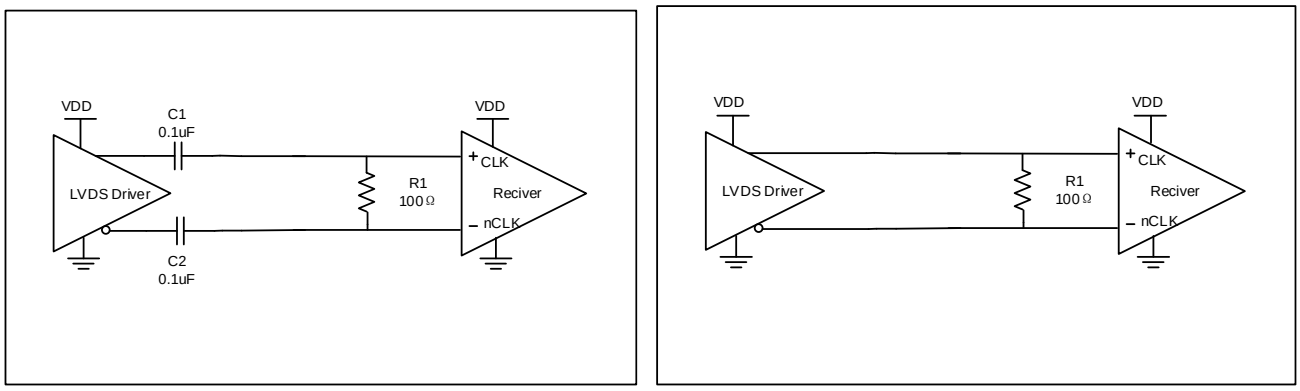
Figure8.LVPECL Driver(AC)





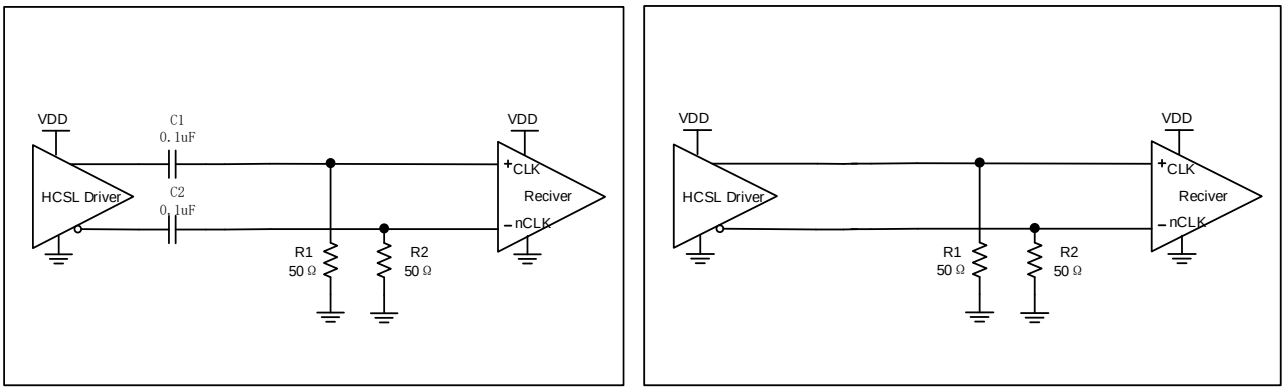
VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

Figure9.LVPECL Driver(DC)



a)AC coupling **b)DC coupling**

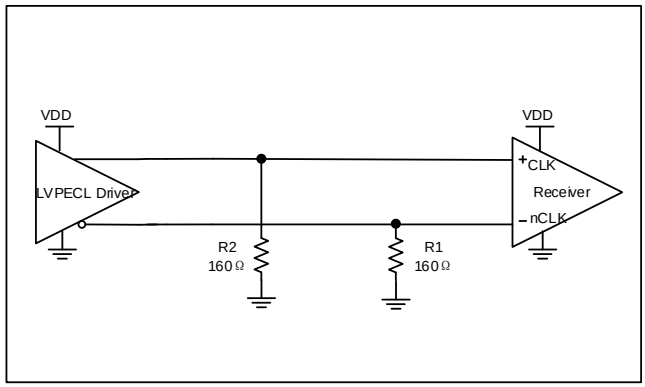
Figure10.LVDS Driver

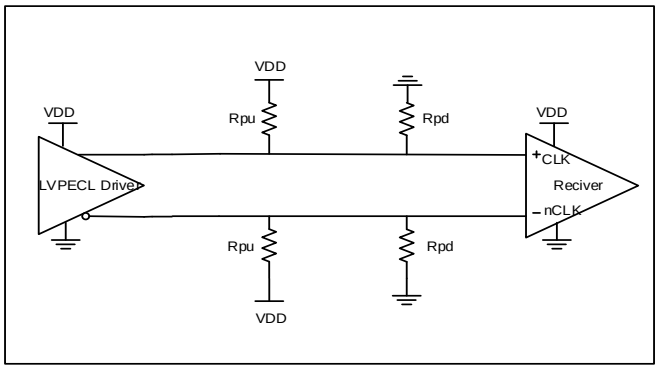


a)AC coupling **b)DC coupling**

Figure11.HCSL Driver

Output connection circuit





VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

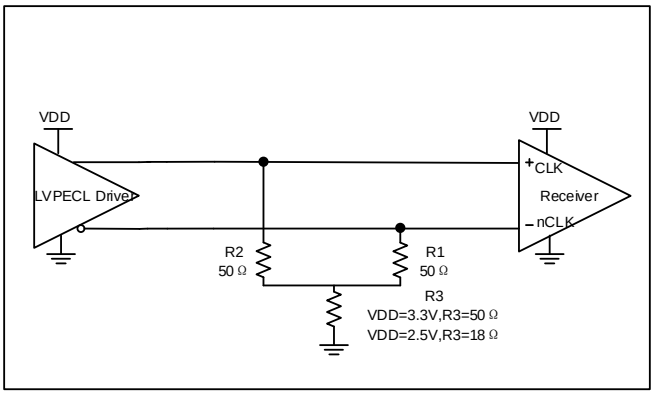
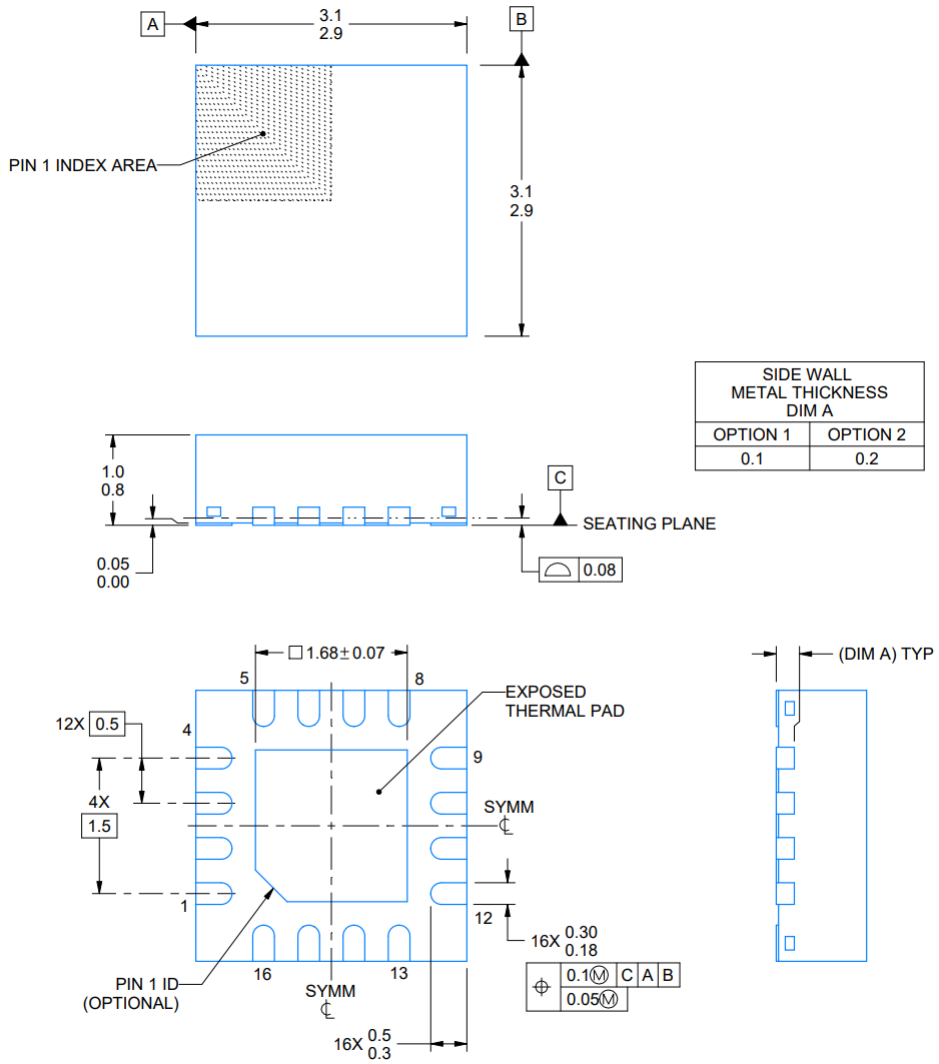


Figure12.LVPECL Driver

PACKAGE DIMENSIONS(QFN-16)



Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
A	0.80	0.90	1.00	K	0.20	-	-
A1	0.00	0.02	0.05	L	0.20	0.30	0.40
A3	-	0.20Ref	-	aaa	0.05		
b	0.20	0.25	0.30	bbb	0.10		
D	3.00BSC			ccc	0.10		
E	3.00BSC			ddd	0.05		
e	0.50BSC			eee	0.08		
D2	1.60	1.70	1.80				
E2	1.60	1.70	1.80				

Reflow profile

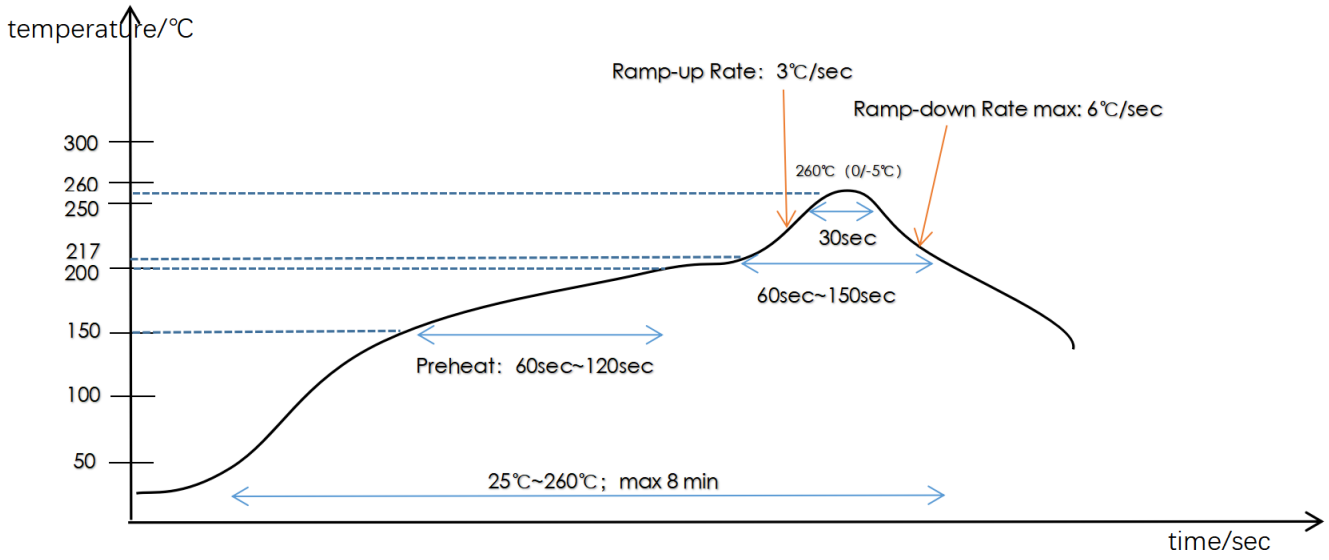


Figure13: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2023.09.22	First Draft.	1.0