

# CD4518 Dual BCD Up-Counter

# CD4520 Dual Binary Up-Counter

## 1. General Description

### 1.1 Description

CD4518 Dual BCD Up Counter and CD4520 Dual Binary Up Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable CLOCK and ENABLE lines for incrementing on either the positive-going or negative-going transition. For single unit operation the ENABLE input is maintained high and the counter advances on each positive-going transition of the CLOCK. The counters are cleared by high levels on their RESET lines. The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the CLOCK input of the latter is held low.

### 1.2 Features

- Positive or negative edge triggering
- Synchronous internal carry propagation
- 100% tested for quiescent current at 18V
- Maximum input current of 1 $\mu$ A at 18V (temperature : +25°C)
- Standardized symmetrical output characteristics

### 1.3 Device Information

| PART NUMBER | PACKAGE |
|-------------|---------|
| CD4518      | DIP     |
| CD4520      | SOP     |
|             | TSSOP   |

## 2. Pin Description and Functional Diagram

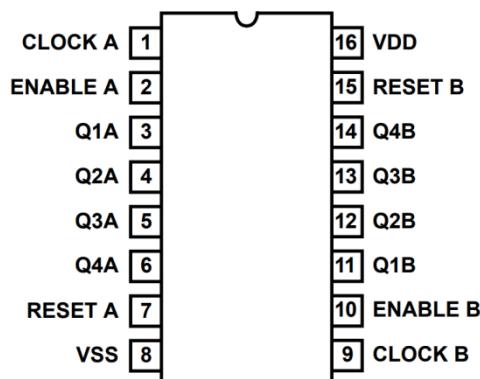
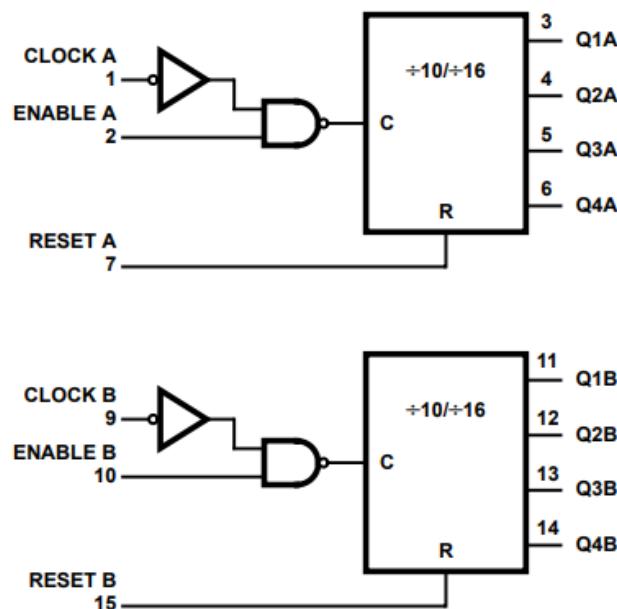


Figure 2.1 Top View



V<sub>SS</sub> = 8  
V<sub>DD</sub> = 16

Figure 2.2 Functional Diagram

### 3. System Diagram

#### 3.1 Logic Diagram

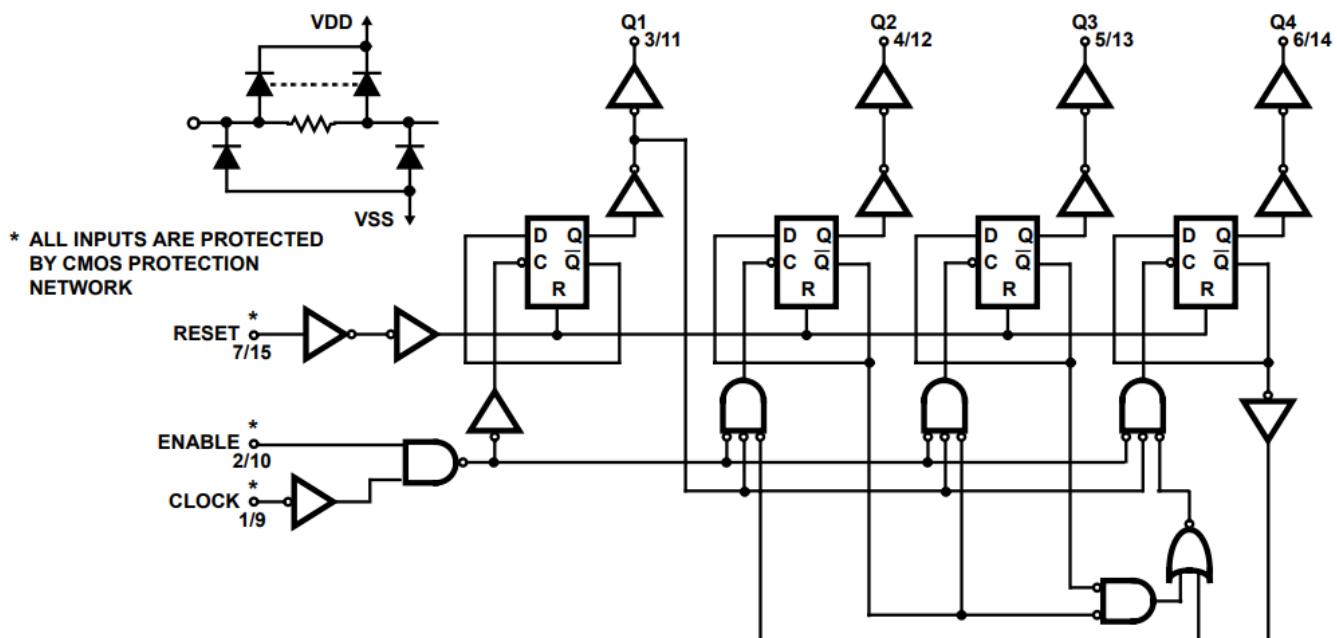


Figure 3.1: CD4518 Logic Diagram for one or two identical counters

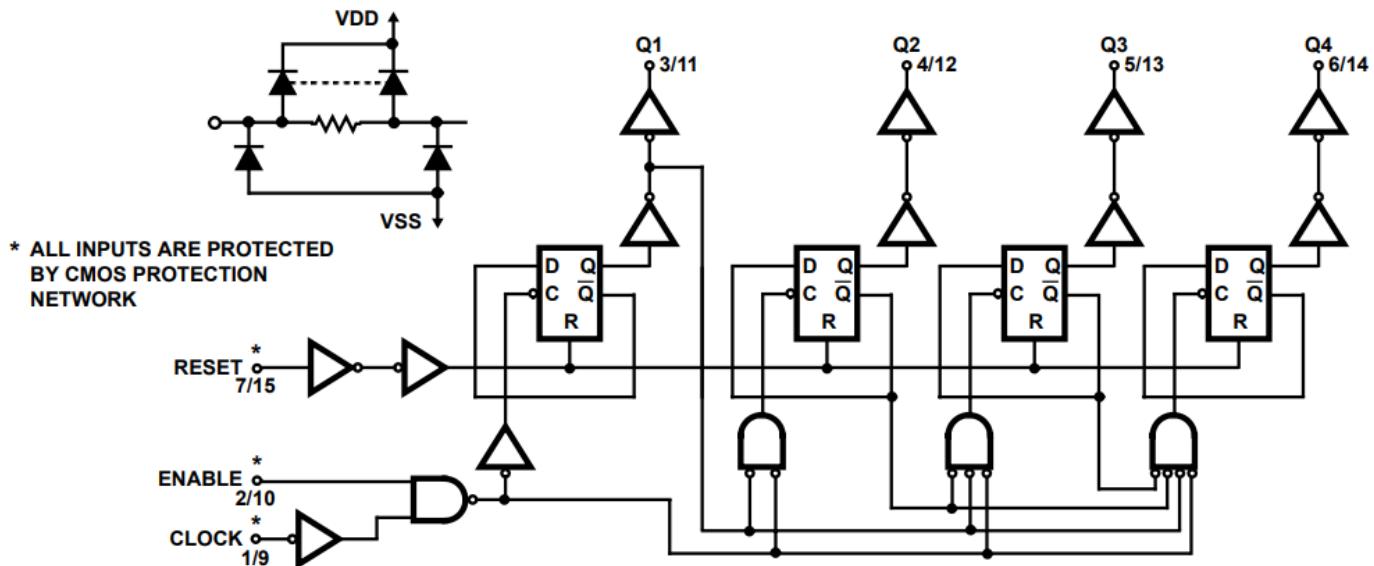


Figure 3.2: CD4520 Logic Diagram for one or two identical counters

### 3.2 Truth Table

| Clock | Enable | Reset | Action            |
|-------|--------|-------|-------------------|
| ↑     | 1      | 0     | Increment Counter |
| 0     | ↓      | 0     | Increment Counter |
| ↓     | X      | 0     | No Change         |
| X     | ↑      | 0     | No Change         |
| ↑     | 0      | 0     | No Change         |
| 1     | ↓      | 0     | No Change         |
| X     | X      | 1     | Q1 thru Q4 = 0    |

X = Don't Care, 1 ≡ High State, 0 ≡ Low State, ↑=positive-going transition, ↓=negative-going transition.

## 4. Specifications

### 4.1 Absolute Maximum Ratings

| Symbol | Parameter  | MIN  | MAX     | Unit |
|--------|--|------|---------|------|
| VDD    | DC Supply Voltage Range<br>(Voltage Referenced to VSS Terminals) | -0.5 | 20      | V    |
| VI     | Input Voltage Range, All Inputs                                  | 0.5  | VDD+0.5 | V    |
| PD     | Power Dissipation  |      | 500     | mW   |
| TJ     | Junction Temperature   |      | 125     | °C   |
| TOP    | Operating Temperature  | 0    | 70      | °C   |

Absolute maximum ratings are those values beyond which the device could be permanently damaged. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions.



## 4.2 Electrical Characteristics

( $T_a=25^\circ\text{C}$ , voltages are referenced to VSS (ground=0V), unless otherwise specified)

| Symbol          | Parameter                 | Test Condition |      |     | MIN   | TYP  | MAX  | Unit |
|-----------------|---------------------------|----------------|------|-----|-------|------|------|------|
|                 |                           | VO             | VIN  | VDD |       |      |      |      |
| I <sub>DD</sub> | Supply Current            |                | 0,5  | 5   | --    |      | 1    | uA   |
|                 |                           |                | 0,10 | 10  | --    |      | 1    | uA   |
|                 |                           |                | 0,18 | 18  | --    |      | 1    | uA   |
| I <sub>OL</sub> | Low Level Output Current  | 0.4            | 0,5  | 5   | 1.5   | 2.5  | --   | mA   |
|                 |                           | 0.5            | 0,10 | 10  | 3     | 6    | --   | mA   |
|                 |                           | 1.5            | 0,15 | 15  | 13    | 24   | --   | mA   |
| I <sub>OH</sub> | High Level Output Current | 4.6            | 0,5  | 5   | -0.5  | -1.3 | --   | mA   |
|                 |                           | 2.5            | 0,5  | 5   | -3    | -5.5 | --   | mA   |
|                 |                           | 9.5            | 0,10 | 10  | -1.5  | -3   | --   | mA   |
|                 |                           | 13.5           | 0,15 | 15  | -5    | -10  | --   | mA   |
| V <sub>OL</sub> | Low Level Output Voltage  |                | 0,5  | 5   | --    | 0.0  | 0.05 | V    |
|                 |                           |                | 0,10 | 10  | --    | 0.0  | 0.05 | V    |
|                 |                           |                | 0,15 | 15  | --    | 0.0  | 0.05 | V    |
| V <sub>OH</sub> | High Level Output Voltage |                | 0,5  | 5   | 4.95  | 5    | --   | V    |
|                 |                           |                | 0,10 | 10  | 9.95  | 10   | --   | V    |
|                 |                           |                | 0,15 | 15  | 14.95 | 15   | --   | V    |
| V <sub>IL</sub> | Low Level Input Voltage   | 0.5,4.5        |      | 5   | --    |      | 1.5  | V    |
|                 |                           | 1,9            |      | 10  | --    |      | 3    | V    |
|                 |                           | 1.5,13.5       |      | 15  | --    |      | 4    | V    |
| V <sub>IH</sub> | High Level Input Voltage  | 0.5,4.5        |      | 5   | 3.5   |      | --   | V    |
|                 |                           | 1,9            |      | 10  | 7     |      | --   | V    |
|                 |                           | 1.5,13.5       |      | 15  | 11    |      | --   | V    |
| I <sub>IN</sub> | Input Leakage Current     |                | 0,18 | 18  |       |      | ±1   | uA   |

## 5. Timing Diagrams

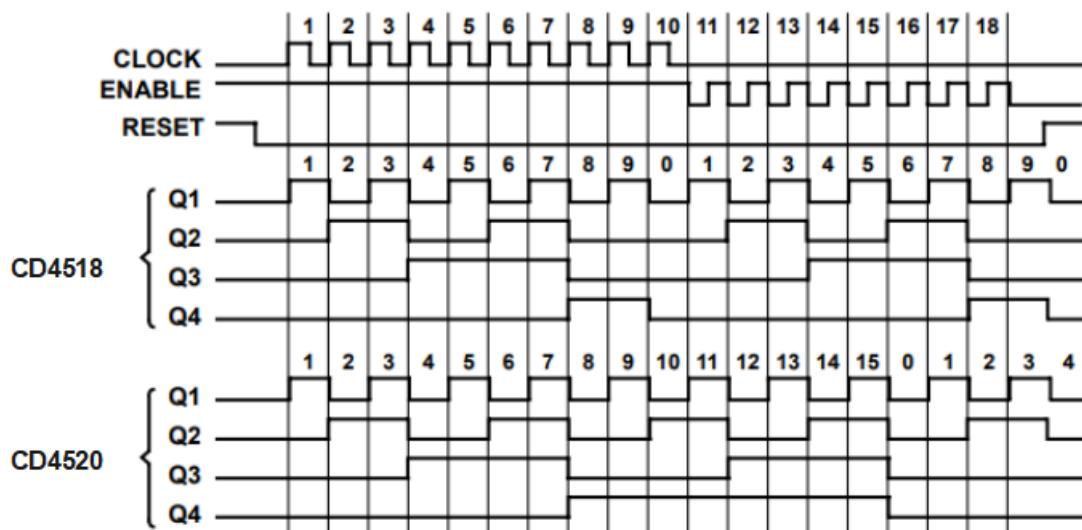


Figure 6.1: Timing diagrams for CD4518 and CD4520

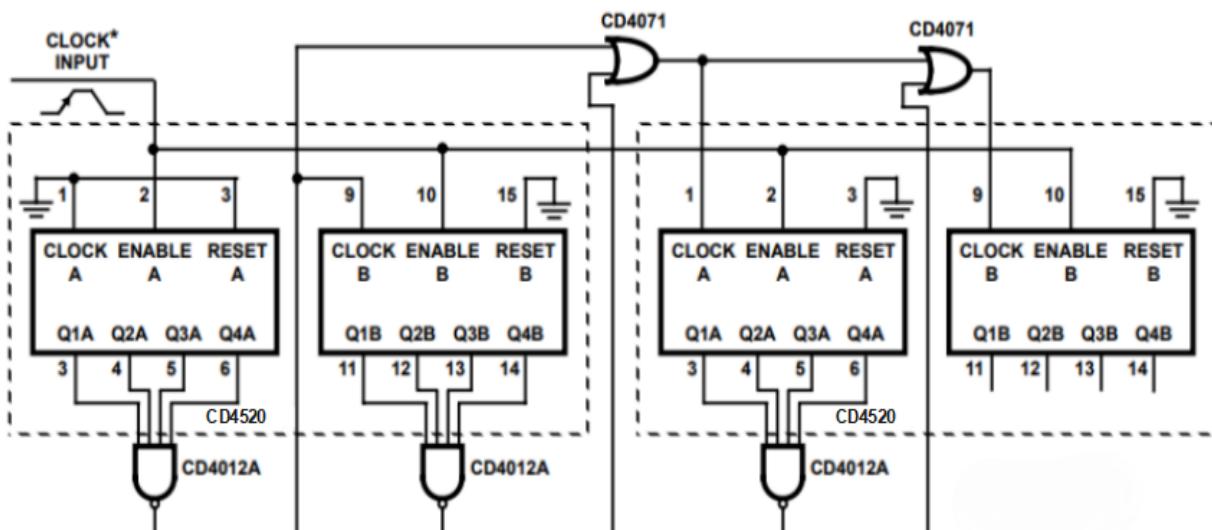


Figure 6.2: Ripple cascading of four counters with positive edge triggering

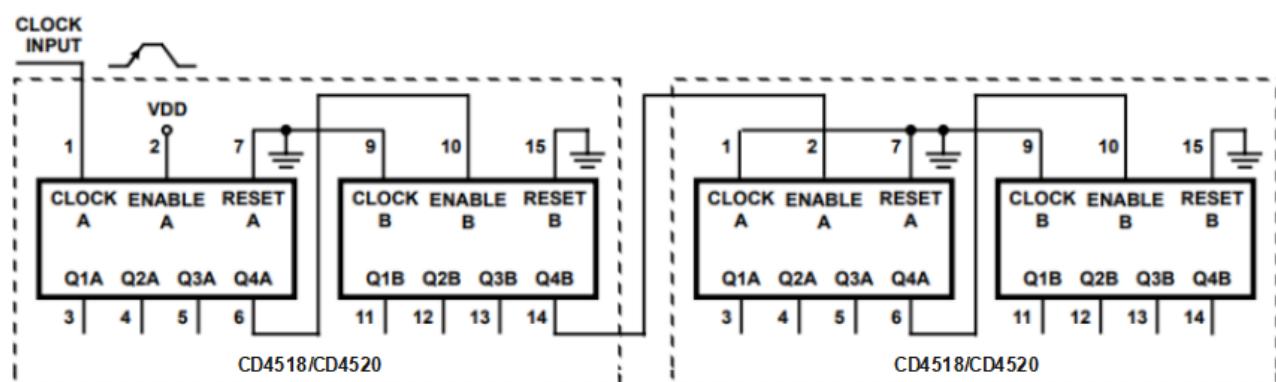


Figure 6.2: Synchronous cascading of four counters with negative edge triggering

\*For synchronous cascading, the clock transition time should be made less than or equal to the sum of the fixed propagation delay at 15pF and the transition time of the output driver stage for the estimated capacitive load.



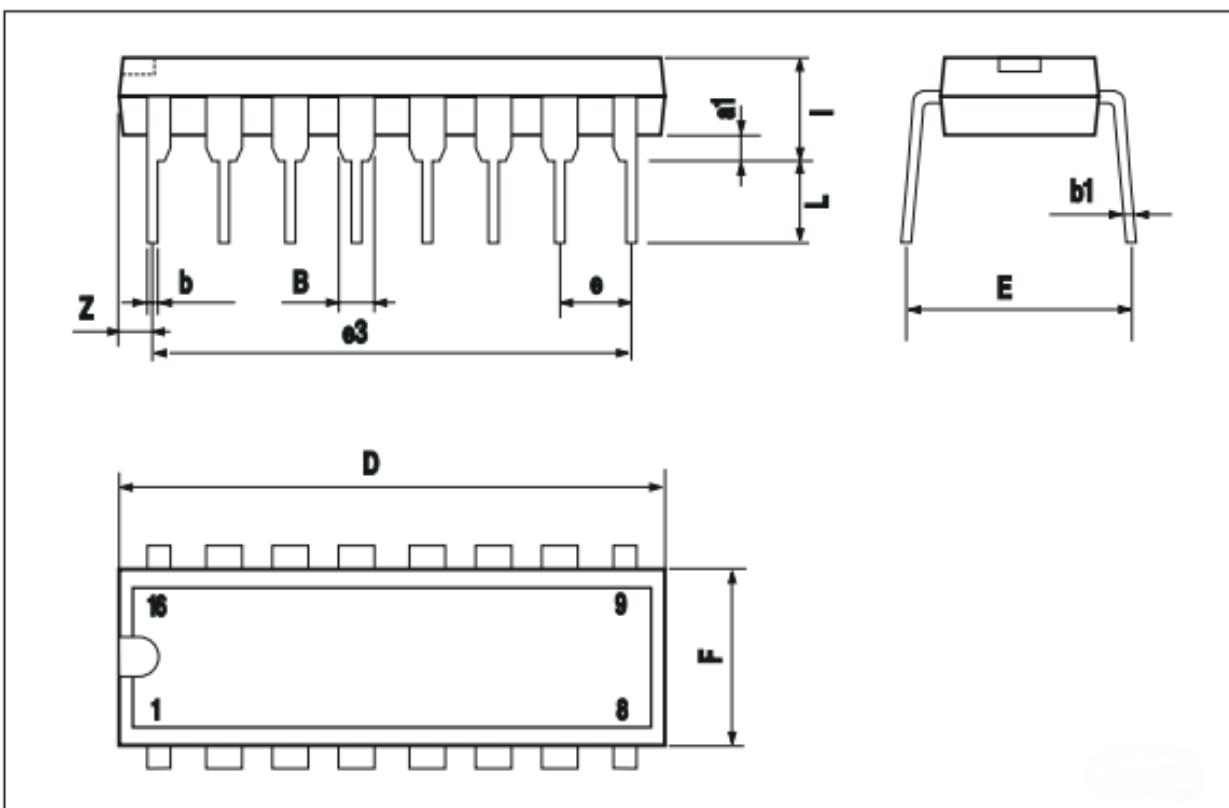
## 6. Ordering Information

| Orderable Device | Package Type | Pins | Packing     | Package Qty |
|------------------|--------------|------|-------------|-------------|
| CD4518ND16ATBE   | DIP          | 16   | Tube        | 25          |
| CD4518NS16ARDQ   | SOP          | 16   | Tape & Reel | 4000        |
| CD4518TS16ARDQ   | TSSOP        | 16   | Tape & Reel | 4000        |
| CD4520ND16ATBE   | DIP          | 16   | Tube        | 25          |
| CD4520NS16ARDQ   | SOP          | 16   | Tape & Reel | 4000        |
| CD4520TS16ARDQ   | TSSOP        | 16   | Tape & Reel | 4000        |

## 7. Package Information

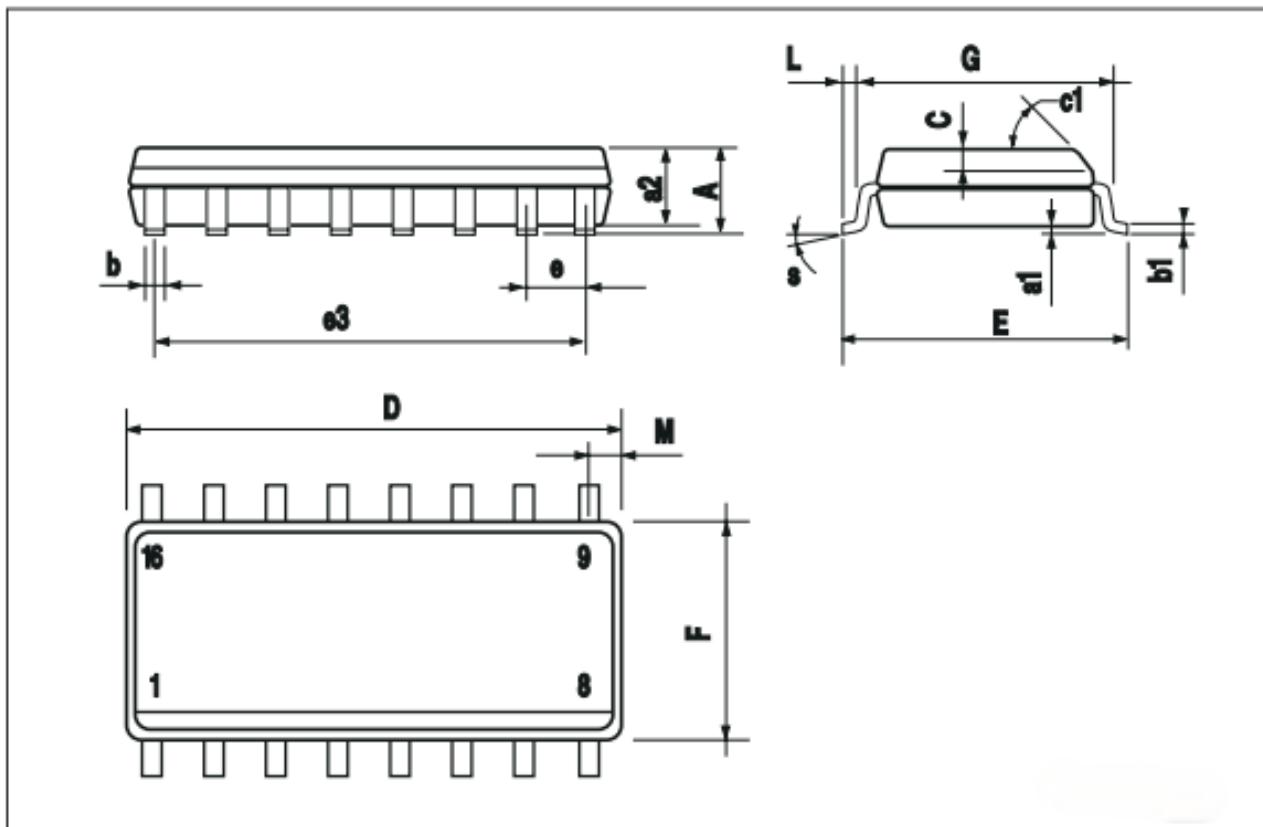
### 7.1 DIP16

| Dim. | mm.  |       |      | inch. |       |       |
|------|------|-------|------|-------|-------|-------|
|      | Min. | Typ.  | Max. | Min.  | Typ.  | Max.  |
| a1   | 0.51 |       |      | 0.020 |       |       |
| B    | 0.77 |       | 1.65 | 0.030 |       | 0.065 |
| b    |      | 0.5   |      |       | 0.020 |       |
| b1   |      | 0.25  |      |       | 0.010 |       |
| D    |      |       | 20   |       |       | 0.787 |
| E    |      | 8.5   |      |       | 0.335 |       |
| e    |      | 2.54  |      |       | 0.100 |       |
| e3   |      | 17.78 |      |       | 0.700 |       |
| F    |      |       | 7.1  |       |       | 0.280 |
| I    |      |       | 5.1  |       |       | 0.201 |
| L    |      | 3.3   |      |       | 0.130 |       |
| Z    |      |       | 1.27 |       |       | 0.050 |



## 7.2 SOP16

| Dim. | mm.        |      |      | inch. |       |       |
|------|------------|------|------|-------|-------|-------|
|      | Min.       | Typ. | Max. | Min.  | Typ.  | Max.  |
| A    |            |      | 1.75 |       |       | 0.068 |
| a1   | 0.1        |      | 0.25 | 0.004 |       | 0.010 |
| a2   |            |      | 1.64 |       |       | 0.063 |
| b    | 0.35       |      | 0.46 | 0.013 |       | 0.018 |
| b1   | 0.19       |      | 0.25 | 0.007 |       | 0.010 |
| C    |            | 0.5  |      |       | 0.019 |       |
| c1   | 45° (typ.) |      |      |       |       |       |
| D    | 9.8        |      | 10   | 0.385 |       | 0.393 |
| E    | 5.8        |      | 6.2  | 0.228 |       | 0.244 |
| e    |            | 1.27 |      |       | 0.050 |       |
| e3   |            | 8.89 |      |       | 0.350 |       |
| F    | 3.8        |      | 4.0  | 0.149 |       | 0.157 |
| G    | 4.6        |      | 5.3  | 0.181 |       | 0.208 |
| L    | 0.5        |      | 1.27 | 0.019 |       | 0.050 |
| M    |            |      | 0.62 |       |       | 0.024 |
| S    | 8° (max.)  |      |      |       |       |       |



## 7.3 TSSOP16

| Dim. | mm.  |          |      | inch. |            |        |
|------|------|----------|------|-------|------------|--------|
|      | Min. | Typ.     | Max. | Min.  | Typ.       | Max.   |
| A    |      |          | 1.2  |       |            | 0.047  |
| A1   | 0.05 |          | 0.15 | 0.002 | 0.004      | 0.006  |
| A2   | 0.8  | 1        | 1.05 | 0.031 | 0.039      | 0.041  |
| b    | 0.19 |          | 0.30 | 0.007 |            | 0.012  |
| c    | 0.09 |          | 0.20 | 0.004 |            | 0.0079 |
| D    | 4.9  | 5        | 5.1  | 0.193 | 0.197      | 0.201  |
| E    | 6.2  | 6.4      | 6.6  | 0.244 | 0.252      | 0.260  |
| E1   | 4.3  | 4.4      | 4.48 | 0.169 | 0.173      | 0.176  |
| e    |      | 0.65 BSC |      |       | 0.0256 BSC |        |
| K    | 0°   |          | 8°   | 0°    |            | 8°     |
| L    | 0.45 | 0.60     | 0.75 | 0.018 | 0.024      | 0.030  |

