JW9624

Dual 4.5A High-Speed, Low-Side Gate Driver

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®9624 is a dual-channel, high-speed, low-side gate-driver device capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, JW9624 can deliver high peak pulses of up to 4.5A source and 4.5A sink into capacitive loads along with rail-to-rail drive capability and extremely small propagation delay (typical 13ns). In addition, the driver features matched internal propagation delays between the two channels. These delays are very well suited for applications requiring dual-gate drives with critical timing, such as synchronous rectifiers. This also enables connecting two channels in parallel to effectively increase current-drive capability or driving two switches in parallel with one input signal. The input pin thresholds are based on TTL and CMOS compatible low-voltage logic, which is fixed and independent of the V_{DD} supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

The JW9624 guarantees robustness with input supply under voltage lock out (UVLO).

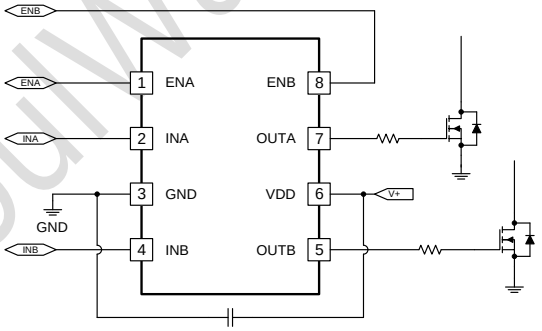
FEATURES

- Two Independent Gate-Drive Channels
- 4.5A Peak Source and Sink-Drive Current
- Independent-Enable Function for Each Output
- TTL and CMOS Compatible Logic Threshold Independent of Supply Voltage
- Hysteretic-Logic Thresholds for High Noise Immunity
- 4.5V To 20V Single-Supply Range
- Outputs Held Low During V_{DD}-UVLO, (Ensures Glitch-Free Operation at Power Up and Power Down)
- Fast Propagation Delays (13ns typical)
- Fast Rise and Fall Times (7ns and 6ns typical)
- 1ns Typical Delay Matching between Two Channels
- Two Outputs are Paralleled for Higher Drive Current
- Outputs Held Low when Inputs Floating
- SOP-8, EMSOP-8, DFN3X3-8 Package
- Operating Temperature: -40℃ to 140℃

APPLICATIONS

- Switched-Mode Power Supplies
- DC-DC Converters
- Motor Control, Solar Power
- Gate Drive for Emerging Wide Band-Gap Power Devices such as GaN

TYPICAL APPLICATION



Typical application circuit

ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW9624SOPB#TRPBF	SOP8	JW9624 YW□□□□□
JW9624EMSOPA#TRPBF	EMSOP8	JW9624 YW□□□□□
JW9624DFNA#TRPBF	DFN3X3-8	JW9624 YW□□□□□

Notes:

1) JW□□□□# TRPBF
- PB Free
- Tape and Reel(If" TR" is not shown, it means tube)
- Package Code
- Part No.

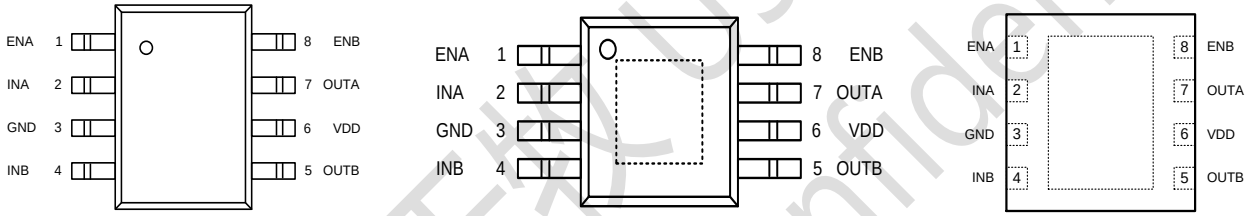
2) Line1: JW□□□□
- Product code
- Joulwatt LOGO

Line2: YW□□□□□
- Lot number
- Week code
- Year code

3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION

TOP VIEW



SOP-8 EMSOP-8 DFN3X3-8

ABSOLUTE MAXIMUM RATING[1)]

Supply Voltage, V_{DD} ..... -0.3V to 25V
OUTA, OUTB Voltage (DC) ..... -0.3V to V_{DD} + 0.3V
OUTA, OUTB Voltage (Repetitive pulse < 200ns) ..... -2V to V_{DD} + 0.3V
Output source/sink current (Continuous) 0.3A
Output source/sink current (Pulse < 0.5μs) 4.5A
INA, INB, ENA, ENB Voltage (DC) ..... -0.3V to 25V
INA, INB, ENA, ENB Voltage (Repetitive pulse < 20ns) ..... -5V to 25V
JunctionTemperature ..... -40ºC to 150ºC
Lead Temperature 260ºC
Storage Temperature ..... -65ºC to +150ºC
ESD Rating (Human-body model, HBM) ..... ±4kV
ESD Rating (Charged-device model, CDM) ..... ±1kV

RECOMMENDED OPERATING CONDITIONS[2)]

V_{DD} ..... 4.5V to 20V
INA, INB ..... 0V to 20V
ENA, ENB ..... 0V to 20V
Operation Junction Temperature (T_J) ..... -40ºC to +140ºC

THERMAL PERFORMANCE[3)]

	θ_{JA}	θ_{JC}
SOP8	130.9	80.0ºC/W
EMSOP8	71.8	65.6ºC/W
DFN3X3-8	46.7	46.7ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDE OPERATING CONDITIONS.

2) The device is not guaranteed to function outside of its operating conditions.

3) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD}=12V, T_A=T_J=-40℃ to 140℃, 1μF capacitor from V_{DD} to GND. Currents are positive into, negative out of the specified terminal (unless otherwise stated).

Item	Symbol	Condition	Min.	Typ.	Max.	Units
Bias Currents						
Start-up current	$I_{DD(off)}$	V_{DD}=3.4V, INA=V_{DD}, INB=V_{DD}	140	280	420	μA
		V_{DD}=3.4V, INA=GND, INB=GND	140	280	420	
Under Voltage Lock Out (UVLO)						
Supply start threshold	V_{ON}		3.91	4.2	4.5	V
Minimum operating voltage after supply start	V_{OFF}		3.4	3.89	4.4	
Supply voltage hysteresis	V_{DD_HYS}		0.25	0.31	0.4	
V_{DD} UVLO to OUT delay	t_{DD}	V_{DD} rising			6	μs
INA, INB						
Input signal high threshold	V_{IN_H}	Output high	1.93	2.13	2.33	V
Input signal low threshold	V_{IN_L}	Output low	1	1.2	1.4	
Input hysteresis	V_{IN_HYS}		0.73	0.93	1.13	
Input pull-down resistance	R_{IL}			400		kΩ
ENA, ENB						
Enable signal high threshold	V_{EN_H}	Output enabled	1.93	2.13	2.33	V
Enable signal low threshold	V_{EN_L}	Output disabled	1	1.2	1.4	
Enable hysteresis	V_{EN_HYS}		0.73	0.93	1.13	
Enable pull-up resistance	R_{EH}			200		kΩ
OUTA, OUTB						
Sink peak current[4)]	I_{SNK}	C_{LOAD}=0.22μF, F_{SW}=1kHz		4.5		A
Source peak current[4)]	I_{SRC}			-4.5		
High output voltage	V_{DD}-V_{OH}	I_{OUT}= -10mA			0.07	V
Low output voltage	V_{OL}	I_{OUT}= 10mA			0.014	
Output pull-up resistance[4)]	R_{OH}			0.74		Ω
Output pull-down resistance[4)]	R_{OL}			0.74		

Notes:

4) Guaranteed by design.

SWITCHING CHARACTERISTICS

Over operating free-air temperature range (unless otherwise stated)

Item	Symbol	Condition	Min.	Typ.	Max.	Units
Rise time	t_R	C_{LOAD} = 1.8nF		7	18	ns
Fall time	t_F	C_{LOAD} = 1.8nF		6	13	
Delay matching between two channels	t_M	INA=INB, OUTA and OUTB at 50% transition point		1	4[4)]	
Minimum input pulse width that changes the output state[4)]	t_{PW}			15	25	
Input to output propagation delay	t_{D1}, t_{D2}	C_{LOAD} = 1.8nF, 5V input pulse	6	13	30	
EN to output propagation delay	t_{D3}, t_{D4}	C_{LOAD} = 1.8nF, 5V enable pulse	6	13	30	

Notes:

4) Guaranteed by design.

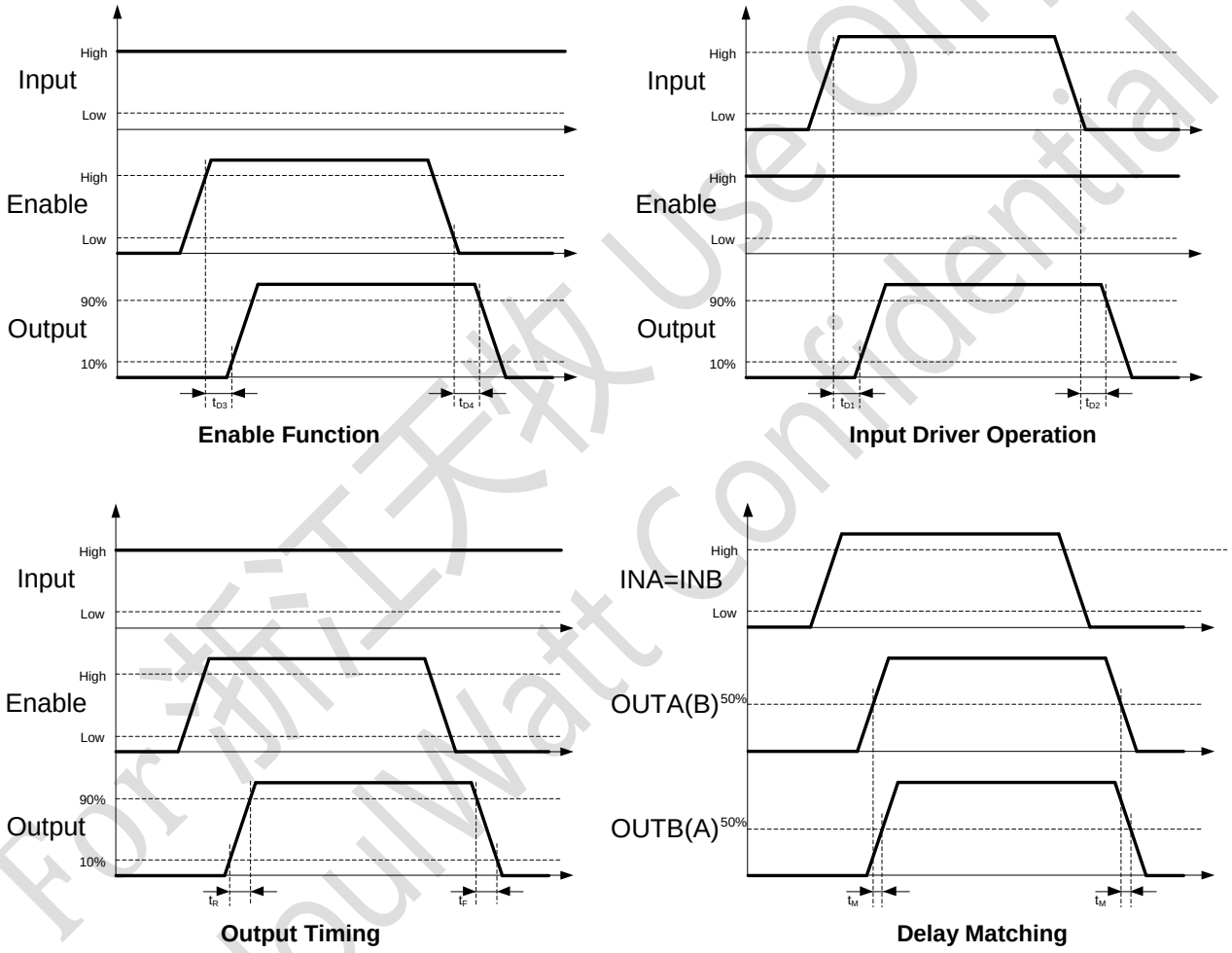


Figure 1. Switching Characteristics for JW9624

PIN DESCRIPTION

Pin No.	Name	Description
1	ENA	Enable input for channel A: ENA bias LOW disable channel A output regardless of INA state, ENA biased HIGH or floating enables channel A output.
2	INA	Input to channel A: OUTA held LOW if INA is unbiased or floating.
3	GND	Ground
4	INB	Input to channel B: OUTB held LOW if INB is unbiased or floating.
5	OUTB	Output of channel B
6	V_{DD}	Bias supply input
7	OUTA	Output of channel A
8	ENB	Enable input for channel B: ENB bias LOW disable channel B output regardless of INB state, ENB biased HIGH or floating enables channel B output.
Exposed Pad		Thermal Pad. The exposed pad is not directly connected to any leads of the package. It is recommended to externally connecting this pad to GND in PCB layout for better EMI immunity and thermal performance.

BLOCK DIAGRAM

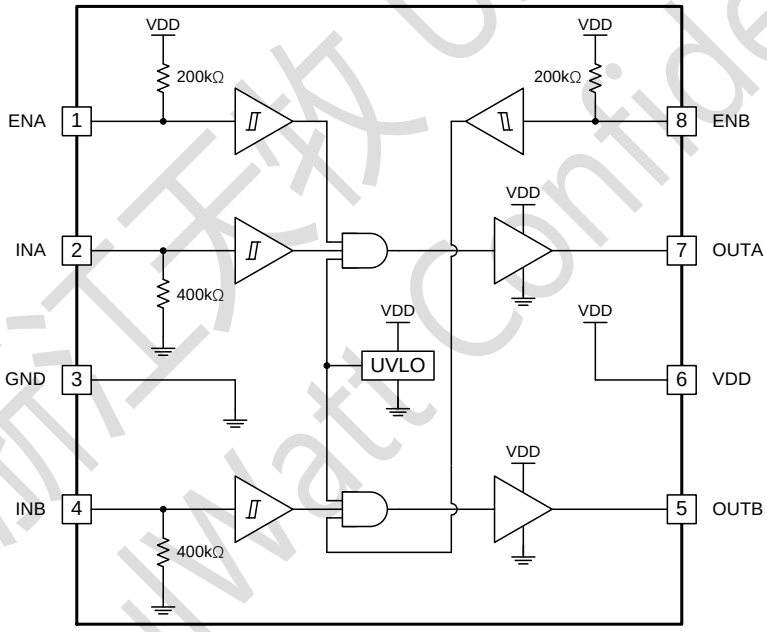


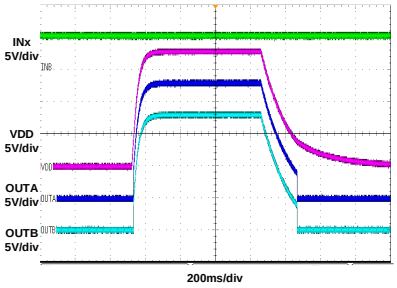
Figure 2. JW9624 Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD}=12V, T_A = +25°C, C_{OUTA}=1.8nF, C_{OUTB}=1.8nF, unless otherwise noted.

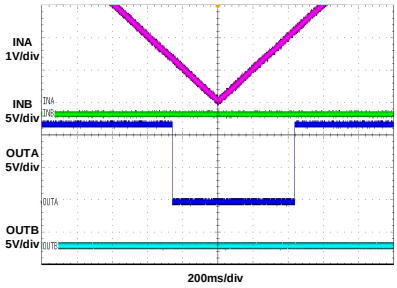
V_{DD} On/off

V_{DD}=0←→18V, INA=INB=5V



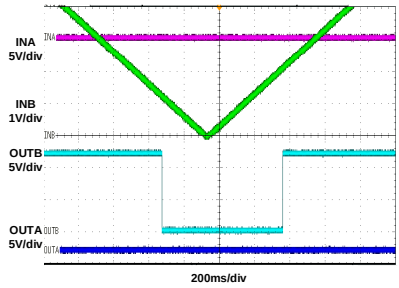
INA Slow On/off

INA=0V←→5V (Triangle, 1Hz), INB float



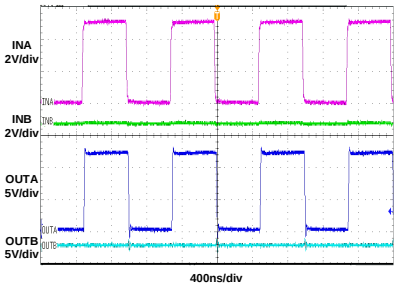
INB Slow On/off

INB=0V←→5V (Triangle, 1Hz), INA float



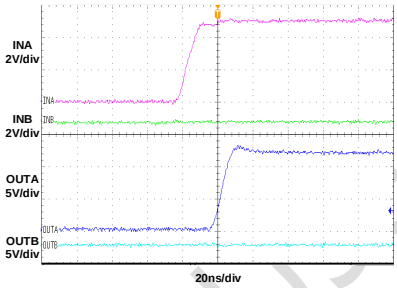
INA Quick On/off

INA=0V←→5V (Square, 1MHz), INB float



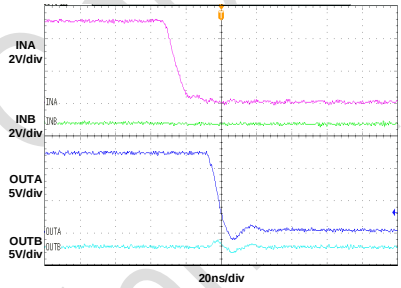
Channel A Propagation Delay

INA=0V→5V, INB float



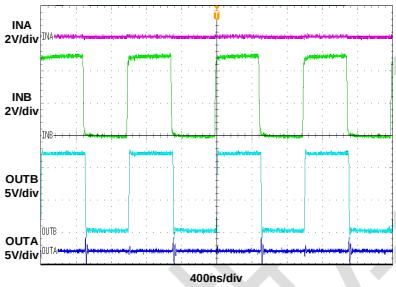
Channel A Propagation Delay

INA=5V→0V, INB float



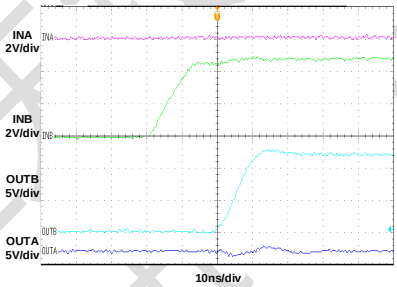
INB Quick On/off

INB=0V←→5V (Square, 1MHz), INA float



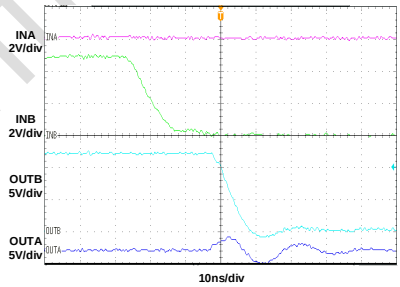
Channel B Propagation Delay

INB=0V→5V, INA float



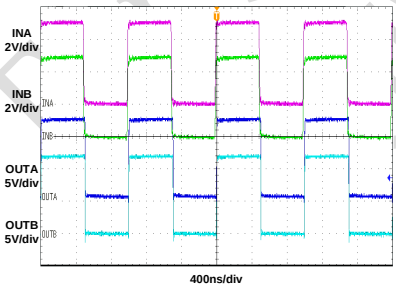
Channel B Propagation Delay

INB=5V→0V, INA float



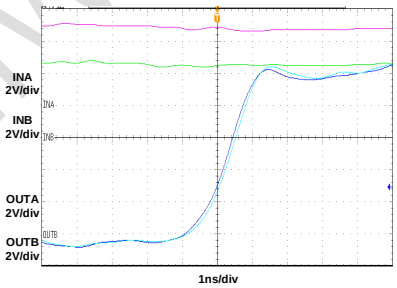
INA=INB Quick On/off

INA=INB=0V←→5V, OUTA/ OUTB float



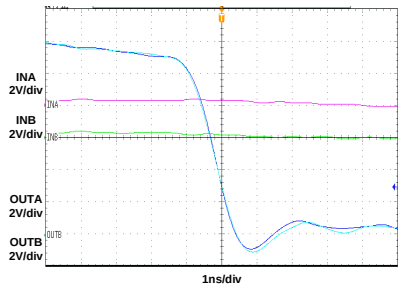
Propagation Delay Match

INA=INB=0V→5V, OUTA/ OUTB float



Propagation Delay Match

INA=INB=5V→0V, OUTA/ OUTB float

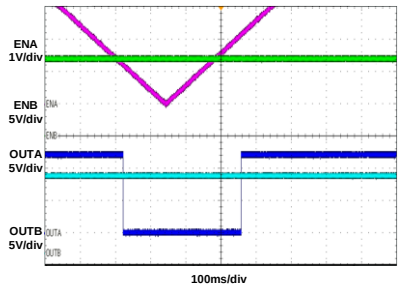


TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD}=12V, T_A = +25°C, C_{OUTA}=1.8nF, C_{OUTB}=1.8nF, unless otherwise noted.

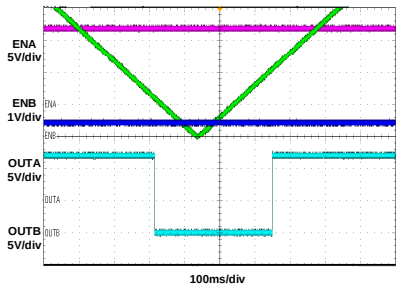
ENA Slow On/off

ENA=0V←→5V, ENB float, INA=INB=5V



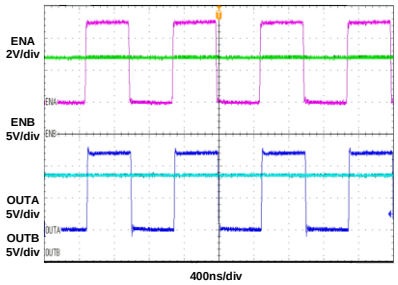
ENB Slow On/off

ENB=0V←→5V, ENA float, INA=INB=5V



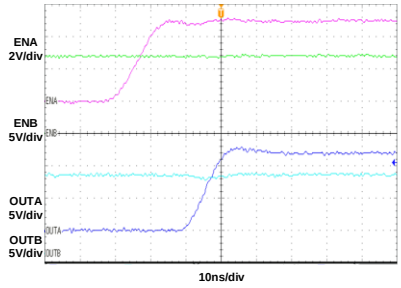
ENA Quick On/off

ENA=0V←→5V, ENB float, INA=INB=5V



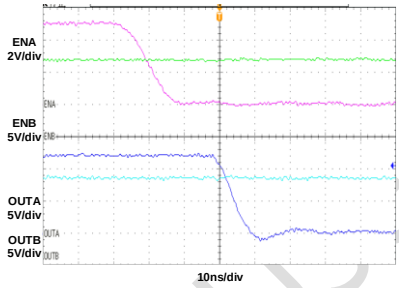
ENA Propagation Delay

ENA=0V→5V, ENB float, INA=INB=5V



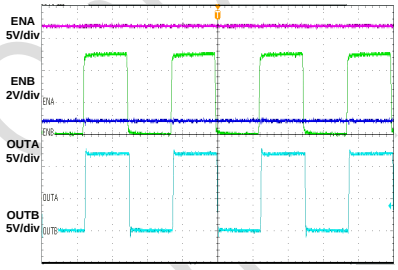
ENA Propagation Delay

ENA=5V→0V, ENB float, INA=INB=5V



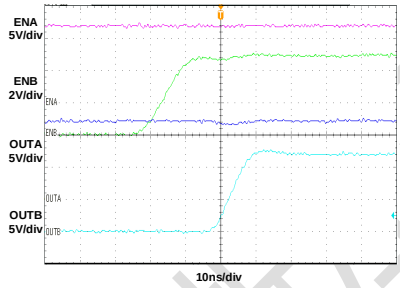
ENB Quick On/off

ENB=0V←→5V, ENA float, INA=INB=5V



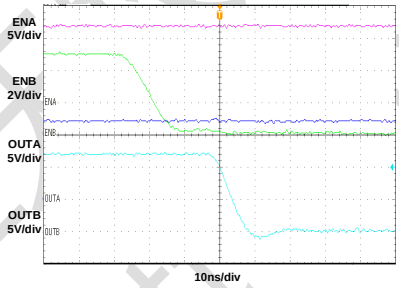
ENB Propagation Delay

ENB=0V→5V, ENA float, INA=INB=5V



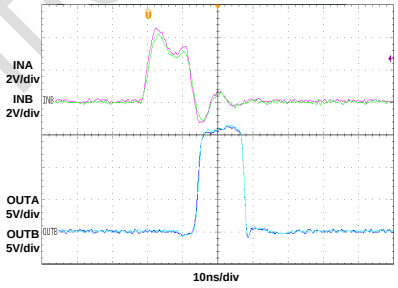
ENB Propagation Delay

ENB=5V→0V, ENA float, INA=INB=5V



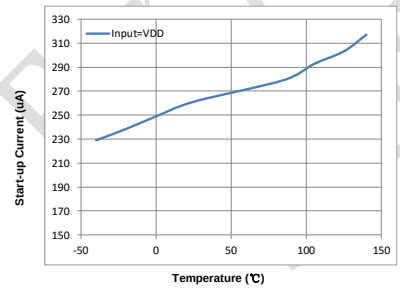
Short Pulse Input

INA=INB=12ns short pulse



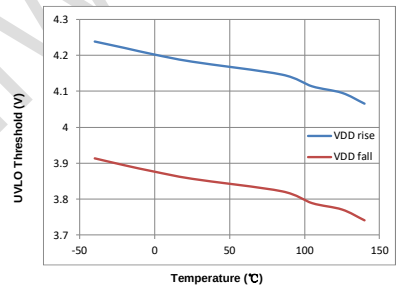
Start-up Current vs Temperature

INA=INB=V_{DD}



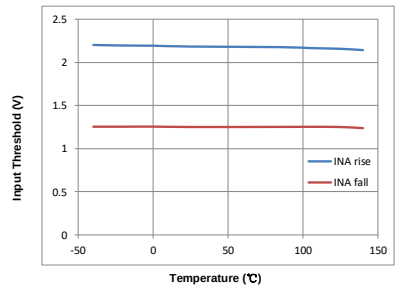
UVLO Threshold vs Temperature

V_{DD}=3V→5V→3V



Input Threshold vs Temperature

Channel A

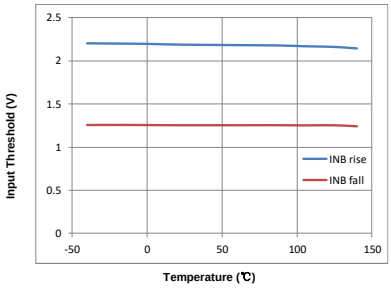


TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD}=12V, T_A = +25°C, C_{OUTA}=1.8nF, C_{OUTB}=1.8nF, unless otherwise noted.

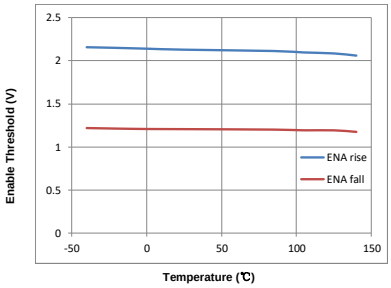
Input Threshold vs Temperature

Channel B



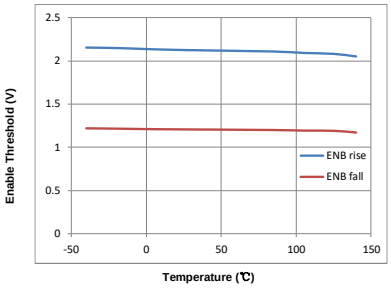
Enable Threshold vs Temperature

Channel A



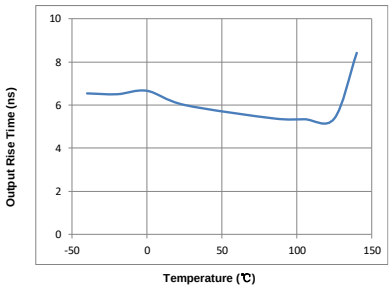
Enable Threshold vs Temperature

Channel B



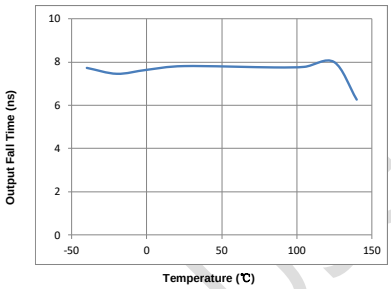
Output Rise Time vs Temperature

C_{LOAD}=1.8nF



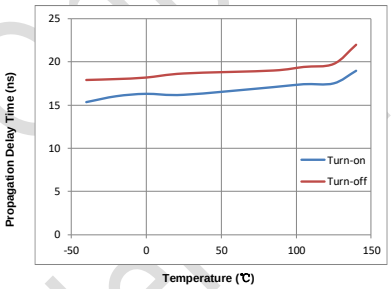
Output Fall Time vs Temperature

C_{LOAD}=1.8nF



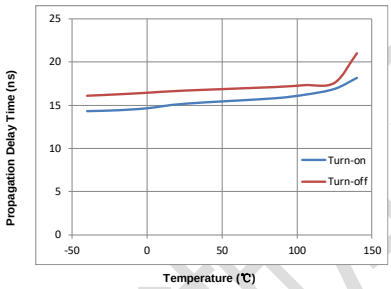
Propagation Delay vs Temperature

INA to OUTA propagation delay



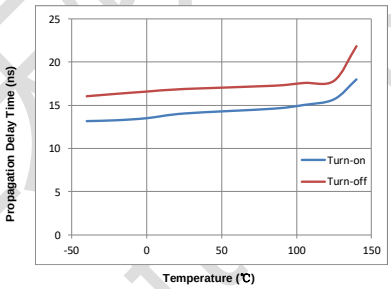
Propagation Delay vs Temperature

INB to OUTB propagation delay



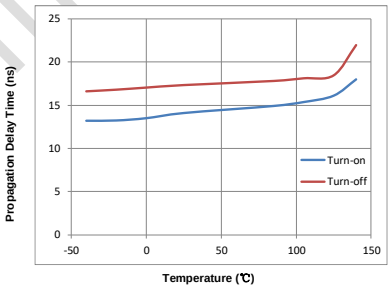
Propagation Delay vs Temperature

ENA to OUTA propagation delay



Propagation Delay vs Temperature

ENB to OUTB propagation delay



FUNCTIONAL DESCRIPTION

V_{DD} and Under Voltage Lock Out

The JW9624 has internal under voltage lock out (UVLO) protection features on the V_{DD} pin supply circuit block. When V_{DD} is rising and the level is still below UVLO threshold, this circuit holds the output LOW, regardless of the status of the inputs. The UVLO is typically 4.2V with 310mV typical hysteresis. This hysteresis prevents chatter when low V_{DD} supply voltage has noise from the power supply and also when there are droops in the V_{DD} bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low voltage levels such as below 5V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN power semiconductor devices.

Because the device draws current from the V_{DD} pin to bias all internal circuits, it is recommended two V_{DD} bypass capacitors to prevent noise problems. A 0.1μF ceramic capacitor must be located as close as possible to the V_{DD} to GND pins of the gate-driver device. In addition, a larger capacitor (such as 1μF) with relatively low ESR must be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

Input Stage

The input pins of JW9624 are based on a TTL and CMOS compatible input-threshold logic that is independent of the V_{DD} supply voltage. With typically high threshold = 2.13V and typically low threshold = 1.2V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3V and 5V digital power-controller devices. The wide hysteresis (typical 0.93V) offers high noise immunity. JW9624 also features tight control of the input pin threshold voltage levels which eases system design considerations. The very low input capacitance on these pins reduces loading and increases switching speed. The JW9624 features an important safety feature wherein, whenever any of the input pins is in a floating condition, the output of the respective channel is held in the low state. This is achieved using GND pull down resistors on input pins.

Device Functional Modes

The JW9624 is provided with independent enable pins ENA and ENB for exclusive control of each driver channel operation. Like the input pins, the enable pins are also based on a TTL and CMOS compatible input-threshold logic that is independent of the supply voltage and are effectively controlled using logic signals from 3.3V and 5V microcontrollers. The JW9624 also features tight control of the Enable-function threshold-voltage levels which eases system design considerations. The ENA and ENB pins are internally pulled up to V_{DD} using pull up resistors as a result of which the outputs of the device are enabled in the default state. Table 1 shows the device logic of JW9624.

Table 1. Device Logic Table

ENA	ENB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	x	x	L	L
x(1)	x	L	L	L	L
x	x	L	H	L	H
x	x	H	L	H	L
x	x	H	H	H	H

(1) x = Floating condition

Output Stage

The two rail-to-rail output stages are able to provide a typical 4.5A peak sourcing and sinking capabilities. Add a resistor in series with OUTx to slow the corresponding rise/fall time of the MOSFET gate. The driver output stage has a shoot through protection. Gate Drive Outputs held active low during startup or power down once UVLO is not exceeded. Under any situation, startup, UVLO or shutdown, outputs are held under defined conditions.

PCB Layout Guidelines

For minimum noise problem and best operating performance, the PCB layout of JW9624 must be carefully designed:

1. Locate the V_{DD} bypass capacitors between V_{DD} and GND as close as possible to the driver with minimal trace length to improve the noise filtering. The bypass capacitors can be placed on bottom layer.
2. Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the Output pins and the Gate of the power device.
3. Current loop paths should be minimized parallel the source and return traces, taking advantage of flux cancellation, if feasible, while routing the tracks.
4. Use a ground plane to provide noise shielding and recommends to externally connect the exposed pads to GND in PCB layout for better thermal and EMI immunity.

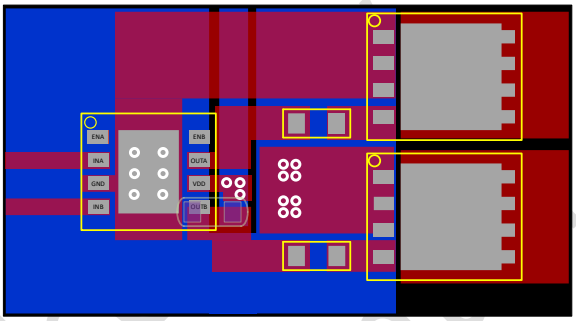
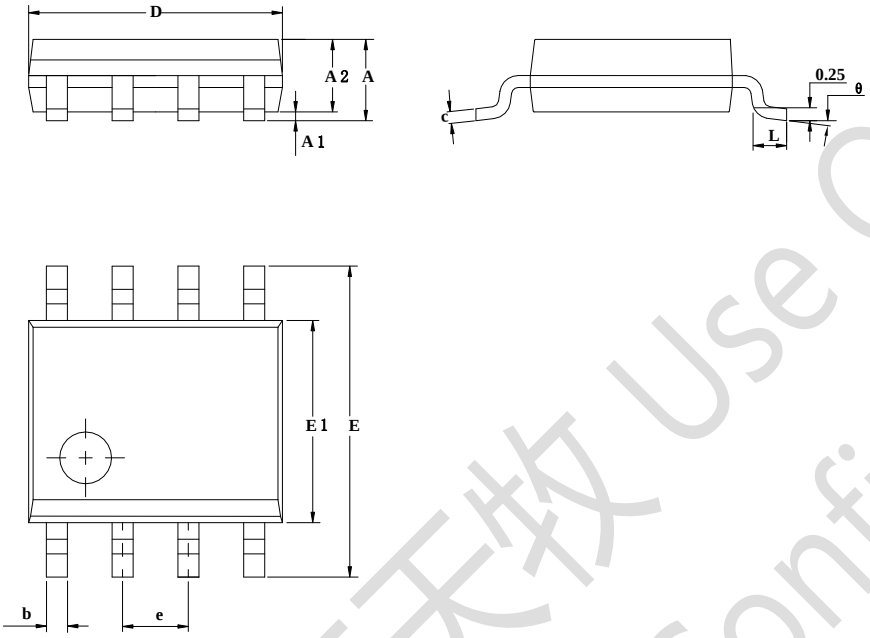


Figure 3. JW9624 PCB Layout Example (DFN)

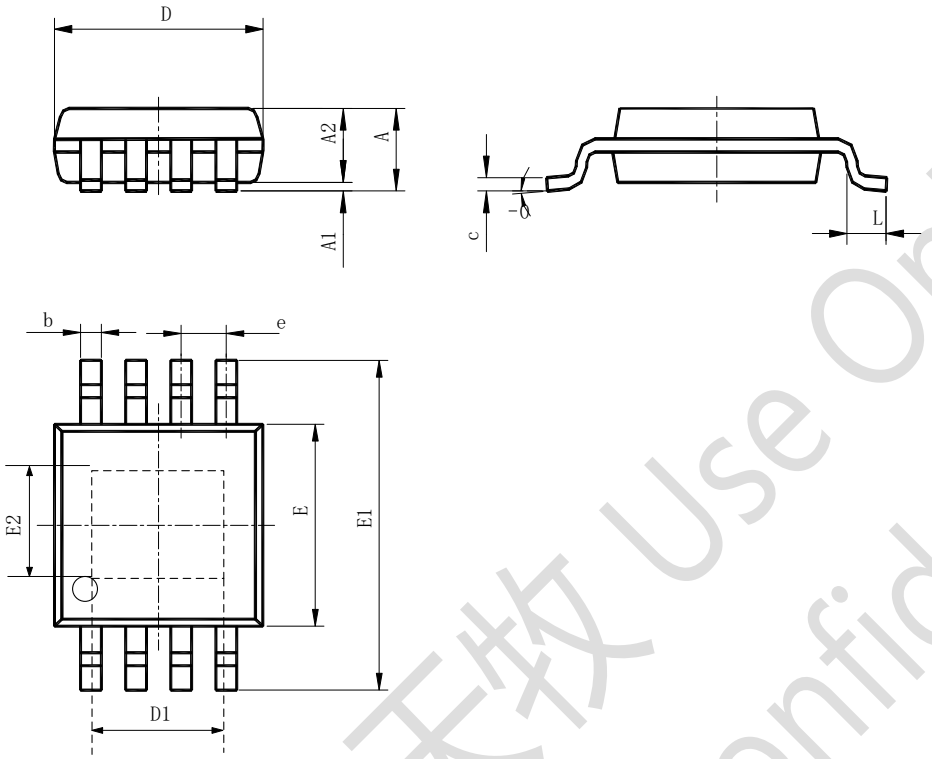
PACKAGE OUTLINE

SOP8 UNIT: mm



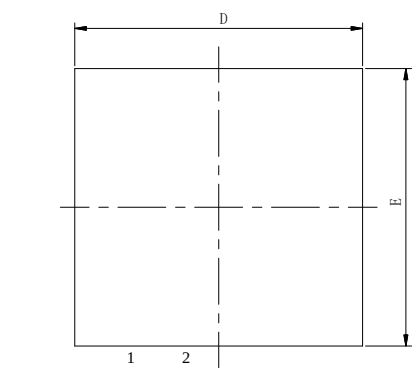
Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	0.15	0.25
A2	1.25	1.40	1.65
b	0.32	0.42	0.52
c	0.10	0.20	0.30
D	4.50	5.00	5.50
E	5.50	6.00	6.50
E1	3.50	3.90	4.30
e	1.27TYP		
L	0.40	—	1.27
θ	0°	—	8°

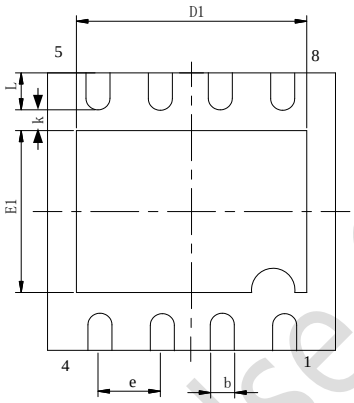
EMSOP8 UNIT: mm

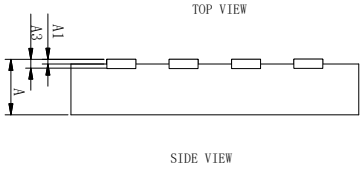


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.82	—	1.10
A1	0.02	—	0.15
A2	0.75	—	0.95
b	0.25	—	0.38
c	0.09	—	0.23
D	2.90	3.00	3.10
D1	1.70	—	1.90
E1	4.75	—	5.05
E	2.90	3.00	3.10
E2	1.45	—	1.65
e	0.65BSC		
L	0.40	—	0.80
θ	0	—	6°

DFN3X3-8 UNIT: mm







SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.203REF		
D	2.924	3.00	3.076
E	2.924	3.00	3.076
D1	2.20	2.30	2.40
E1	1.40	1.50	1.60
k	0.20	—	—
b	0.20	—	0.30
e	0.650TYP		
L	0.399	**0.450**	0.551

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