6-LVPECL Output Ultra-Low Additive Jitter/Differential Clock Buffer

Description

The US5D8946 is a 2-GHz,6-output differential high-performance clock fanout buffer.
The US5D8946 is a highly versatile, low additive jitter buffer that can generate six copies of LVPECL clock outputs.The can accept LVPECL, LVDS, HCSL or LVCMOS(single-ended) inputs.The device has a differential input equipped with center-tapped, differential, 100 Ω on-chip termination resistors.It has a maximum clock frequency up to 2- GHz.

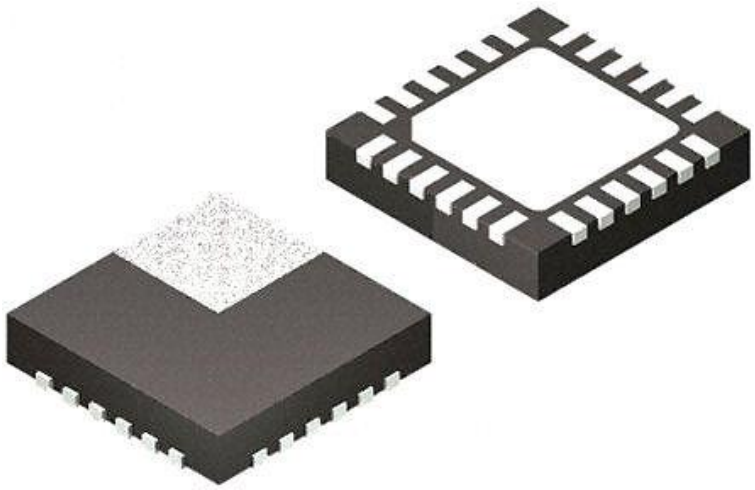
The device is designed for a signal fanout of high-frequency, low phase-noise clock and data signal. It is designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.

Applications

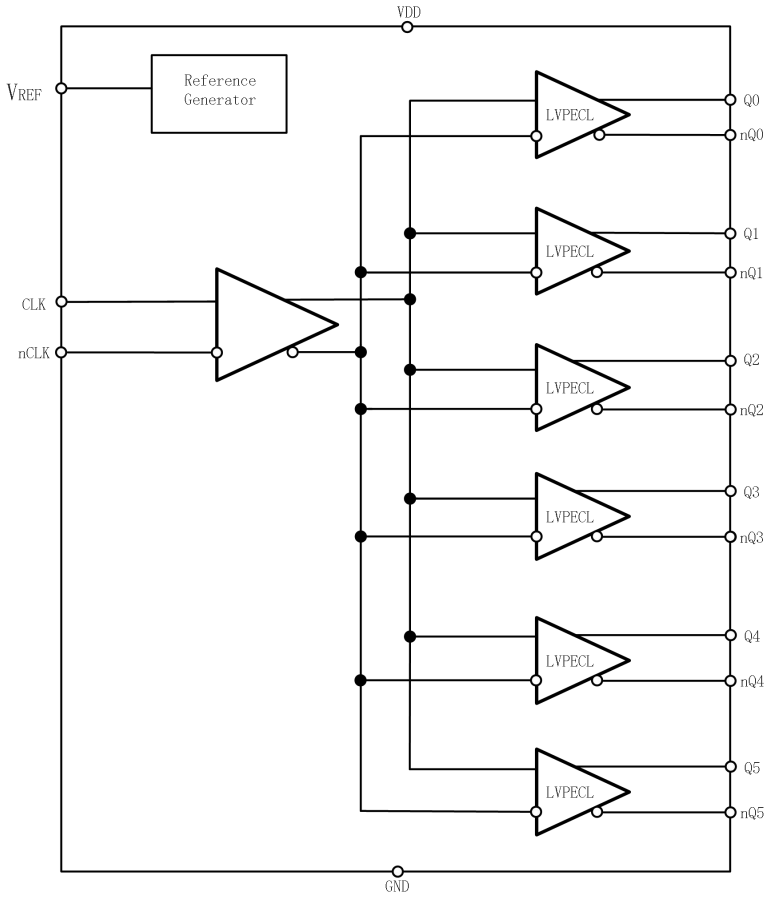
- Clock distribution and level translation for ADCs, DACs, Multi-Gigabit Elthernet, XAUI, Fibre channel, SATA/SAS, SONET/SDH,CPRI, High-Frequency Backplanes
- Switches, Routers, Line Cards, Timing Cards
- Servers, Computing, PCI Express(PCIe 3.0,4.0,5.0)
- Remote Radio Units and Baseband Units

Features

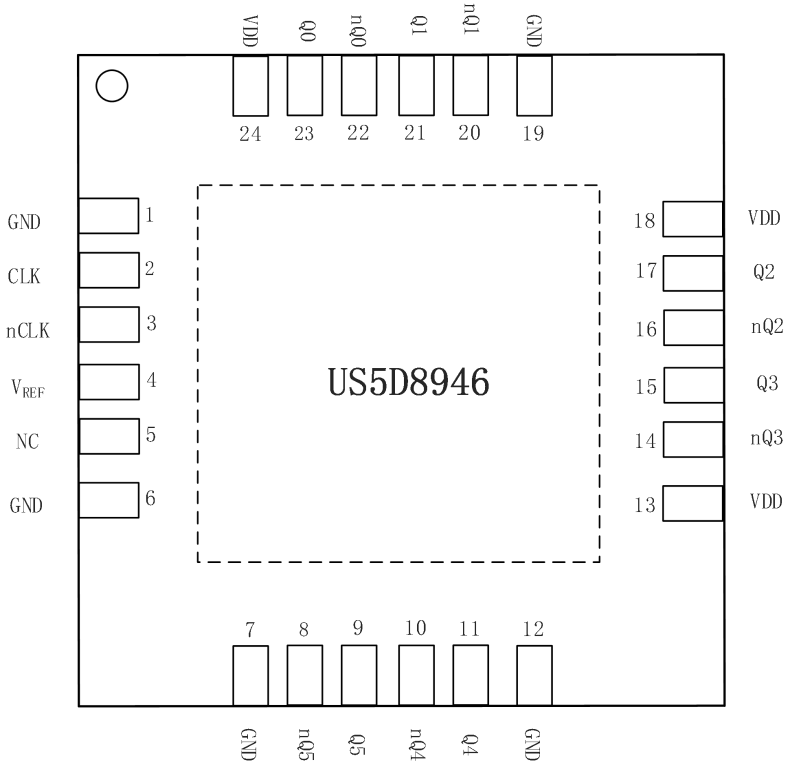
- 1:6 Differential Buffer
- Universal Input Accept LVPECL,LVDS and HCSL
- Six LVPECL output
- Maximum Output Frequency LVPECL
  - 2-GHz
- Maximum Propagation Delay:350ps(typical)
- Output skew: 20 ps (typical)
- Part-to-part skew< 300ps
- Additive RMS phase jitter @ 156.25MHz: 50fs RMS (12kHz - 20MHz), typical @ 3.3V/ 3.3V
- Supply voltage : VDD= 3.3V or 2.5V
- Industrial Temperature Range:-40°C to 85°C
- Available in QFN-24(4mm x 4mm) package



Block Diagram



Pin Assignment for QFN-24 Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type	Description
1	GND	Power	Ground.
2	CLK	Input	Differential input pair.
3	nCLK	Input	Differential input pair.
4	V_{REF}	Input	Reference Voltage. This pin provides the reference voltage for biasing ac-coupled CLK and CLK inputs.
5	NC	NC	Not connect.
6	GND	Power	Ground.
7	GND	Power	Ground.
8	nQ5	Output	Differential LVPECL output pair no. 5. Unused output pair can be left floating.
9	Q5	Output	Differential LVPECL output pair no. 5. Unused output pair can be left floating.
10	nQ4	Output	Differential LVPECL output pair no. 4. Unused output pair can be left floating.
11	Q4	Output	Differential LVPECL output pair no. 4. Unused output pair can be left floating.
12	GND	Power	Ground.
13	VDD	Power	Power supply.
14	nQ3	Output	Differential LVPECL output pair no. 3. Unused output pair can be left floating.
15	Q3	Output	Differential LVPECL output pair no. 3. Unused output pair can be left floating.
16	nQ2	Output	Differential LVPECL output pair no. 2. Unused output pair can be left floating.
17	Q2	Output	Differential LVPECL output pair no. 2. Unused output pair can be left floating.
18	VDD	Power	Power supply.
19	GND	Power	Ground.
20	nQ1	Output	Differential LVPECL output pair no. 1. Unused output pair can be left floating.
21	Q1	Output	Differential LVPECL output pair no. 1. Unused output pair can be left floating.
22	nQ0	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating.
23	Q0	Output	Differential LVPECL output pair no. 0. Unused output pair can be left floating.
24	VDD	Power	Power supply.

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD}	4.6V
V_{IN}	-0.5V to V_{DD} + 0.5V
T_J :Junction Temperature	125°C
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	°C
T_J	Junction temperature			125	°C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5% 2.5-5%	3.3 2.5	3.3+5% 2.5+5%	V

Electrical Characteristics

At VDD = 3.3 V and TA = –40°C to +85°C and TPCB ≤ 105°C (unless otherwise noted).

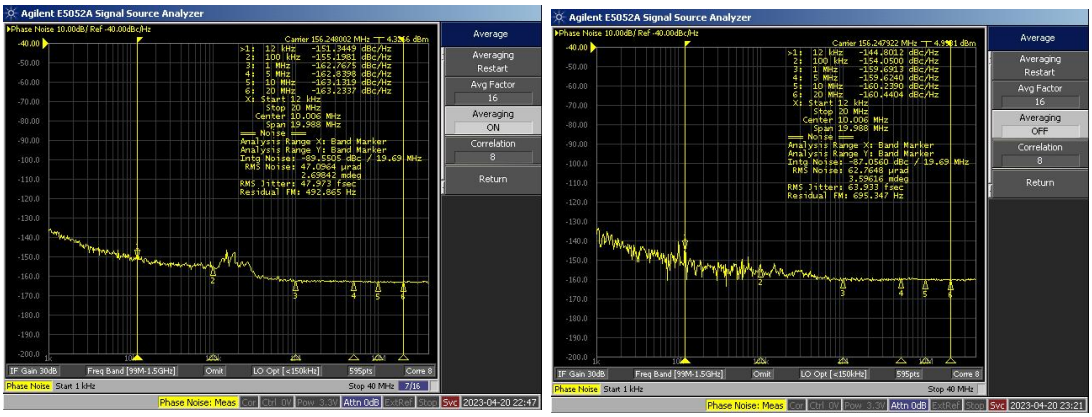
Parameter		Test Conditions	Min	Typ	Max	Unit
DC input characteristics						
V_{IH}	Input High Voltage		1.6		VDD	V
V_{IL}	Input Low Voltage		GND		VDD-0.2	V
V_{ID}	Input Differential Voltage	±1.7V between input pins	0.4		3.4	Vp-p
C_{IN}	Input capacitance			0.4		pF
DC output characteristics						
V_{OH}	Output High Voltage	Load=50Ω to(VDD-2.0V)	VDD-1.26		VDD-0.76	V
V_{OL}	Output Low Voltage	Load=50Ω to(VDD-2.0V)	VDD-1.99		VDD-1.54	
V_{OD}	Output Voltage Swing		610		1040	mV
V_{REF}	Reference Voltage			VDD/2		V

Electrical Characteristics(Continued)

VCC = 3.3 V; TA = –40°C to +85°C and TPCB ≤ 105°C (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
AC PERFORMANCE						
F_{OUT}	Output Frequency		0.1		2000	MHz
I_{DD}	Operating current	VDD=3.3V, All outputs active		250		mA
T_R/T_F	Output Rise/Fall Time	20% to 80%		120	300	ps
T_{PD}	Propagation Delay			350	600	ps
$T_{SK,O}$	Output skew				30	ps
$T_{sk,pp}$	Part-to-Part Skew				300	ps
T_{RJIT}	Additive jitter	Additive RMS phase jitter @ 156.25MHz: (12kHz - 20MHz)		TBD		fs

PHASE JITTER



(a)Jitter_Source (b)3V3_156M25_LVPECL

Figure 1 .RMS_Jitter_3V3=Sqrt(64²-48²)=38fs

The additive phase jitter for this device was measured using the Low jitter SPXO(156.25MHz) as an input source with and Agilent E5052A phase noise analyzer. (VDD=3.3V)

Timing Diagrams

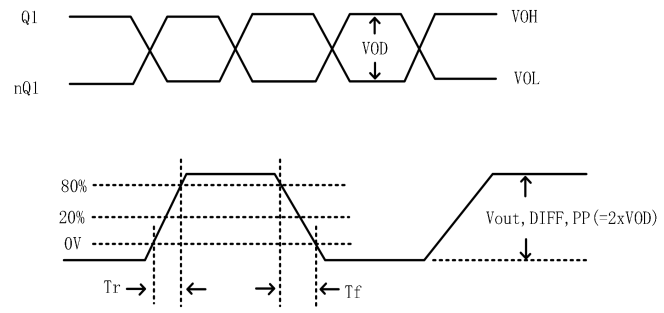
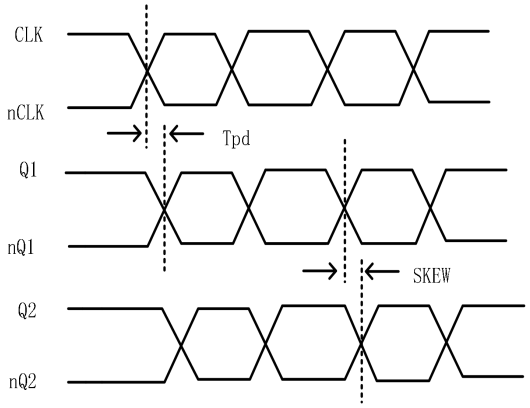


Figure 2.output voltage and rise/fall time



(1) Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn(n = 0, 1, 2....7), or as the difference between the fastest and the slowest tPHLn (n = 0, 1, 2....7).
(2) Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest tPLHn (n = 0, 1, 2....7) across multiple devices, or the difference between the fastest and the slowest tPHLn (n = 0, 1,2....7) across multiple devices

Figure 3.output and skew

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

For the single-ended input LVCMOS signal, Rs and R0 in the driver form a 50Ω impedance match, and the direct-isolated capacitor C3 avoids the influence of the common-mode level between the input and output, and then drives the receiver through the voltage divider and the common-mode level to VDD/2.

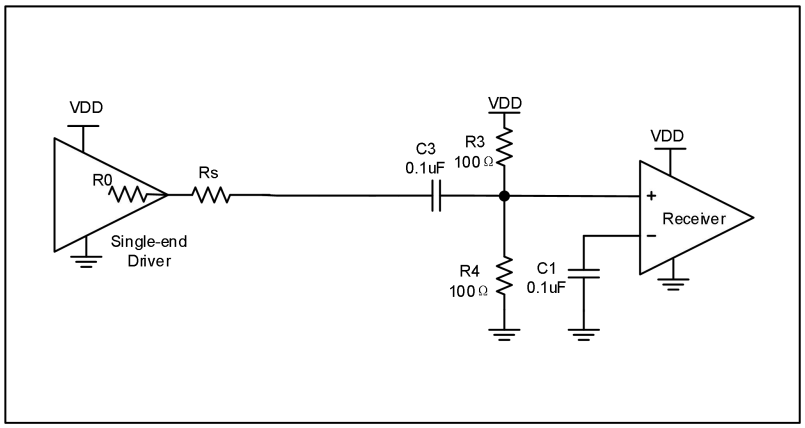
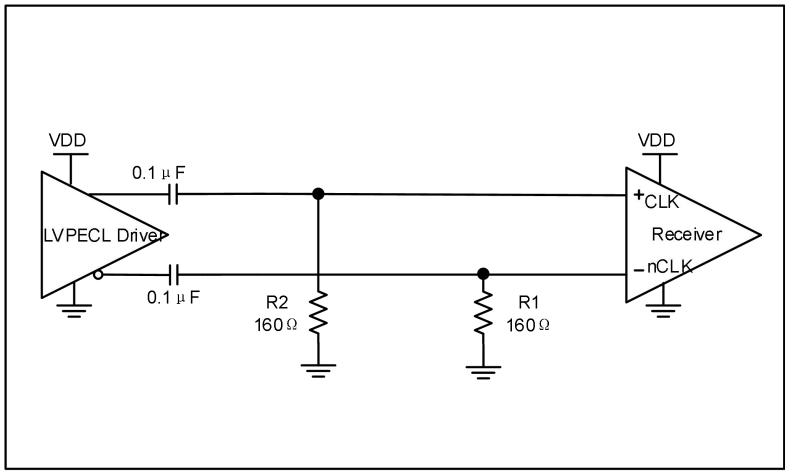
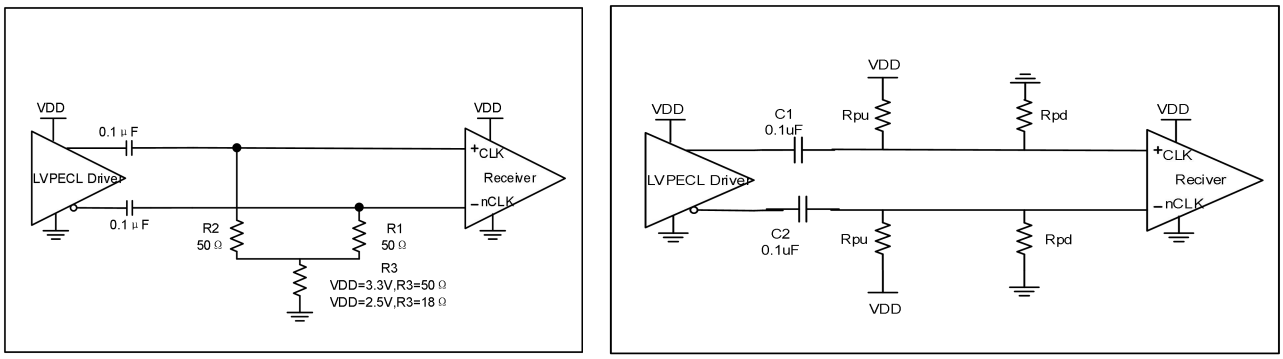


Figure4.Single-termination method of differential input

Input connection circuit

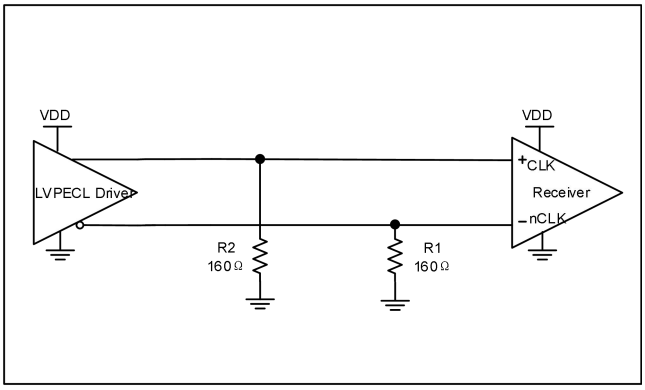
The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both differential signals must meet the VPP and VCMR input requirements. Figure5 to Figure9 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements.

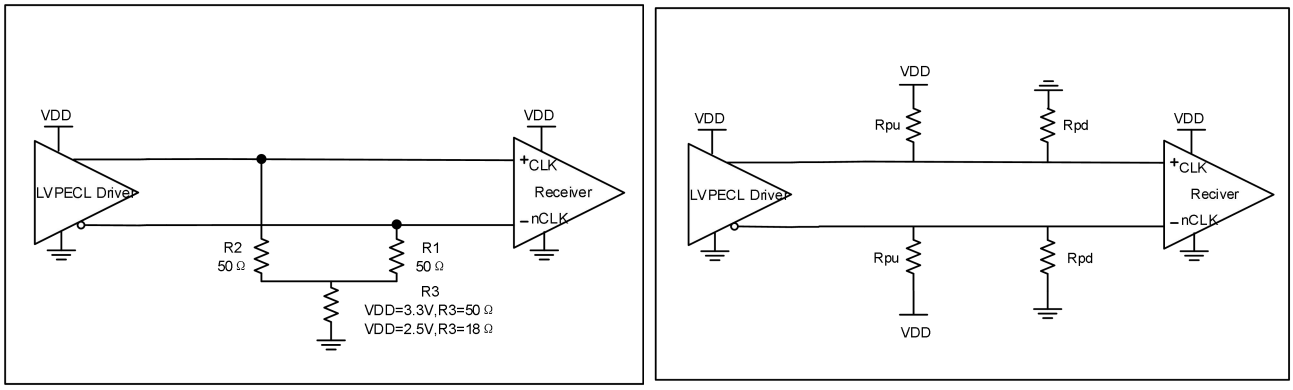




VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

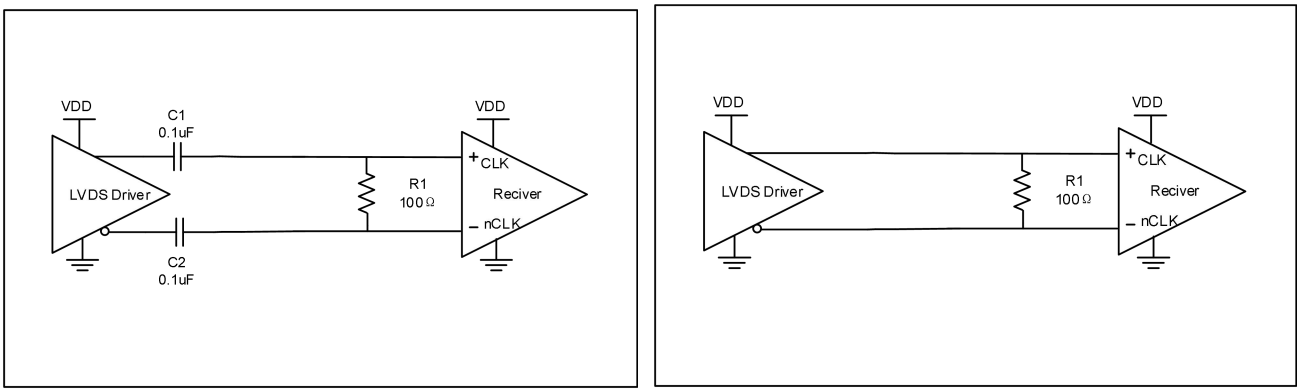
Figure5.LVPECL Driver(AC)





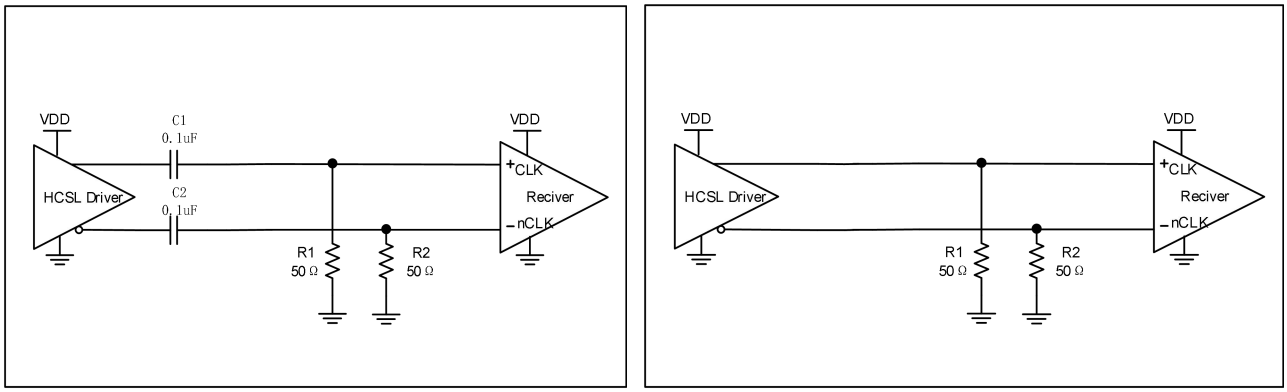
VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

Figure6.LVPECL Driver(DC)



a)AC coupling **b)DC coupling**

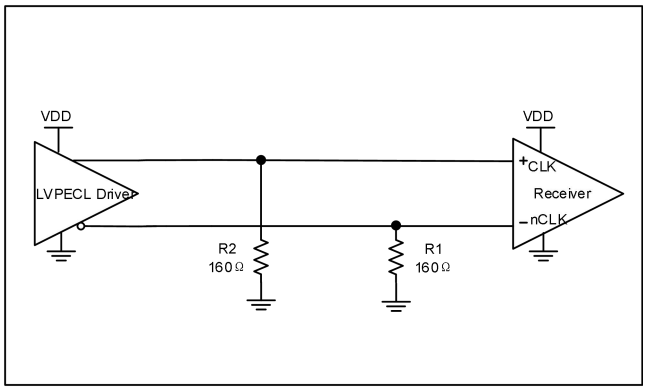
Figure7.LVDS Driver

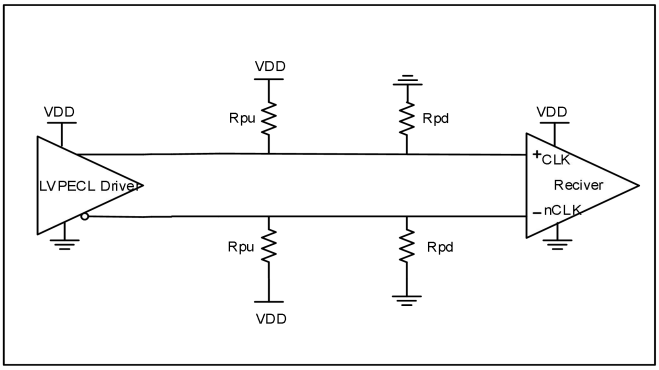


a)AC coupling **b)DC coupling**

Figure8.HCSL Driver

Output connection circuit





VDD	Rpu	Rpd
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

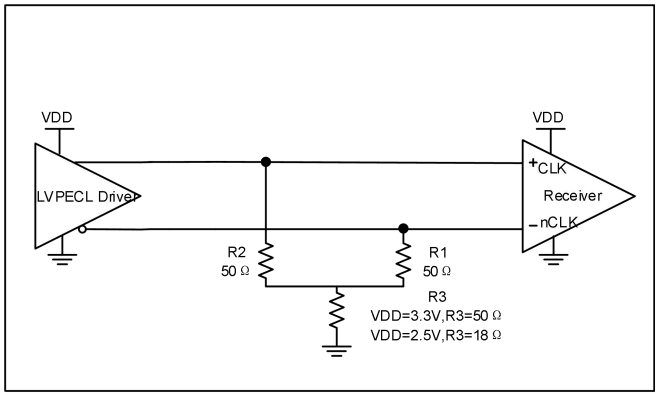
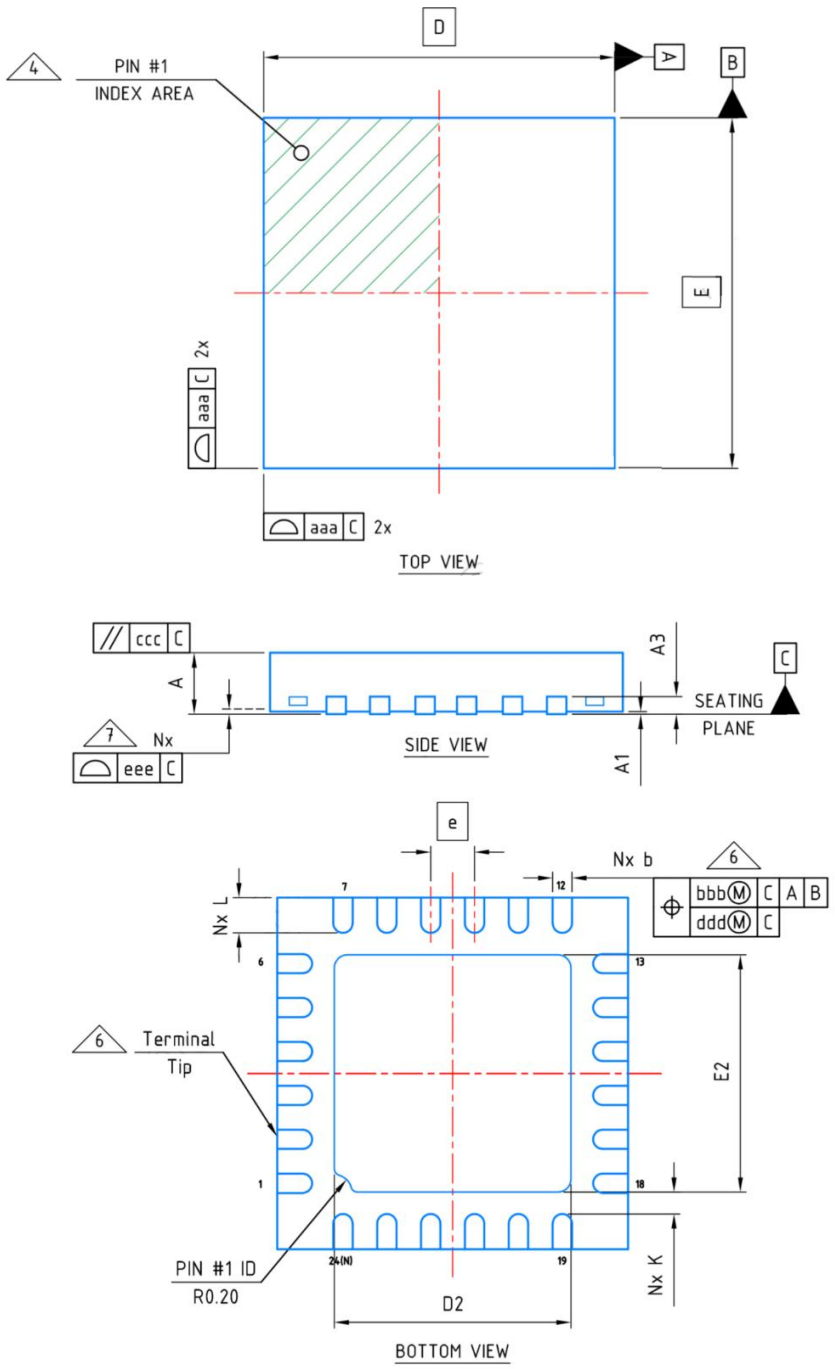


Figure9.LVPECL Driver

PACKAGE DIMENSIONS(QFN-24)



SYMBOL	Millimeter		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	--	0.20	--
b	0.18	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.50 BSC		
D2	2.55	2.70	2.80
E2	2.55	2.70	2.80
K	0.20	--	--
L	0.30	0.40	0.50
aaa	0.05		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
N	24		
ND	6		
NE	6		

Note：

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals on D and E side respectively.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Colanarity applies to the terminals and all other bottom surface metallization.

Reflow profile

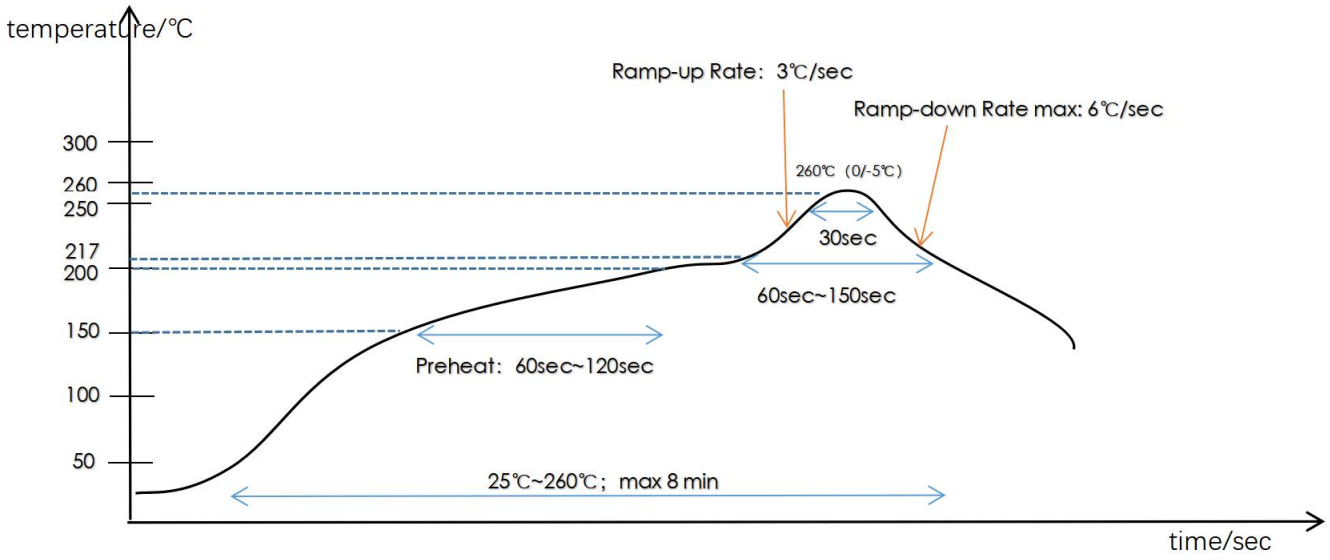


Figure9: Recommended Temperature(PB-Free)

Reflow Condition	Convection or IR/Convection
Average ramp-up rate(217℃ to Peak)	3℃/second max
Preheat temperature 175(±25)℃	60~120 seconds
Temperature maintained above 217℃	60~150 seconds
Time within 5℃ of actual peak temperature	30 seconds
Peak temperature range	260 +0/-5℃
Ramp-down rate	6℃/second max
Time 25℃ to peak temperature	8 minutes max
Maximum number of reflow cycles	≤3

Revision History

Date	Description of Change	Revision
2023.07.10	First Draft.	1.0
2023.10.06	Modified package diagram	1.5