

P-Channel 30V (D-S) MOSFET

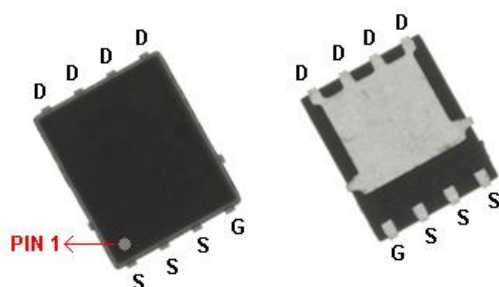
GENERAL DESCRIPTION

The ME7705VT-G is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

Power DFN 5x6

Top View

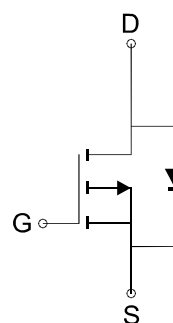


FEATURES

- $R_{DS(ON)}$: 6.5 m Ω (typ.) @ $V_{GS}=-10V$
- $R_{DS(ON)}$: 9.5 m Ω (typ.) @ $V_{GS}=-4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC



P-Channel MOSFET

Ordering Information: ME7705VT-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_A=25^{\circ}C$ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 25	V
Continuous Drain Current	$T_C=25^{\circ}C$	I_D	-41	A
	$T_C=70^{\circ}C$		-33	
	$T_A=25^{\circ}C$		-15	
	$T_A=70^{\circ}C$		-12	
Pulsed Drain Current		I_{DM}	-123	A
Maximum Power Dissipation	$T_C=25^{\circ}C$	P_D	20.8	W
	$T_C=70^{\circ}C$		13	
	$T_A=25^{\circ}C$		2.8	
	$T_A=70^{\circ}C$		1.8	
Operating Junction Temperature		T_J	-55 to 150	$^{\circ}C$
Thermal Resistance-Junction to Case *		$R_{\theta Jc}$	6	$^{\circ}C/W$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	45	$^{\circ}C/W$

* The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μ A	-30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μ A	-1.3		-2.3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±25V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V			-1	μ A
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =-10V, I _D = -20A		6.5	7.8	mΩ
		V _{GS} =-4.5V, I _D = -16A		9.5	12.3	
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V			-1	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V,I _D =-20A	60			nC
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-4.5V, I _D =-20A	31.6			
Q _{gs}	Gate-Source Charge		6.5			
Q _{gd}	Gate-Drain Charge		12.1			
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	2553			pF
C _{oss}	Output Capacitance		433			
C _{rss}	Reverse Transfer Capacitance		375			
t _{d(on)}	Turn-On Delay Time	V _{DS} =-15V, R _L =1Ω V _{GS} =-10V, R _G =3Ω	16.8			ns
t _r	Turn-On Rise Time		55.4			
t _{d(off)}	Turn-Off Delay Time		169			
t _f	Turn-On Fall Time		68.8			

Notes: a. Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$, Guaranteed by design, not subject to production testing.

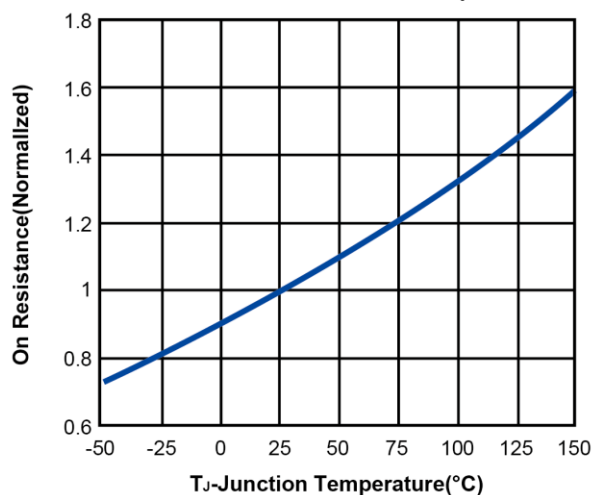
b. Force mos reserves the right to improve or change product design, functions, reliability, qualified manufacturer without notice.

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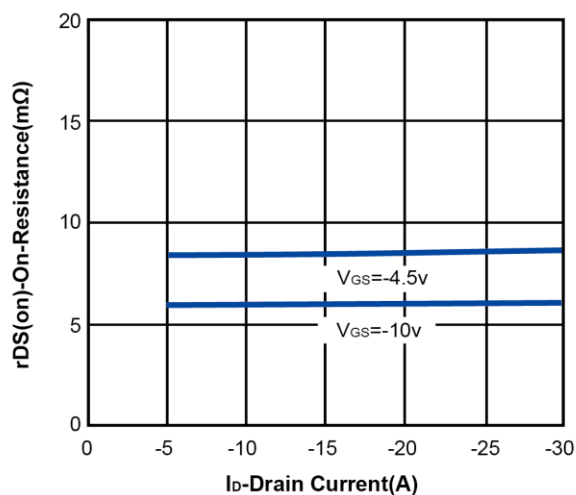
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Typical Characteristics (T_J =25°C Noted)

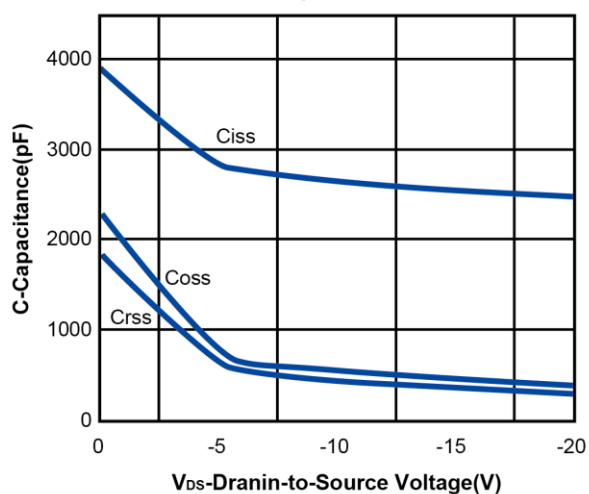
On Resistance vs. Junction Temperature



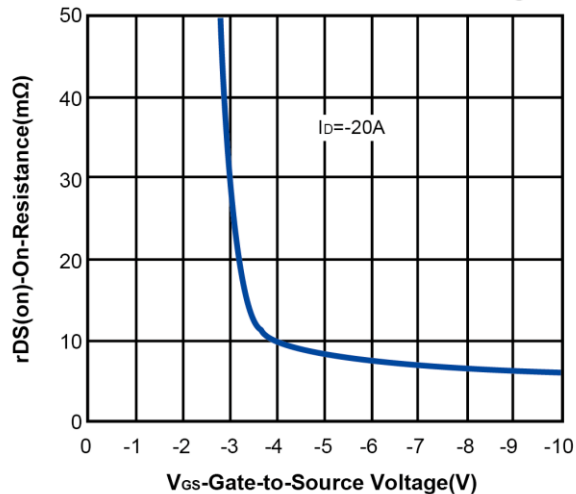
On Resistance vs. Drain Current



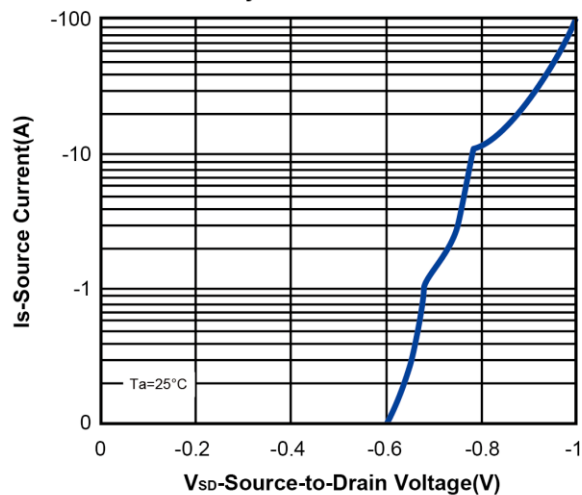
Capacitance



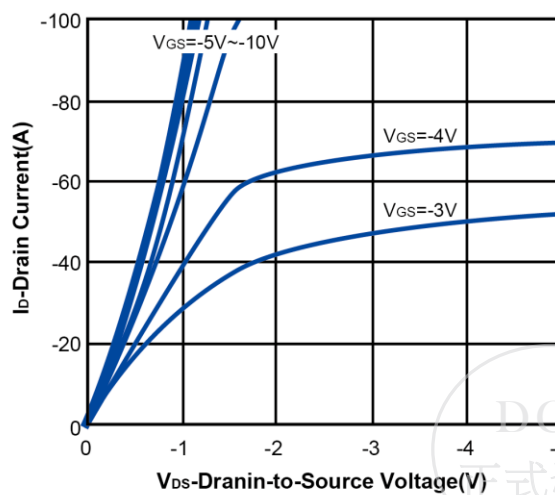
On Resistance vs. Gate-to-Source Voltage



Body-diode characteristics

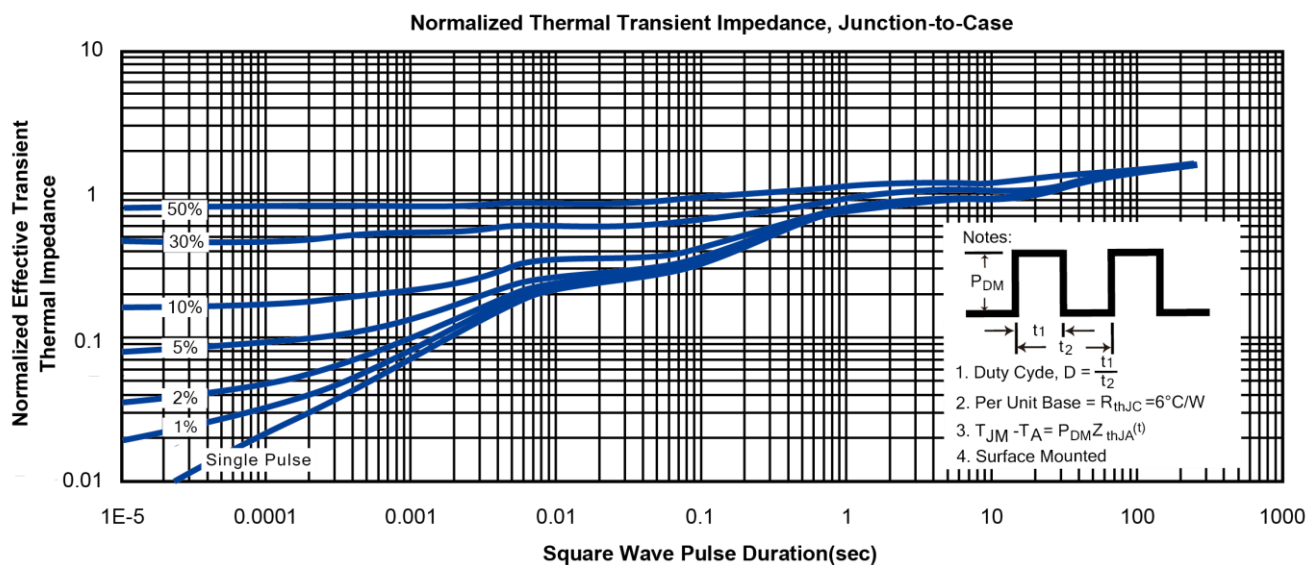
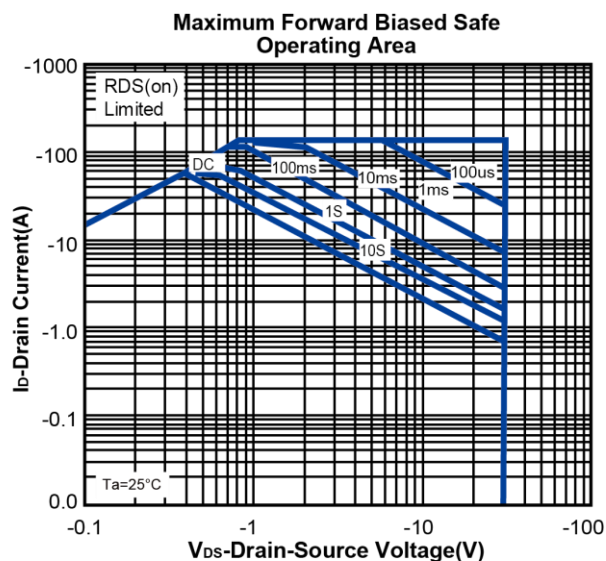
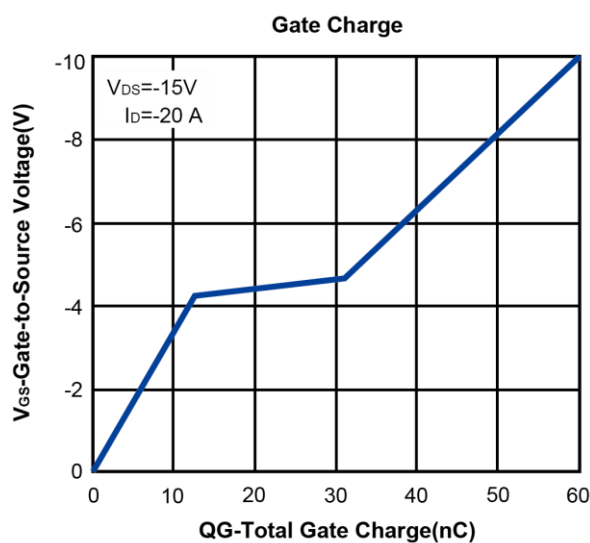


On-Region Characteristics



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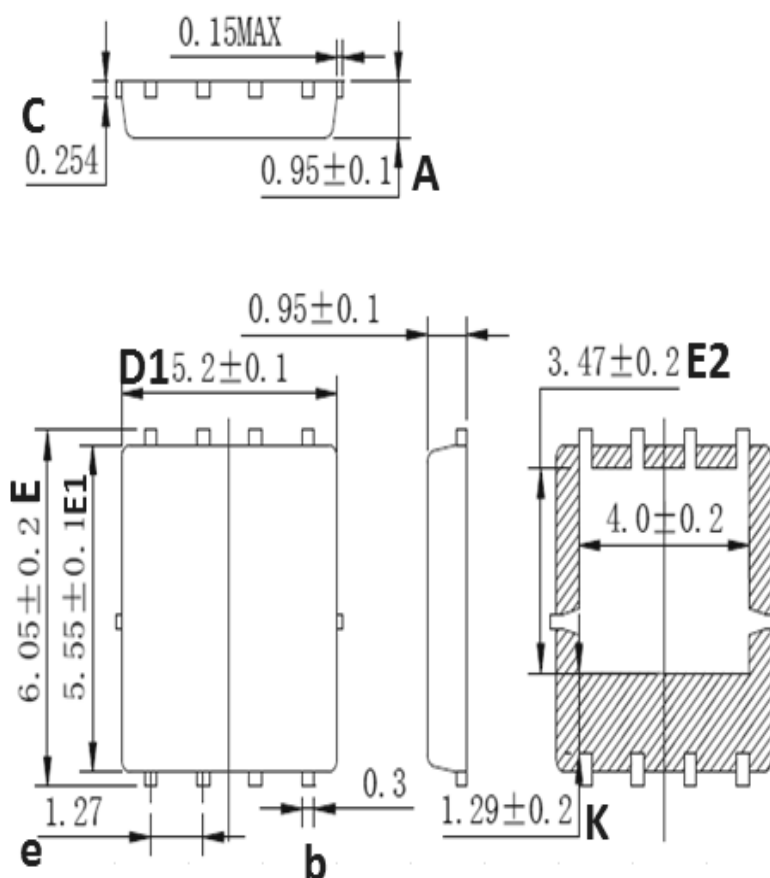
Typical Characteristics (T_J =25°C Noted)



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Power DFN 5x6 Package Outline



SYMBOL	MILLIMETERS(mm)	
	MIN	MAX
A	0.85	1.05
b	0.25	0.35
C	0.20	0.30
D1	5.10	5.30
D2	3.61	3.96
E	5.85	6.25
E1	5.45	5.65
E2	3.27	3.67
e	1.27 BSC	
H	0.56	0.76
K	1.09	1.49
L	0.46	0.66
L1	0.20	0.30

