P-Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The ME7805AS-G is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$: 6.5 mΩ (typ.) @V_{GS}=-10V
- $R_{DS(ON)}$: 10.5 mΩ (typ.) @V_{GS}=-4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

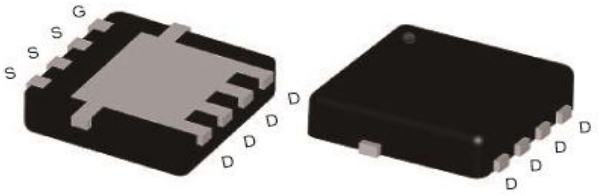
APPLICATIONS

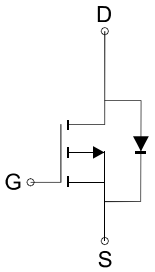
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION

(DFN(S) 3X3)

Top View





P-Channel MOSFET

Ordering Information: ME7805AS-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_C=25℃	I_D	-38	A
	T_C=70℃		-31	
	T_A=25℃		-15	
	T_A=70℃		-12	
Pulsed Drain Current		I_{DM}	-134	A
Maximum Power Dissipation	T_C=25℃	P_D	18.4	W
	T_C=70℃		11.8	
	T_A=25℃		2.78	
	T_A=70℃		1.78	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Case *		$R_{\theta Jc}$	6.8	℃/W
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	45	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1.3		-2.3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance [a]	V_{GS}=-10V, I_D= -20A		6.5	7.8	mΩ
		V_{GS}=-4.5V, I_D= -16A		10.5	12.3	
V_{SD}	Diode Forward Voltage	I_S=-1A, V_{GS}=0V			-1	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-15V, V_{GS}=-10V, I_D=-20A		60		nC
Qg	Total Gate Charge	V_{DS}=-15V, V_{GS}=-4.5V, I_D=-20A		31.6		
Qgs	Gate-Source Charge			6.5		
Qgd	Gate-Drain Charge			12.1		
Ciss	Input Capacitance	V_{DS}=-15V, V_{GS}=0V, f=1MHz		2553		pF
Coss	Output Capacitance			433		
Crss	Reverse Transfer Capacitance			375		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-15V, R_L=1Ω, V_{GS}=-10V, R_G=3Ω		16.8		ns
t_r	Turn-On Rise Time			55.4		
$t_{d(off)}$	Turn-Off Delay Time			169		
t_f	Turn-On Fall Time			68.8		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Force mos reserves the right to improve or change product design, functions, reliability, qualified manufacturer without notice.

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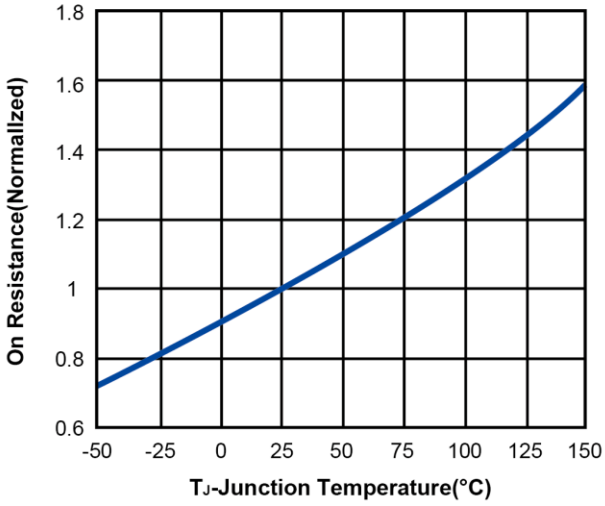
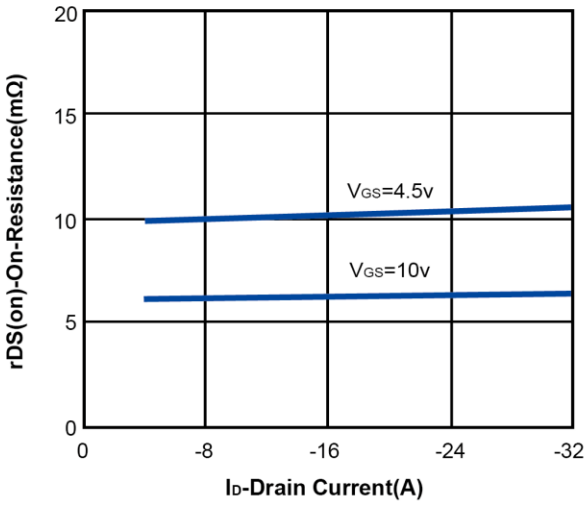
Typical Characteristics (T_J =25℃ Noted)

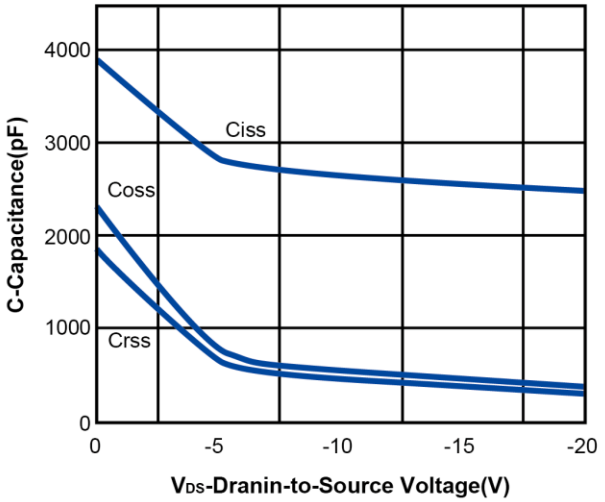
On Resistance vs. Junction Temperature



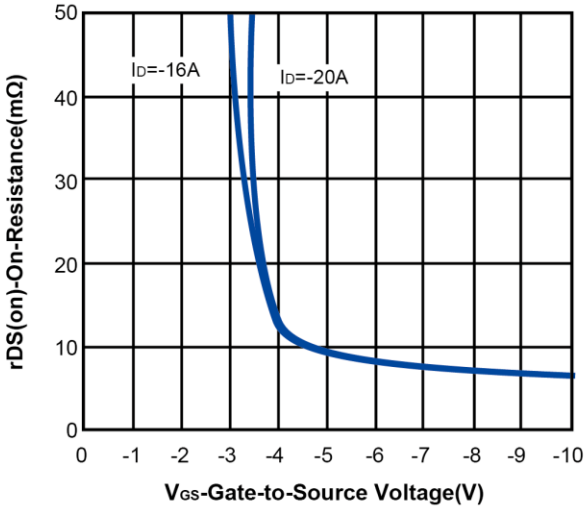
On Resistance vs. Drain Current



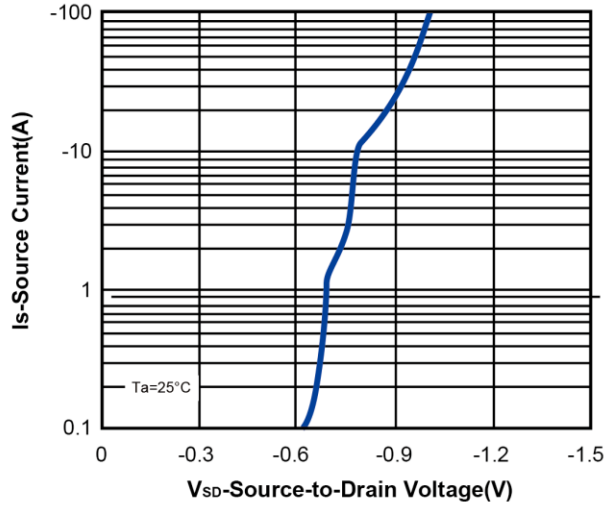
Capacitance



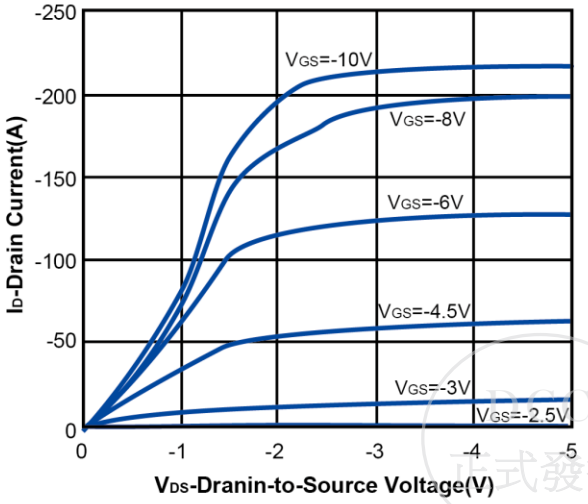
On Resistance vs. Gate-to-Source Voltage



Body-diode characteristics



On-Region Characteristics



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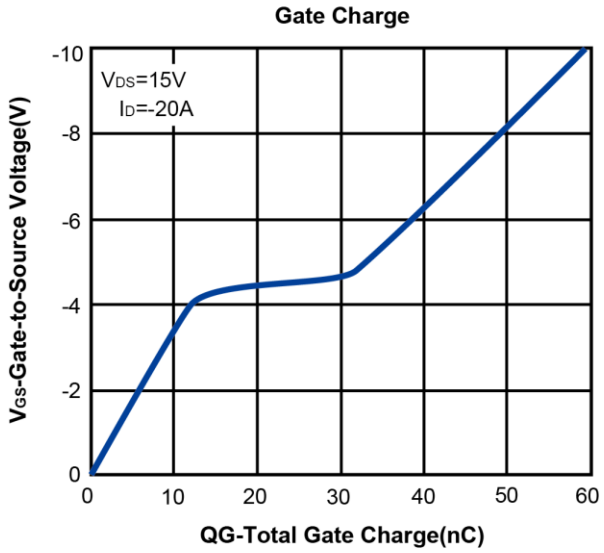

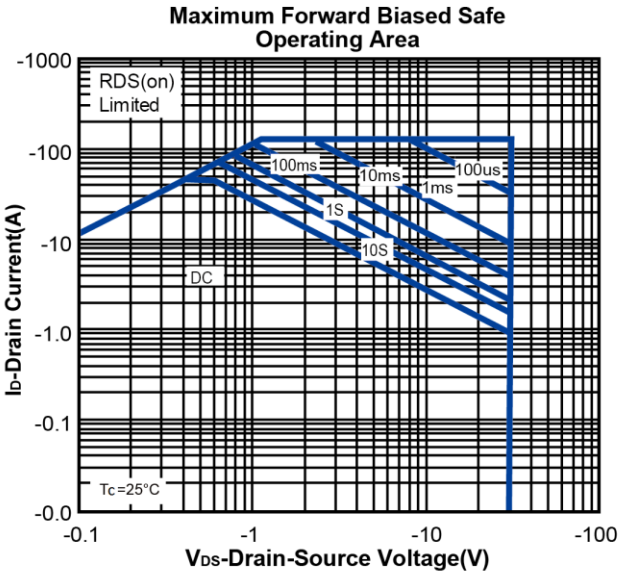

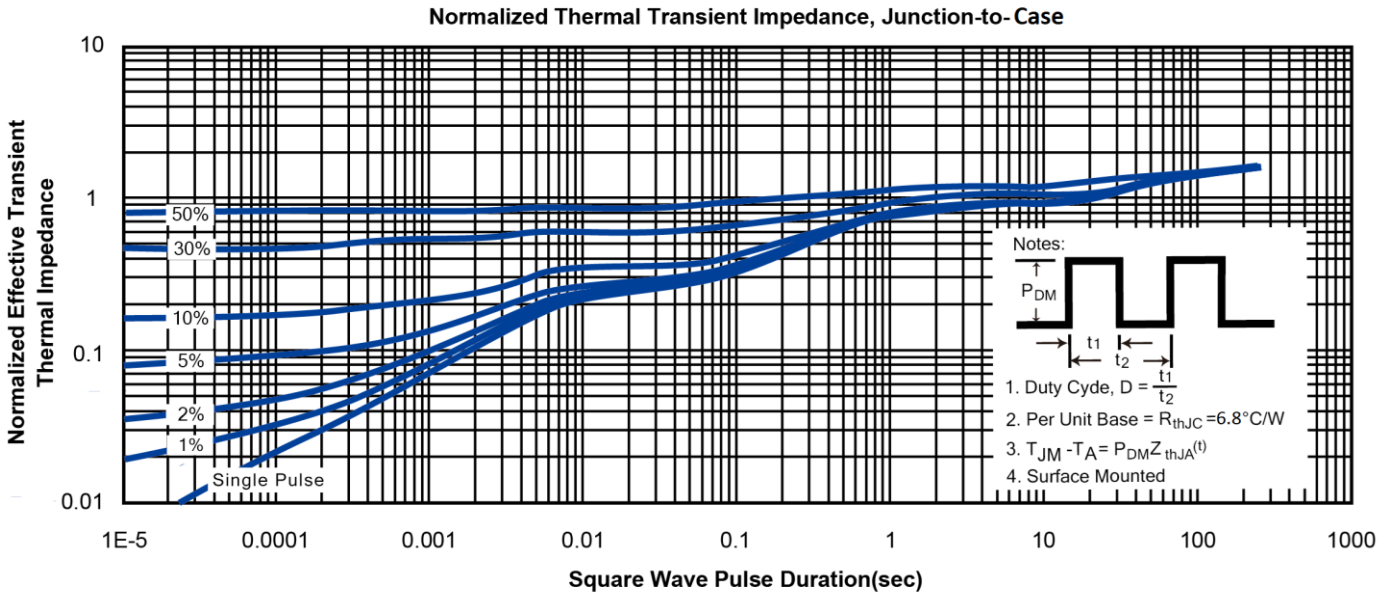

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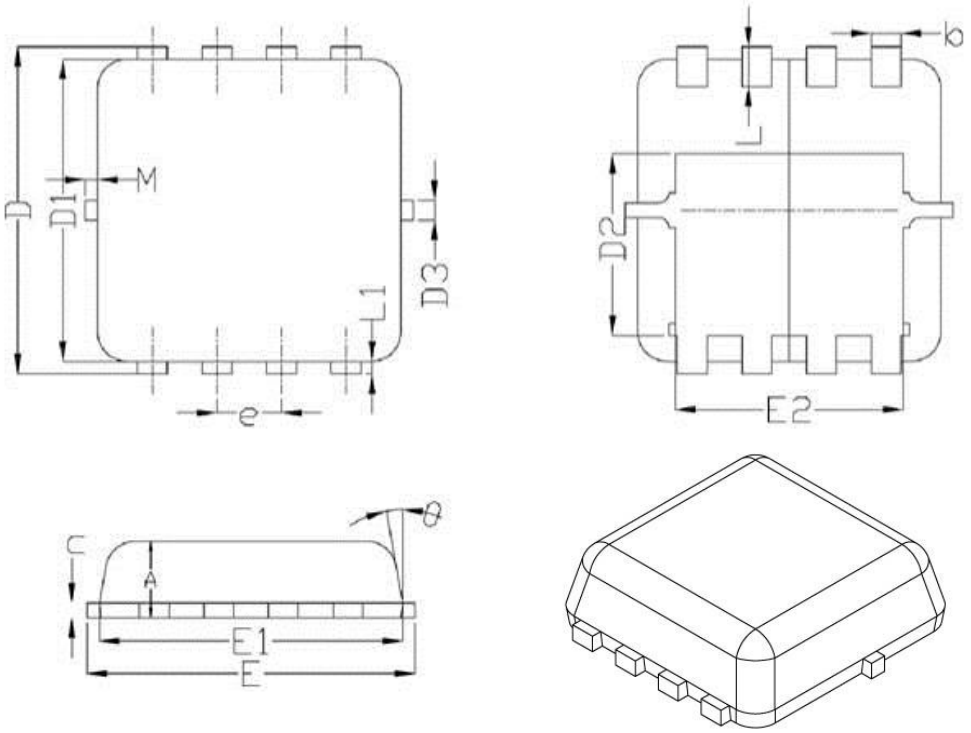
DFN(S) 3X3 Package Outline



SYMBOL	MILLIMETERS (mm)		
	MIN	Typ	MAX
A	0.7	0.8	0.90
b	0.20	0.3	0.40
c	0.08	0.16	0.25
D	2.70	3.1	3.45
D1	2.20	2.7	3.20
D2	1.54	1.8	1.98
D3	0.10	0.2	0.30
E	3.15	3.3	3.45
E1	2.80	3.1	3.30
E2	2.25	2.5	2.65
e	0.65BSC		
H	0.28	0.5	0.68
L	0.30	0.4	0.50
L1	0.06	0.13	0.20
θ	*	*	12°
M	*	*	0.15
*Not specified			