N-Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The ME7232K-G is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and lower power loss that are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦8 mΩ@V_{GS}=10V
- $R_{DS(ON)}$ ≦10 mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

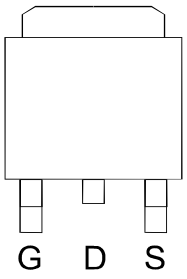
APPLICATIONS

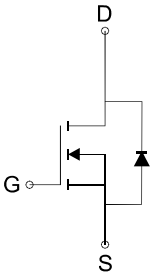
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

(TO-252-3L)

Top View





N-Channel MOSFET

Ordering Information: ME7232K-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current*	T_C=25℃	I_D	46.6	A
	T_C=70℃		37.3	
	T_A=25℃		14.7	
	T_A=70℃		11.8	
Pulsed Drain Current		I_{DM}	140	A
Maximum Power Dissipation*	T_C=25℃	P_D	27.8	W
	T_C=70℃		17.8	
	T_A=25℃		2.8	
	T_A=70℃		1.8	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	4.5	℃/W
Junction-to-Ambient Thermal Resistance*		$R_{\theta JA}$	45	℃/W

*The device mounted on 1in2 FR4 board with 2 oz copper

*Chip silicon limitation current is 100A

Electrical Characteristics (T_J=25℃ Unless Otherwise Specified)

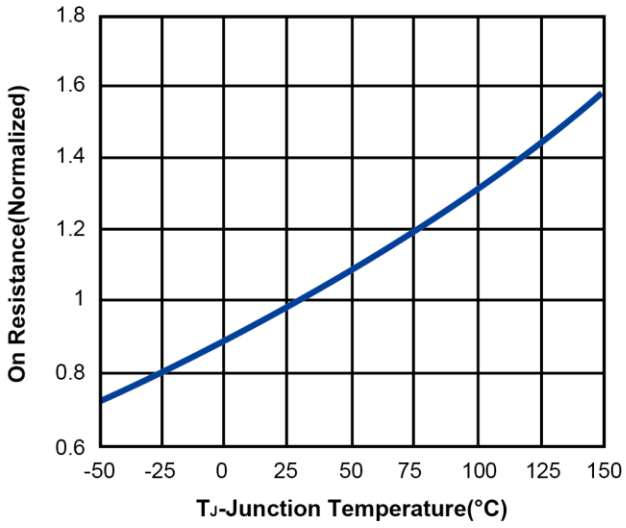
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		2	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D=20A		6	8	mΩ
		V_{GS}=4.5V, I_D=16A		7.5	10	
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V			1	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=20A		38.1		nC
Qgs	Gate-Source Charge			7.5		
Qgd	Gate-Drain Charge			8.2		
Ciss	Input capacitance	V_{DS}=15V, V_{GS}=0V, f=1.0MHz		1692		pF
Coss	Output Capacitance			168		
Crss	Reverse Transfer Capacitance			146		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=15V, R_L=0.75Ω, R_G=6Ω, V_{GS}=10V		19.6		ns
tr	Turn-On Rise Time			257.6		
$t_{d(off)}$	Turn-Off Delay Time			47.7		
t_f	Turn-Off Fall Time			19.6		

Notes: a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

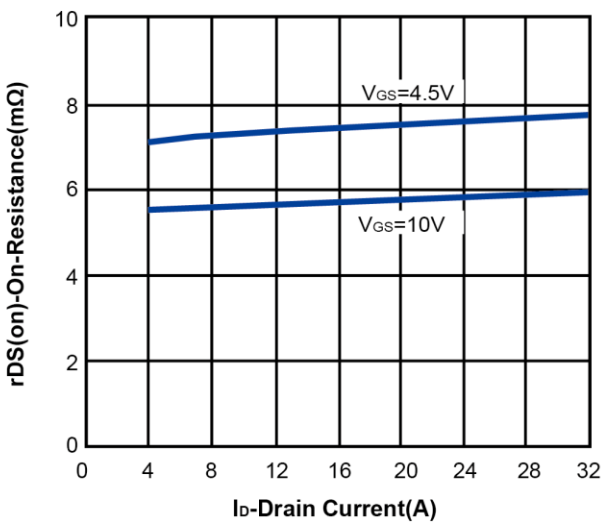
b. Force mos reserves the right to improve or change product design, functions, reliability, qualified manufacturer without notice.

Typical Characteristics (T_J =25℃ Noted)

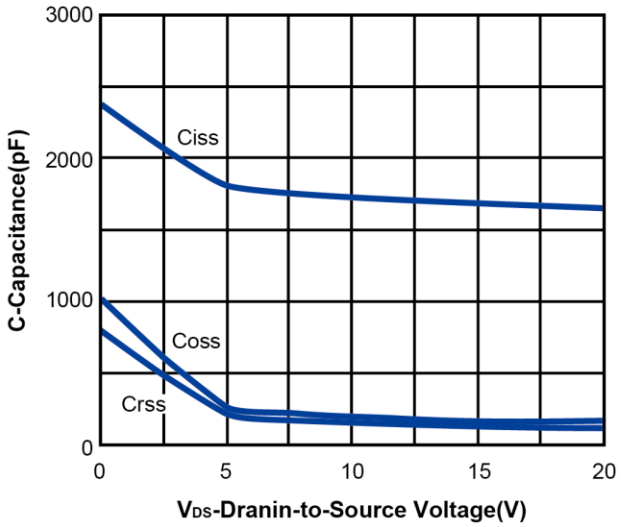
On Resistance vs. Junction Temperature



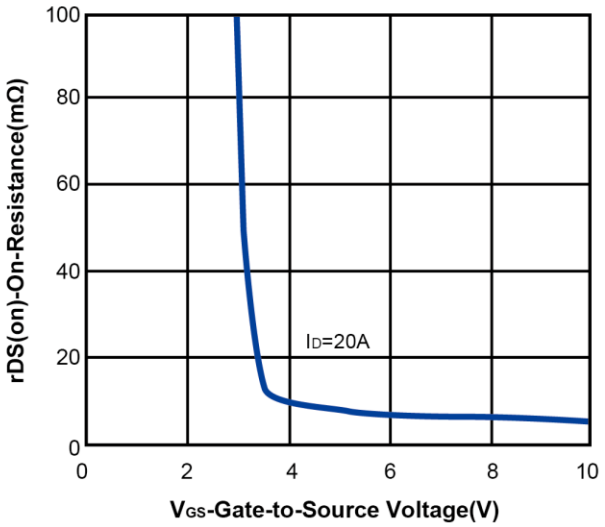
On Resistance vs. Drain Current



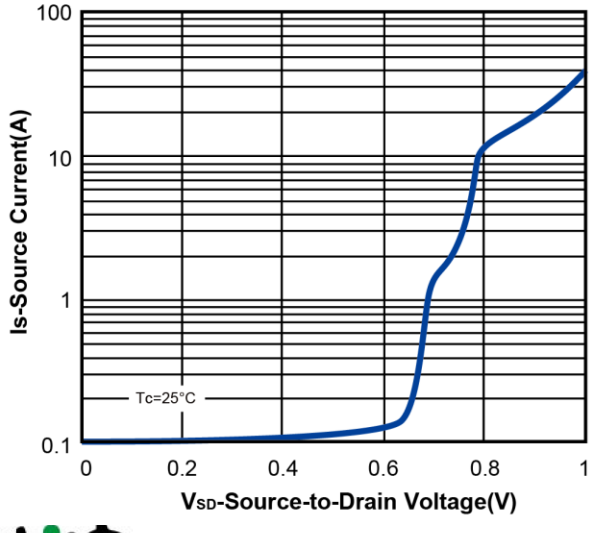
Capacitance



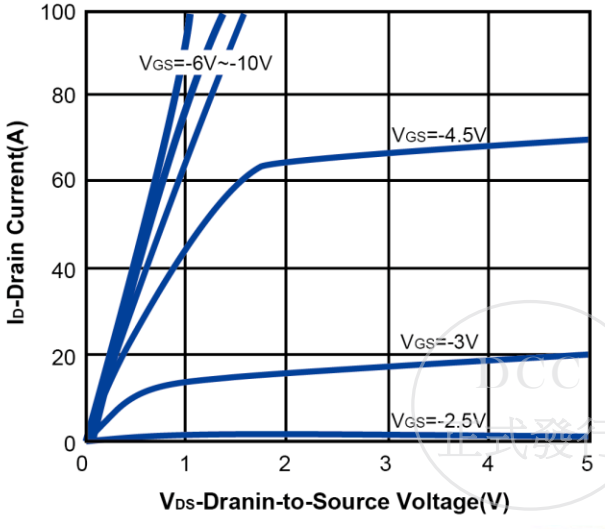
On Resistance vs. Gate-to-Source Voltage



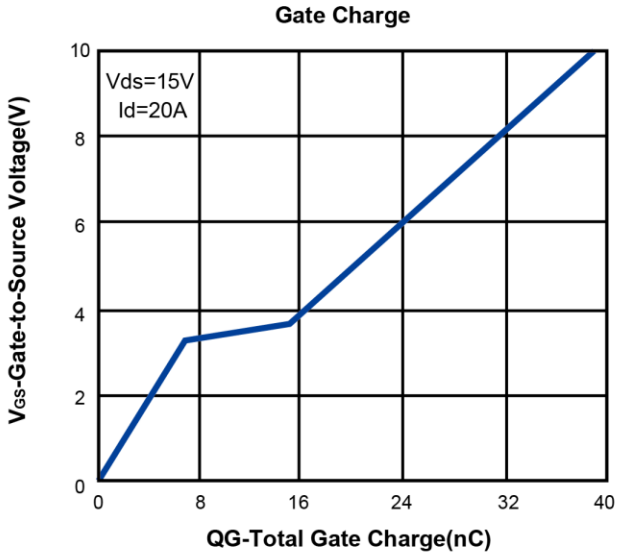
Body-diode characteristics

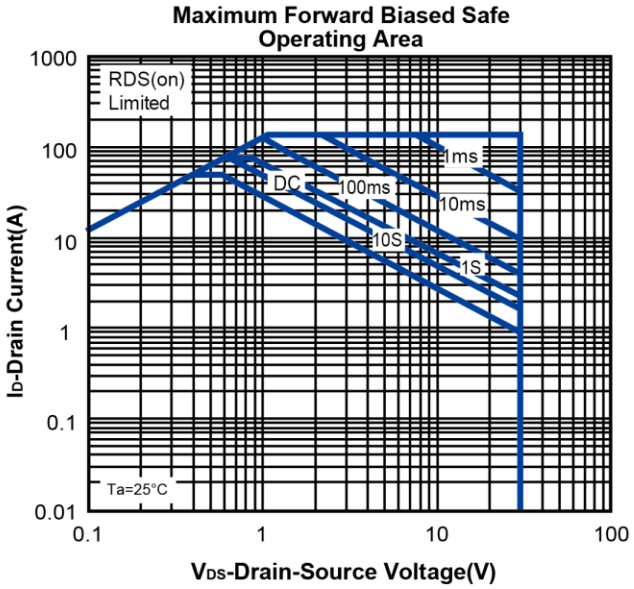


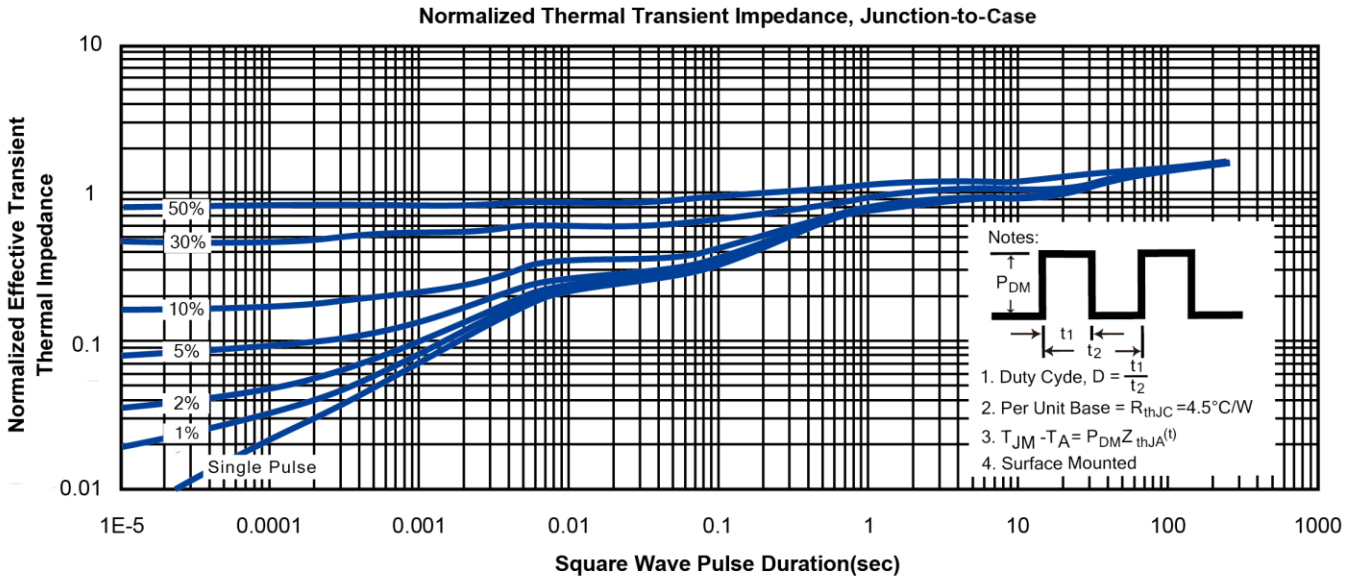
On-Region Characteristics



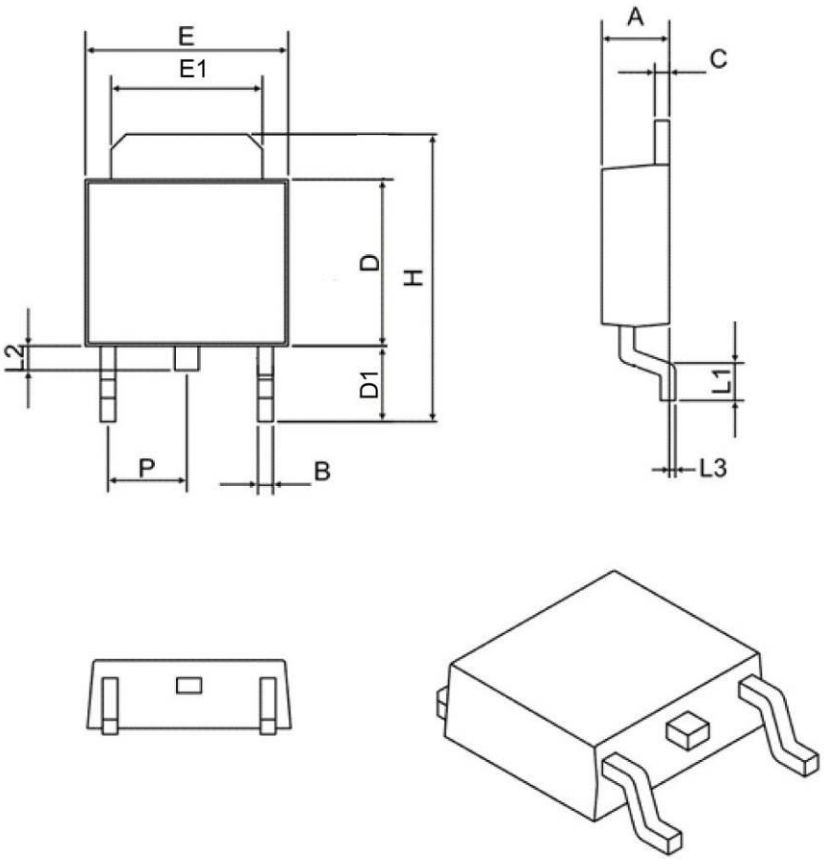
Typical Characteristics (T_J =25℃ Noted)







TO252-3L Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.4
P	2.30 BSC	