MESS138W-G

N - Channel 50-V (D-S) MOSFET

GENERAL DESCRIPTION

The MESS138W-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

FEATURES

- $R_{DS(ON)}$: 1.4 Ω (typ.) @V_{GS}=10V
- $R_{DS(ON)}$: 1.5Ω (typ.) @VGS=4.5V
- $R_{DS(ON)}$: 1.7Ω (typ.) @VGS=2.5V
- $R_{DS(ON)}$: 3Ω (typ.) @VGS=1.8V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

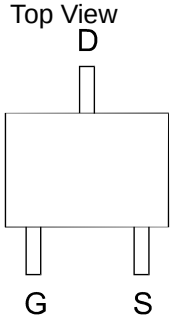
APPLICATIONS

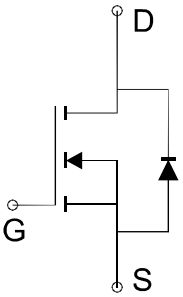
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(SOT-323)

Top View





Ordering Information : MESS138W-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain	T_A=25℃	I_D	350	mA
Pulsed Drain Current		I_{DM}	1050	mA
Maximum Power Dissipation	T_A=25℃	P_D	340	mW
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	367	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

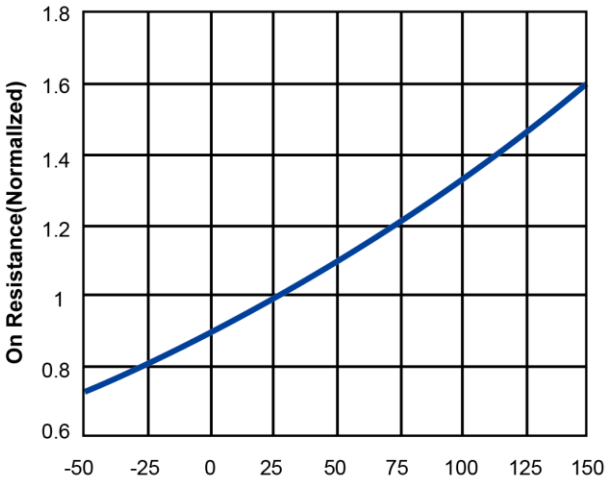
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	50			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.5		1.5	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=50V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	V_{GS}=10V, I_D=500mA		1.4	1.7	Ω
		V_{GS}=4.5V, I_D=200mA		1.5	1.95	
		V_{GS}=2.5V, I_D=100mA		1.7	4	
		V_{GS}=1.8V, I_D=10mA		3	5	
V_{SD}	Diode Forward Voltage *	I_S=500mA, V_{GS}=0V			1.4	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=25V, V_{GS}=4.5V, I_D=300mA		1.9		nC
Qgs	Gate-Source Charge			1.3		
Qgd	Gate-Drain Charge			0.9		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		8.7		Ω
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		34.7		pF
Coss	Output Capacitance			3.3		
Crss	Reverse Transfer Capacitance			2.4		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=25V, R_L=50Ω, V_{GS}=10V, R_G=6Ω		3.6		ns
t_r	Turn-On Rise Time			21.2		
$t_{d(off)}$	Turn-Off Delay Time			3.6		
t_f	Turn-Off Fall Time			41.4		

Notes: a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

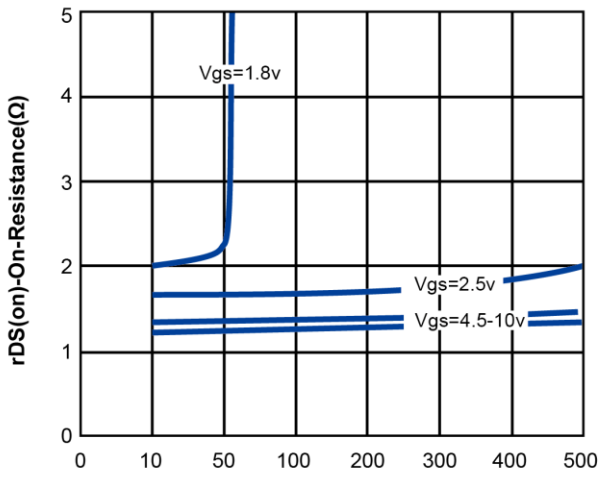
b. Force mos reserves the right to improve or change product design, functions, reliability, qualified manufacturer without notice.

Typical Characteristics (T_J =25°C Noted)

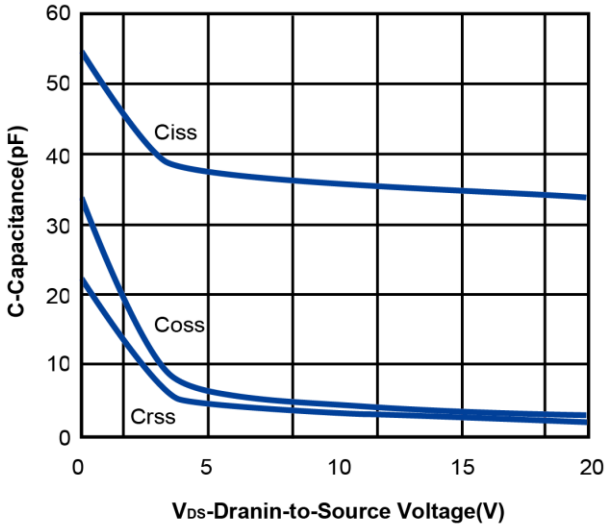
On Resistance vs. Junction Temperature



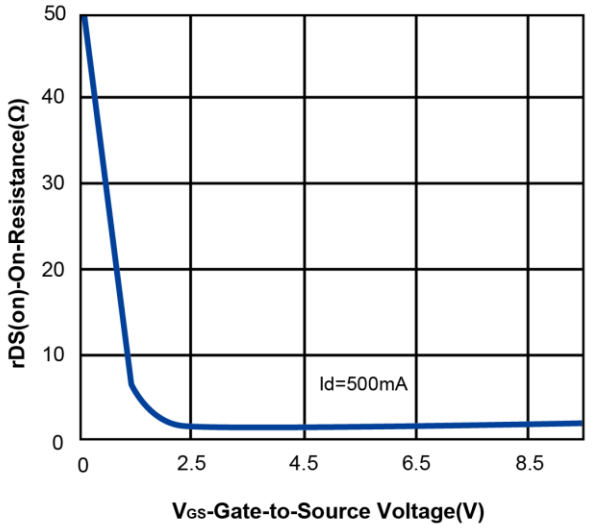
On Resistance vs. Drain Current



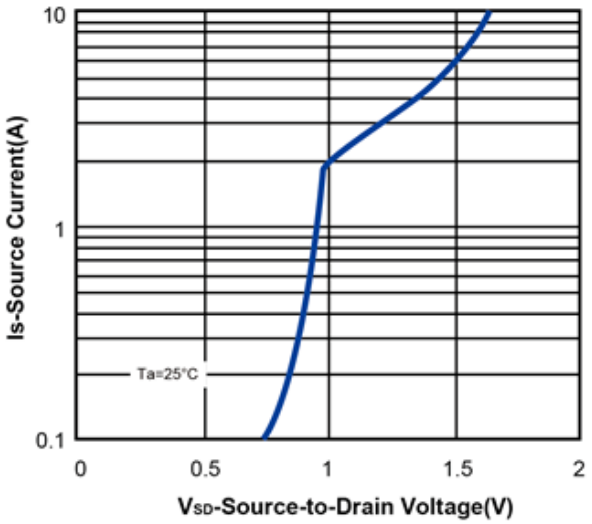
Capacitance



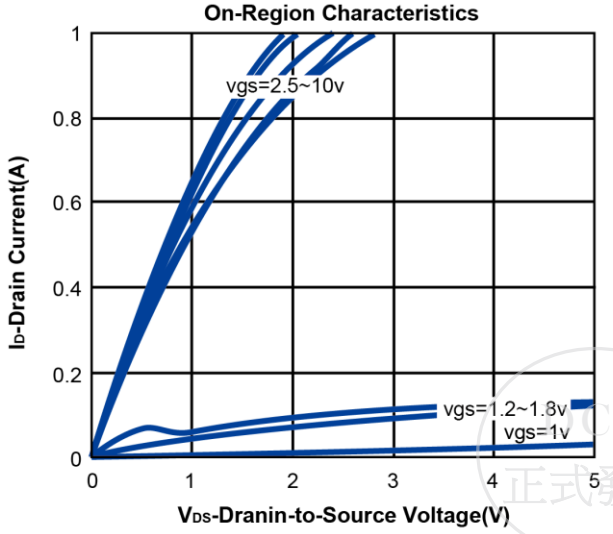
On Resistance vs. Gate-to-Source Voltage



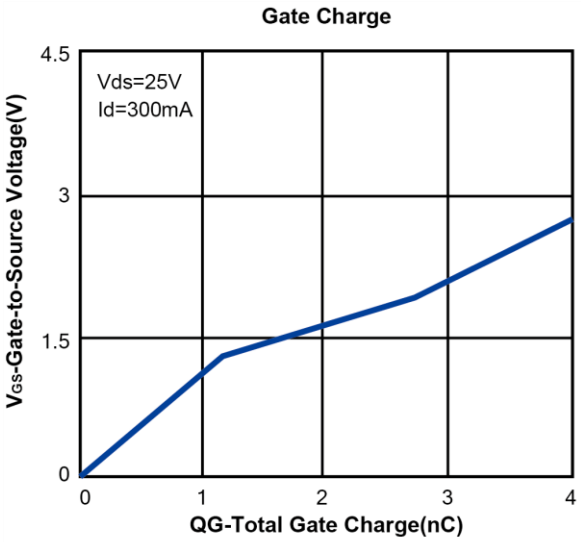
Body-diode characteristics

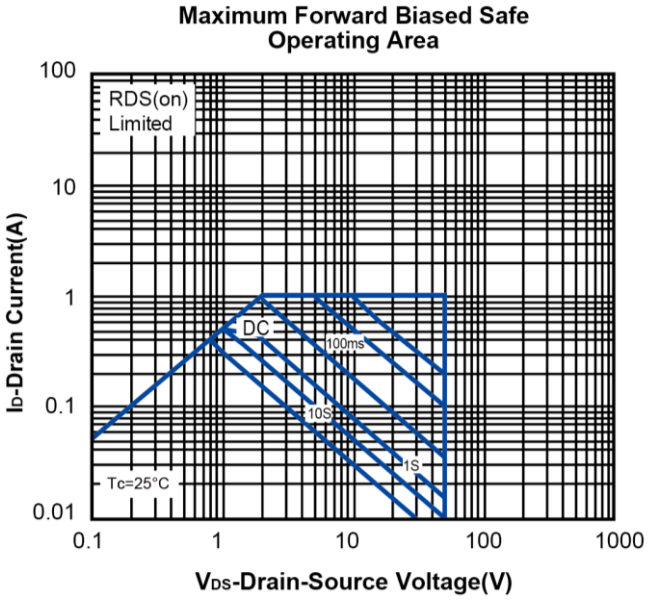


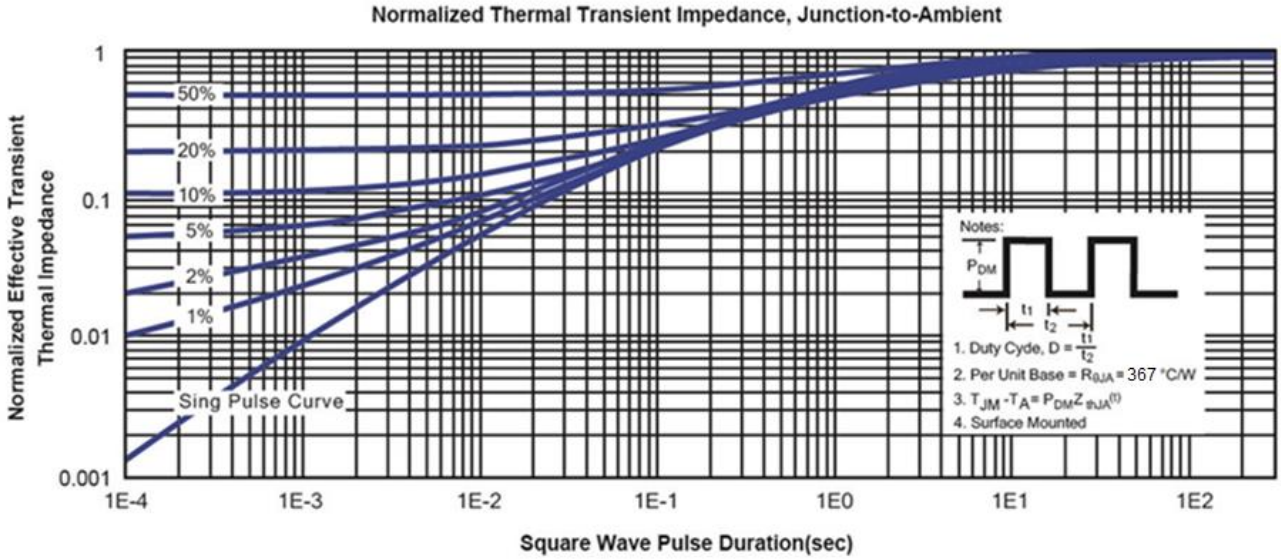
On-Region Characteristics



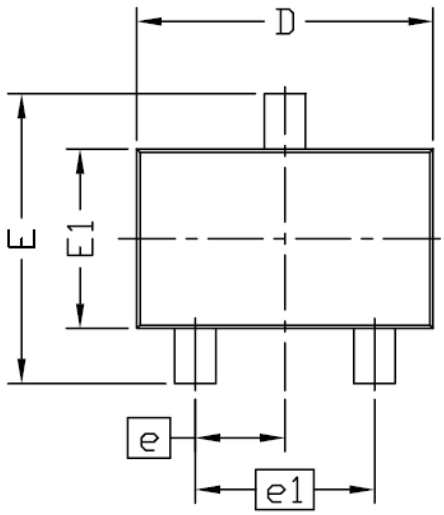
Typical Characteristics (T_J =25℃ Noted)

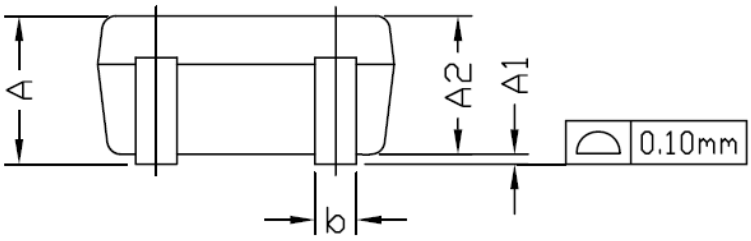


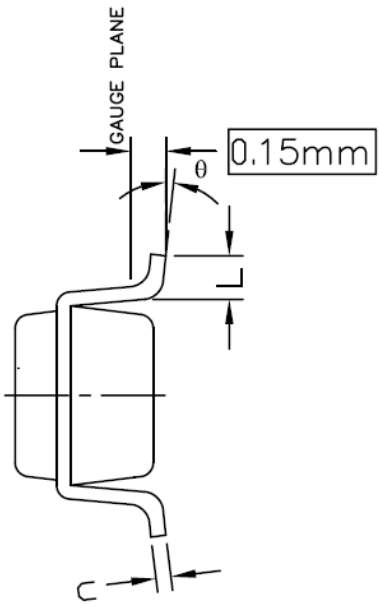




SOT-323 Package





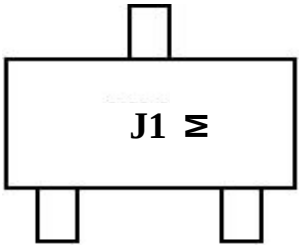


SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.80	1.10
A1	0.00	0.10
A2	0.70	1.00
b	0.20	0.40
c	0.08	0.22
D	1.80	2.20
E	1.80	2.45
e	0.65 BSC	
e1	1.30 BSC	
E1	1.10	1.40
L	0.20	0.46
θ	0°	8°

Device name:MESS138W-G

Package:SOT-323

Marking Code:



J1: Device Marking Code

M: Date code

MONTH CODE

ODD YEARS(2007,2009)

Jan	1
Feb	2
Mar	3
Apr	4
May	5
Jun	6
Jul	7
Aug	8
Sep	9
Oct	T
Nov	V
Dec	C

EVEN YEARS(2006,2008)

Jan	E
Feb	F
Mar	H
Apr	J
May	K
Jun	L
Jul	N
Aug	P
Sep	U
Oct	X
Nov	Y
Dec	Z